1:3 LVPECL CLOCK BUFFER + ADDITIONAL LVCMOS OUTPUT AND PROGRAMMABLE DIVIDER

FEATURES

- **Distributes One Differential Clock Input to Three LVPECL Differential Clock Outputs and One LVCMOS Single-Ended Output**
- **Programmable Output Divider for Two LVPECL Outputs and LVCMOS Output**
- **Low-Output Skew 15 ps (Typical) for Clock-Distribution Applications for LVPECL Outputs; 1.6-ns Output Skew Between LVCMOS and LVPECL Transitions Minimizing Noise**
- **V_{CC} Range 3 V–3.6 V**
- **Signaling Rate Up to 800-MHz LVPECL and 200-MHz LVCMOS**
- **Differential Input Stage for Wide Common-Mode Range**
- **Provides VBB Bias Voltage Output for Single-Ended Input Signals**
- **Receiver Input Threshold ±75 mV**
- **24-Terminal QFN Package (4 mm × 4 mm)**
- **Accepts Any Differential Signaling: LVDS, HSTL, CML, VML, SSTL-2, and Single-Ended: LVTTL/LVCMOS**

DESCRIPTION

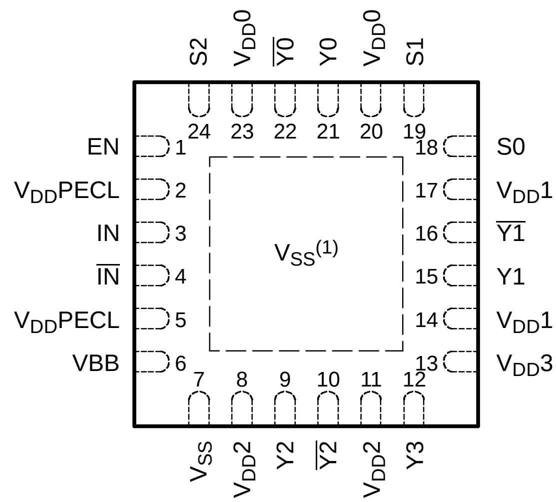
The CDCM1804 clock driver distributes one pair of differential clock inputs to three pairs of LVPECL differential clock outputs Y[2:0] and $\overline{Y[2:0]}$, with minimum skew for clock distribution. The CDCM1804 is specifically designed for driving 50-Ω transmission lines. Additionally, the CDCM1804 offers a single-ended LVCMOS output Y3. This output is delayed by 1.6 ns over the three LVPECL output stages to minimize noise impact during signal transitions.

The CDCM1804 has three control terminals, S0, S1, and S2, to select different output mode settings. The S[2:0] terminals are 3-level inputs and therefore allow up to 3^3 = 27 combinations. Additionally, an enable terminal (EN) is provided to disable or enable all outputs simultaneously. The EN terminal is a 3-level input as well and extends the number of settings to $2 \times 27 = 54$. See Table 1 for details.

The CDCM1804 is characterized for operation from –40°C to 85°C.

For use in single-ended driver applications, the CDCM1804 also provides a VBB output terminal that can be directly connected to the unused input as a common-mode voltage reference.

RGE PACKAGE (TOP VIEW)



(1) Thermal pad must be connected to V_{SS}.

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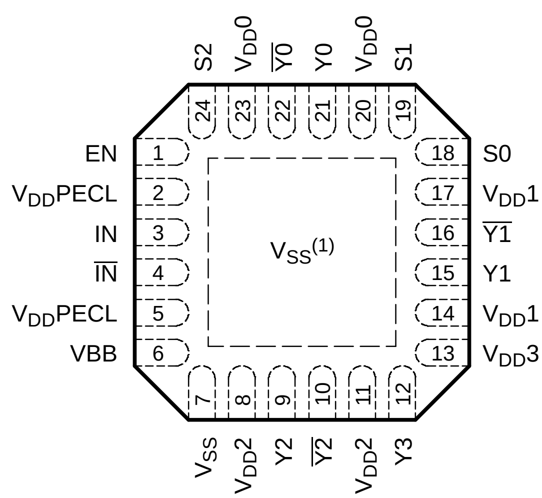
RTH PACKAGE (TOP VIEW)



(1) Thermal pad must be connected to V_{SS}.

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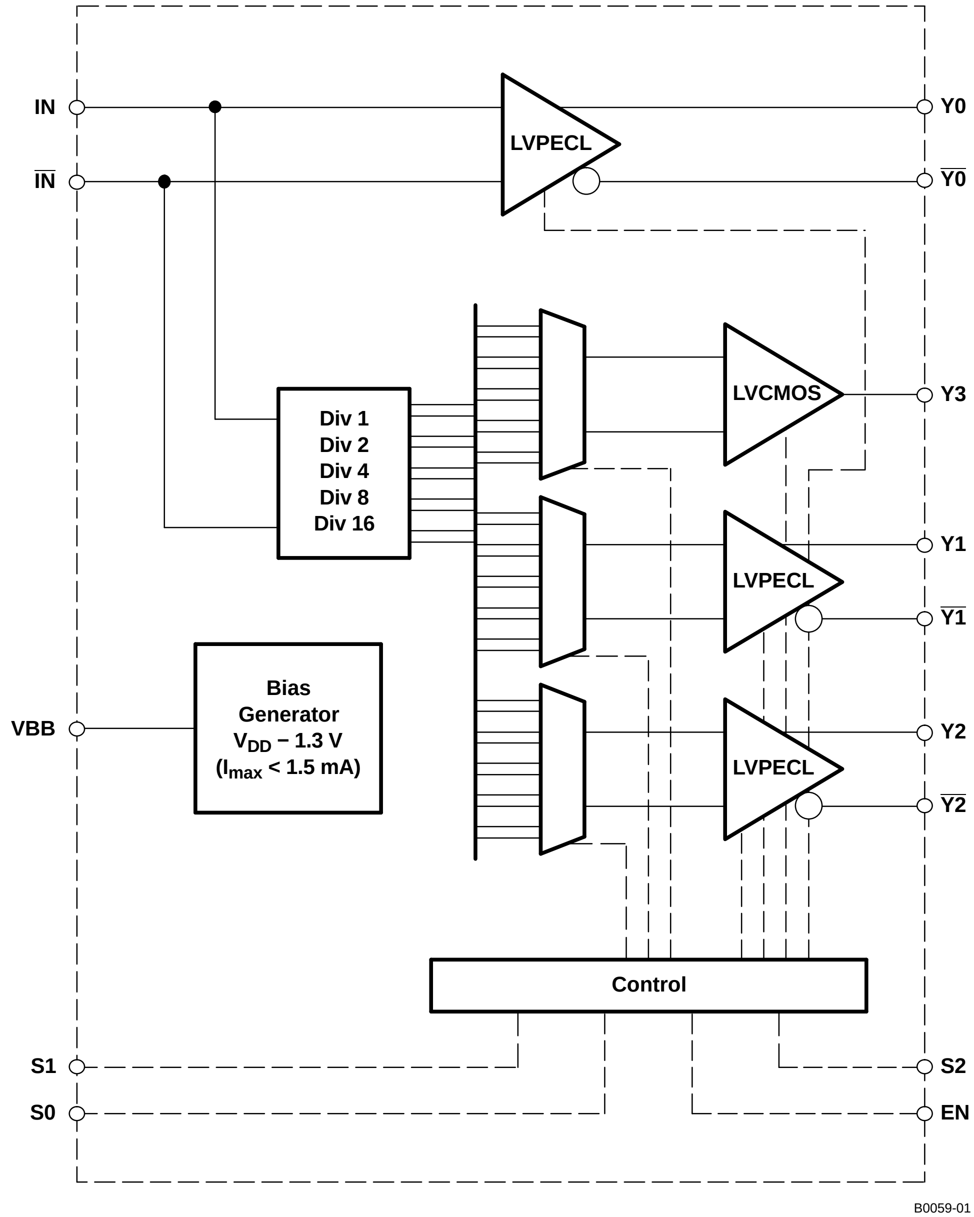
FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	1	I (with 60-kΩ pullup)	ENABLE: Enables or disables all outputs simultaneously. The EN terminal offers three different configurations: tied to GND (logic 0), external 60-kΩ pulldown resistor (pull to V_{DD}/2), or left floating (logic 1); EN = 1: outputs on according to S[2:0] settings EN = V_{DD}/2: outputs on according to S[2:0] settings EN = 0: outputs Y[3:0] off (high impedance) See Table 1 for details.
IN, $\overline{\text{IN}}$	3, 4	I (differential)	Differential input clock: Input stage is sensitive and has a wide common-mode range. Therefore, almost any type of differential signal can drive this input (LVPECL, LVDS, CML, HSTL). Because the input is high-impedance, it is recommended to terminate the PCB transmission line before the input (e.g., with 100 Ω across input). Input can also be driven by single-ended signal if the complementary input is tied to VBB. A more-advanced scheme for single-ended signals is given in the *Application Information* section near the end of this document. The inputs employ an ESD structure protecting the inputs in case of an input voltage exceeding the rails by more than ~0.7 V. Reverse biasing of the IC through these inputs is possible and must be prevented by limiting the input voltage < V_{DD}.
S[2:0]	18, 19, 24	I (with 60-kΩ pullup)	Select mode of operation: Defines the output configuration of Y[3:0]. Each terminal offers three different configurations: tied to GND (logic 0), external 60-kΩ pulldown resistor (pull to V_{DD}/2), or left floating (logic 1); see Table 1 for details.
VBB	6	O	Bias voltage output to be used to bias unused complementary input $\overline{\text{IN}}$ for single-ended input signals. The output voltage of VBB is V_{DD} – 1.3 V. When driving a load, the output current drive is limited to about 1.5 mA.
V_{SS}	7	Supply	Device ground
V_{DD}PECL	2, 5	Supply	Supply voltage LVPECL input + internal logic
V_{DD}[2:0]	8, 11, 14, 17, 20, 23	Supply	LVPECL output supply voltage for output Y[2:0]. Each output can be disabled by pulling the corresponding V_{DD}x to GND. **CAUTION:** In this mode, no voltage from outside may be forced, because internal diodes could be forced in forward direction. Thus, it is recommended to disconnect the output.
V_{DD}3	13	Supply	Supply voltage LVCMOS output. The LVCMOS output can be disabled by pulling V_{DD}3 to GND. **CAUTION:** In this mode, no voltage from outside may be forced because internal diodes could be forced in a forward direction. Thus, it is recommended to leave Y3 unconnected, tied to GND, or terminated into GND.
Y[2:0] $\overline{\text{Y[2:0]}}$	9, 15, 21 10, 16, 22	O (LVPECL)	LVPECL clock outputs. These outputs provide low-skew copies of IN or down-divided copies of clock IN based on selected mode of operation S[2:0]. If an output is unused, the output can simply be left open to save power and minimize noise impact to the remaining outputs.
Y3	12	O	LVCMOS clock output. This output provides copy of IN or down-divided copy of clock IN based on selected mode of operation S[2:0]. Also, this output can be disabled when V_{DD}3 becomes tied to GND.

CONTROL TERMINAL SETTINGS

The CDCM1804 has three control terminals (S0, S1, and S2) and an enable terminal (EN) to select different output mode settings. All four inputs (S0, S1, S2, and EN) are 3-level inputs offering 54 different combinations. In addition, the EN input allows the disabling of all outputs and forcing them into a high-z (or 3-state) output state when pulled to GND.

Each control input incorporates a 60-kΩ pullup resistor. Thus, it is easy to choose the input setting by designing a resistor pad between the control input and GND. To choose a logic zero, the resistor value must be zero. Setting the input high requires leaving the resistor pad empty (no resistor installed). For setting the input to V_{DD}/2, the installed resistor must be a 60-kΩ pulldown to GND with a 10% tolerance or better.

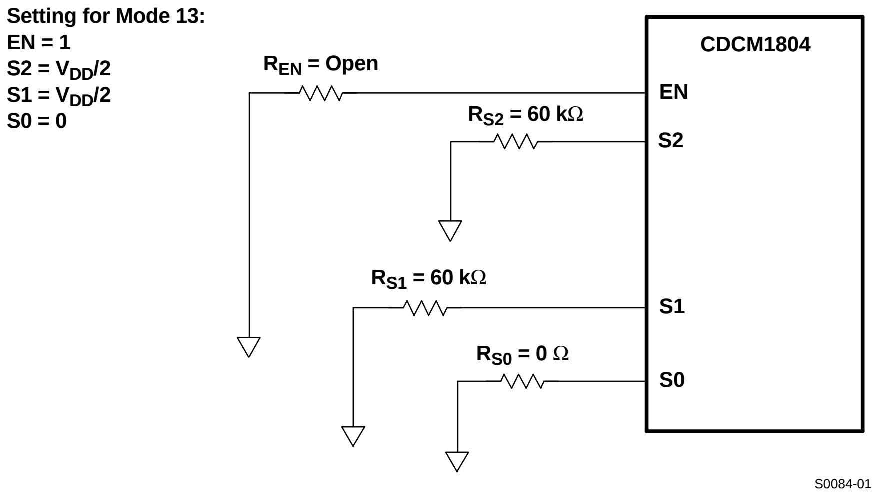


Figure 1. Control Terminal Setting for Example

Table 1. Selection Mode Table

					LVPECL (1)			LVCMOS
MODE	EN	S2	S1	S0	Y0	Y1	Y2	Y3
0	0	x	x	x	Off (high-z)			
1	1	0	0	0	÷ 1	÷ 1	÷ 1	Off (high-z)
2	1	0	0	V_{DD}/2	÷ 1	Off (high-z)	Off (high-z)	÷ 4
3	1	0	0	1	÷ 1	÷ 1	Off (high-z)	÷ 4
4	1	0	V_{DD}/2	0	÷ 1	÷ 2	Off (high-z)	÷ 4
5	1	0	V_{DD}/2	V_{DD}/2	÷ 1	÷ 4	Off (high-z)	÷ 4
6	1	0	V_{DD}/2	1	÷ 1	÷ 8	Off (high-z)	÷ 4
7	1	0	1	0	÷ 1	Off (high-z)	÷ 1	÷ 4
8	1	0	1	V_{DD}/2	÷ 1	÷ 1	÷ 1	÷ 4
9	1	0	1	1	÷ 1	÷ 2	÷ 1	÷ 4
10	1	V_{DD}/2	0	0	÷ 1	÷ 4	÷ 1	÷ 4
11	1	V_{DD}/2	0	V_{DD}/2	÷ 1	÷ 8	÷ 1	÷ 4
12	1	V_{DD}/2	0	1	÷ 1	Off (high-z)	÷ 2	÷ 4
13	1	V_{DD}/2	V_{DD}/2	0	÷ 1	÷ 1	÷ 2	÷ 4
14	1	V_{DD}/2	V_{DD}/2	V_{DD}/2	÷ 1	÷ 2	÷ 2	÷ 4
15	1	V_{DD}/2	V_{DD}/2	1	÷ 1	÷ 4	÷ 2	÷ 4
16	1	V_{DD}/2	1	0	÷ 1	÷ 8	÷ 2	÷ 4
17	1	V_{DD}/2	1	V_{DD}/2	÷ 1	Off (high-z)	÷ 4	÷ 4
18	1	V_{DD}/2	1	1	÷ 1	÷ 1	÷ 4	÷ 4
19	1	1	0	0	÷ 1	÷ 2	÷ 4	÷ 4
20	1	1	0	V_{DD}/2	÷ 1	÷ 4	÷ 4	÷ 4
21	1	1	0	1	÷ 1	÷ 8	÷ 4	÷ 4
22	1	1	V_{DD}/2	0	÷ 1	Off (high-z)	÷ 8	÷ 4
23	1	1	V_{DD}/2	V_{DD}/2	÷ 1	÷ 1	÷ 8	÷ 4
24	1	1	V_{DD}/2	1	÷ 1	÷ 2	÷ 8	÷ 4
25	1	1	1	0	÷ 1	÷ 4	÷ 8	÷ 4

(1) The LVPECL outputs are open-emitter stages. Thus, if you leave the unused LVPECL outputs Y0, Y1, or Y2 unconnected, then the current consumption is minimized and noise impact to remaining outputs is neglectable. Also, each output can be individually disabled by connecting the corresponding V_{DD} input to GND.

Table 1. Selection Mode Table (continued)

					LVPECL[1]			LVCMOS
MODE	EN	S2	S1	S0	Y0	Y1	Y2	Y3
26	1	1	1	$V_{DD}/2$	÷ 1	÷ 8	÷ 8	÷ 4
27	1	1	1	1	÷ 1	Off (high-z)	÷ 16	÷ 4
28	$V_{DD}/2$	0	0	0	÷ 1	÷ 1	÷ 16	÷ 4
29	$V_{DD}/2$	0	0	$V_{DD}/2$	÷ 1	÷ 2	÷ 16	÷ 4
30	$V_{DD}/2$	0	0	1	÷ 1	÷ 4	÷ 16	÷ 4
31	$V_{DD}/2$	0	$V_{DD}/2$	0	÷ 1	÷ 8	÷ 16	÷ 4
32	$V_{DD}/2$	0	$V_{DD}/2$	$V_{DD}/2$	÷ 1	Off (high-z)	Off (high-z)	÷ 1
33	$V_{DD}/2$	0	$V_{DD}/2$	1	÷ 1	÷ 1	Off (high-z)	÷ 1
34	$V_{DD}/2$	0	1	0	÷ 1	÷ 2	Off (high-z)	÷ 1
35	$V_{DD}/2$	0	1	$V_{DD}/2$	÷ 1	÷ 1	Off (high-z)	÷ 2
36	$V_{DD}/2$	0	1	1	÷ 1	÷ 2	Off (high-z)	÷ 2
37	$V_{DD}/2$	$V_{DD}/2$	0	0	÷ 1	Off (high-z)	Off (high-z)	÷ 2
38	$V_{DD}/2$	$V_{DD}/2$	0	$V_{DD}/2$	÷ 1	÷ 1	÷ 1	÷ 2
39	$V_{DD}/2$	$V_{DD}/2$	0	1	÷ 1	÷ 2	÷ 8	÷ 2
40	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$	0	÷ 1	÷ 2	÷ 8	÷ 8
41	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$	÷ 1	÷ 4	Off (high-z)	÷ 1
42	$V_{DD}/2$	$V_{DD}/2$	$V_{DD}/2$	1	÷ 1	÷ 8	Off (high-z)	÷ 1
43	$V_{DD}/2$	$V_{DD}/2$	1	0	÷ 1	÷ 4	Off (high-z)	÷ 2
44	$V_{DD}/2$	$V_{DD}/2$	1	$V_{DD}/2$	÷ 1	÷ 8	Off (high-z)	÷ 2
45	$V_{DD}/2$	$V_{DD}/2$	1	1	÷ 1	÷ 1	÷ 2	÷ 2
46	$V_{DD}/2$	1	0	0	÷ 1	Off (high-z)	Off (high-z)	÷ 8
47	$V_{DD}/2$	1	0	$V_{DD}/2$	÷ 1	÷ 4	Off (high-z)	÷ 8
48	$V_{DD}/2$	1	0	1	÷ 1	÷ 4	÷ 8	÷ 8
49	$V_{DD}/2$	1	$V_{DD}/2$	0	÷ 1	÷ 8	Off (high-z)	÷ 8
50	$V_{DD}/2$	1	$V_{DD}/2$	$V_{DD}/2$	÷ 1	÷ 2	÷ 8	÷ 16
Rsv	$V_{DD}/2$	1	$V_{DD}/2$	1	Reserved	Reserved	Reserved	Reserved
Rsv	$V_{DD}/2$	1	1	0	N/A	Low	Low	Low
53	$V_{DD}/2$	1	1	$V_{DD}/2$	÷ 1	÷ 1	÷ 1	÷ 1
54	$V_{DD}/2$	1	1	1	÷ 1	÷ 1	÷ 1	÷ 1

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)[1]

V_{DD}	Supply voltage	–0.3 V to 3.8 V
V_I	Input voltage	–0.2 V to (V_{DD} + 0.2 V)
V_O	Output voltage	–0.2 V to (V_{DD} + 0.2 V)
	Differential short-circuit current, Yn, $\overline{Yn}$, I_{OSD}	Continuous
	Electrostatic discharge (HBM 1.5 kΩ, 100 pF), ESD	>2000 V
	Moisture level 24-terminal QFN package (solder reflow temperature of 235°C) MSL	2
T_{stg}	Storage temperature	–65°C to 150°C
T_J	Maximum junction temperature	125°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	–40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

LVPECL INPUT IN, $\overline{IN}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	Input frequency		0		800	MHz
V_{CM}	High-level input common mode		1		V_{DD} – 0.3	V
V_{IN}	Input voltage swing between IN and $\overline{IN}$(1)		500		1300	mV
	Input voltage swing between IN and $\overline{IN}$(2)		150		1300	
I_{IN}	Input current	V_I = V_{DD} or 0 V			±10	µA
R_{IN}	Input impedance		300			kΩ
C_I	Input capacitance at IN, $\overline{IN}$			1		pF

(1) Is required to maintain ac specifications
(2) Is required to maintain device functionality

LVPECL OUTPUT DRIVER Y[2:0], $\overline{Y[2:0]}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{clk}	Output frequency, see Figure 4		0		800	MHz
V_{OH}	High-level output voltage	Termination with 50 Ω to V_{DD} – 2 V	V_{DD} – 1.18		V_{DD} – 0.81	V
V_{OL}	Low-level output voltage	Termination with 50 Ω to V_{DD} – 2 V	V_{DD} – 1.98		V_{DD} – 1.55	V
V_O	Output voltage swing between Y and $\overline{Y}$, see Figure 4.	Termination with 50 Ω to V_{DD} – 2 V	500			mV
I_{OZL}	Output 3-state current	V_{DD} = 3.6 V, V_O = 0 V			5	µA
I_{OZH}		V_{DD} = 3.6 V, V_O = V_{DD} – 0.8 V			10	
t_r/t_f	Rise and fall time	20% to 80% of V_{OUTPP}, see Figure 9.	200		350	ps
$t_{skpecl(o)}$	Output skew between any LVPECL output Y[2-0] and $\overline{Y[2-0]}$	See Note A in Figure 8.		15	30	ps
t_{Duty}	Output duty-cycle distortion(1)	Crossing point-to-crossing point distortion	–50		50	ps
$t_{sk(pp)}$	Part-to-part skew	Any Y, see Note B in Figure 8.		50		ps
C_O	Output capacitance	V_O = V_{DD} or GND		1		pF
LOAD	Expected output load			50		Ω

(1) For an 800-MHz signal, the 50-ps error would result in a duty-cycle distortion of ±4% when driven by an ideal clock input signal.

LVPECL INPUT-TO-LVPECL OUTPUT PARAMETERS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LVPECL INPUT-TO-LVPECL OUTPUT PARAMETER						
$t_{pd(lh)}$	Propagation delay rising edge	VOX to VOX	320		600	ps
$t_{pd(hl)}$	Propagation delay falling edge	VOX to VOX	320		600	ps
$t_{sk(p)}$	LVPECL pulse skew	VOX to VOX, see Note C in Figure 8.			100	ps

LVCMOS OUTPUT PARAMETER, Y3

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clk}	OUTPUT frequency, see Figure 5[(1)].			0		200	MHz
$t_{skLVCMOS(o)}$	Output skew between the LVCMOS output Y3 and LVPECL outputs Y[2:0]	VOX to V_{DD}/2, see Figure 8.		1.3	1.6	2.1	ns
$t_{sk(pp)}$	Part-to-part skew	Y3, see Note B in Figure 8.			300		ps
V_{OH}	High-level output voltage	V_{DD} = min to max	I_{OH} = –100 µA	V_{DD} – 0.1			V
		V_{DD} = 3 V	I_{OH} = –6 mA	2.4			
		V_{DD} = 3 V	I_{OH} = –12 mA	2			
V_{OL}	Low-level output voltage	V_{DD} = min to max	I_{OL} = 100 µA			0.1	V
		V_{DD} = 3 V	I_{OL} = 6 mA			0.5	
		V_{DD} = 3 V	I_{OL} = 12 mA			0.8	
I_{OH}	High-level output current	V_{DD} = 3.3 V	V_O = 1.65 V		–29		mA
I_{OL}	Low-level output current	V_{DD} = 3.3 V	V_O = 1.65 V		37		mA
I_{OZ}	High-impedance-state output current	V_{DD} = 3.6 V	V_O = V_{DD} or 0 V			±5	µA
C_O	Output capacitance	V_{DD} = 3.3 V			2		pF
t_{Duty}	Output duty cycle distortion[(2)]	Measured at V_{DD}/2		–150		150	ps
$t_{pd(lh)}$	Propagation delay rising edge from IN to Y3	VOX to V_{DD}/2 load, see Figure 10.		1.6		2.6	ns
$t_{pd(hl)}$	Propagation delay falling edge from IN to Y3	VOX to V_{DD}/2 load, see Figure 10.		1.6		2.6	ns
t_r	Output rise slew rate	20% to 80% of swing, see Figure 10.		1.4	2.3		V/ns
t_f	Output fall slew rate	80% to 20% of swing, see Figure 10.		1.4	2.3		V/ns

(1) Operating the CDCM1804 LVCMOS output above the maximum frequency does not cause a malfunction to the device, but the Y3 output will not achieve enough signal swing to meet the output specification. Therefore, the CDCM1804 can be operated at higher frequencies, while the LVCMOS output Y3 becomes unusable.
(2) For a 200-MHz signal, the 150-ps error would result in a duty cycle distortion of ±3% when driven by an ideal clock input signal.

JITTER CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{jitterLVPECL}$	Additive phase jitter from input to LVPECL output Y[2:0], see Figure 2.	12 kHz to 20 MHz, f_{out} = 250 MHz to 800 MHz, divide-by-1 mode			0.15	ps rms
		50 kHz to 40 MHz, f_{out} = 250 MHz to 800 MHz, divide-by-1 mode			0.25	
$t_{jitterLVCMOS}$	Additive phase jitter from input to LVCMOS output Y3, see Figure 3.	12 kHz to 20 MHz, f_{out} = 250 MHz, divide-by-1 mode			0.25	ps rms
		50 kHz to 40 MHz, f_{out} = 250 MHz, divide-by-1 mode			0.4	

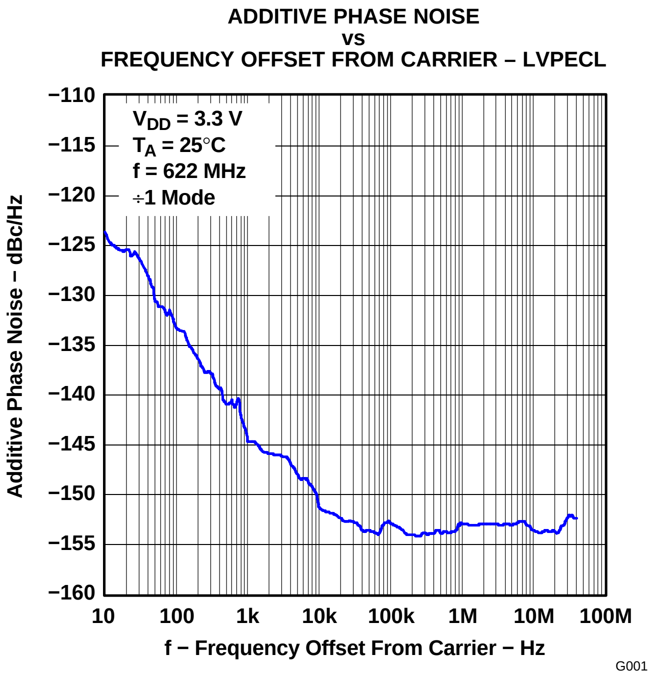


Figure 2.

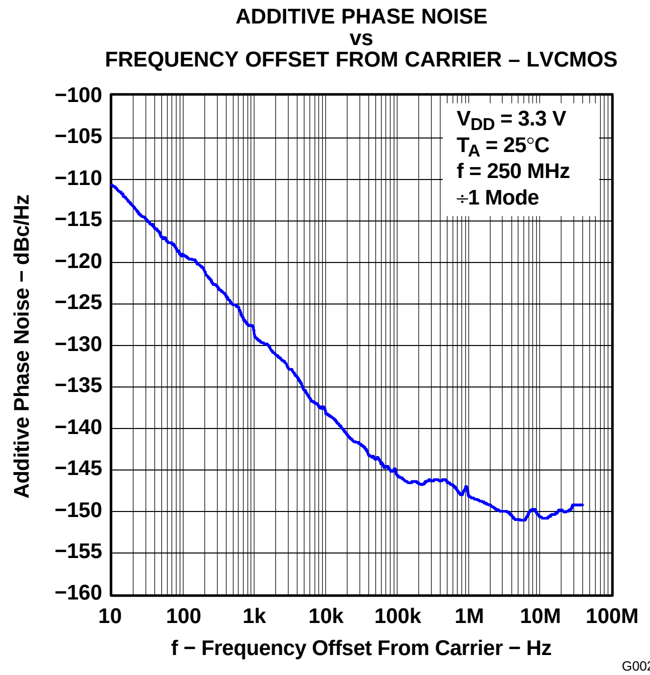


Figure 3.

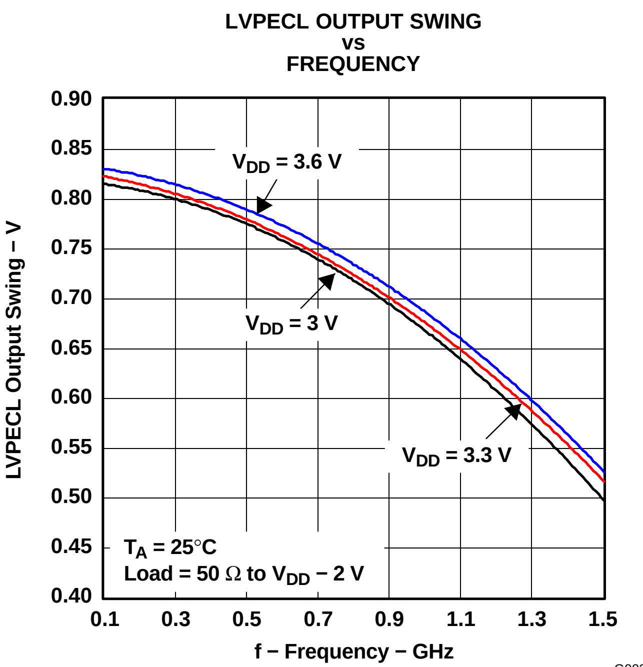


Figure 4.

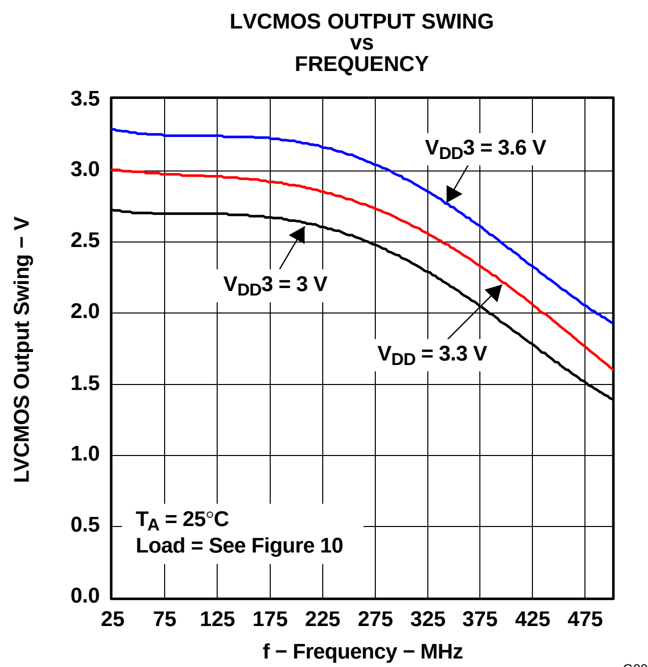


Figure 5.

SUPPLY CURRENT ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Supply current	Full load	All outputs enabled and terminated with 50 Ω to V_{DD} – 2 V on LVPECL outputs and 10 pF on LVCMOS output, f = 800 MHz for LVPECL outputs and 200 MHz for LVCMOS, V_{DD} = 3.3 V		160		mA
		No load	Outputs enabled, no output load, f = 800 MHz for LVPECL outputs and 200 MHz for LVCMOS, V_{DD} = 3.6 V			110	mA
	Supply current saving per LVPECL output stage disabled, no load		f = 800 MHz for LVPECL output, V_{DD} = 3.3 V		10		mA
I_{DDZ}	Supply current, 3-state		All outputs in the high-impedance state by control logic, f = 0 Hz, V_{DD} = 3.6 V			0.5	mA

SUPPLY CURRENT
vs
FREQUENCY

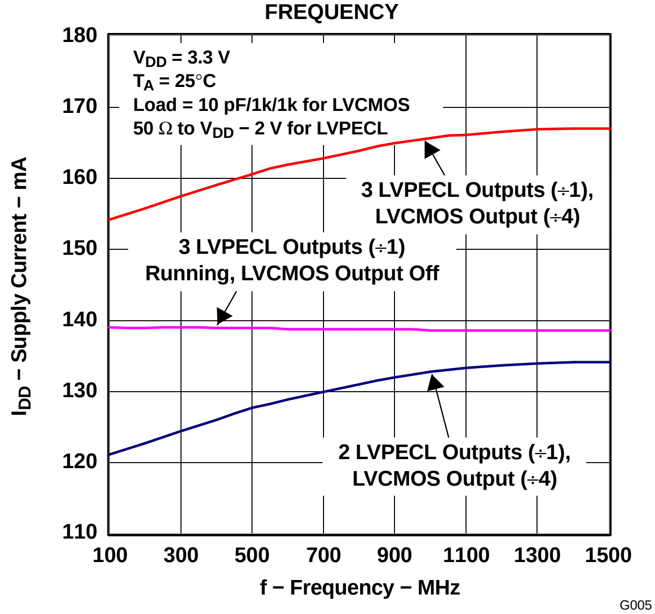


Figure 6.

PACKAGE THERMAL RESISTANCE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JA-1}$	QFN-24 package thermal resistance (1)	4-layer JEDEC test board (JESD51-7), airflow = 0 ft/min		106.6		°C/W
$R_{\theta JA-2}$	QFN-24 package thermal resistance with thermal vias in PCB (1)	4-layer JEDEC test board (JESD51-7) with four thermal vias of 22-mil diameter each, airflow = 0 ft/min		55.4		°C/W

(1) It is recommended to provide four thermal vias to connect the thermal pad of the package effectively with the PCB and ensure a good heat sink.

Example:

Calculation of the junction-lead temperature with a 4-layer JEDEC test board using four thermal vias:

$T_{Chassis}$ = 85°C (temperature of the chassis)

$P_{effective} = I_{max} \times V_{max}$ = 110 mA × 3.6 V = 396 mW (maximum power consumption inside the package)

$\theta T_{Junction} = R_{\theta JA-2} \times P_{effective}$ = 55.45°C/W × 396 mW = 21.96°C

$T_{Junction} = \theta T_{Junction} + T_{Chassis}$ = 21.96°C + 85°C = 107°C (the maximum junction temperature of $T_{die-max}$ = 125°C is not violated)

CONTROL INPUT CHARACTERISTICS

over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{su}	Setup time, S0, S1, S2, and EN terminals before clock IN		25			ns
t_h	Hold time, S0, S1, S2, and EN terminals after clock IN		0			ns
$t_{(disable)}$	Time between latching the EN low transition and when all outputs are disabled (how much time is required until the outputs turn off)			10		ns
$t_{(enable)}$	Time between latching the EN low-to-high transition and when outputs are enabled based on control settings (how much time passes before the outputs carry valid signals)			1		µs
Rpullup	Internal pullup resistor on S[2:0] and EN inputs		42	60	78	kΩ
$V_{IH(H)}$	Three-level input high, S0, S1, S2, and EN terminals (1)		0.9 V_{DD}			V
$V_{IM(M)}$	Three-level input MID, S0, S1, S2, and EN terminals		0.3 V_{DD}		0.7 V_{DD}	V
$V_{IL(L)}$	Three-level input low, S0, S1, S2, and EN terminals				0.1 V_{DD}	V
I_{IH}	Input current, S0, S1, S2, and EN terminals	$V_I = V_{DD}$			–5	µA
I_{IL}		V_I = GND	38		85	µA

(1) Leaving this terminal floating automatically pulls the logic level high to V_{DD} through an internal pullup resistor of 60 kΩ.

BIAS VOLTAGE VBB

over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBB	Output reference voltage	V_{DD} = 3 V–3.6 V, I_{BB} = –0.2 mA	V_{DD} – 1.4		V_{DD} – 1.2	V

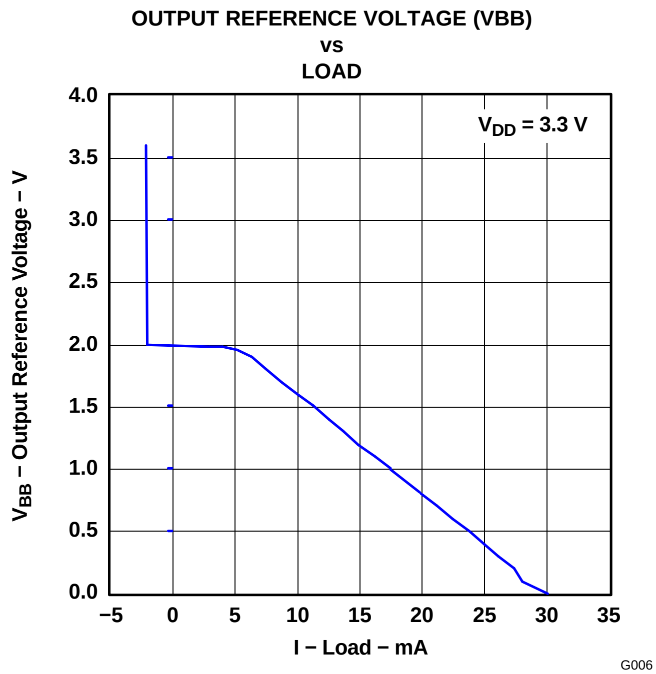
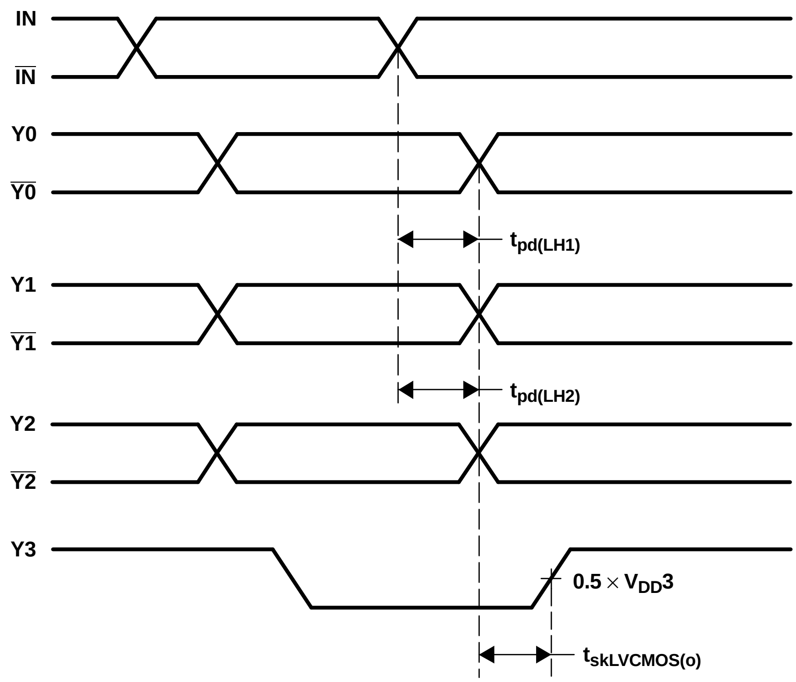

OUTPUT REFERENCE VOLTAGE (VBB)
vs
LOAD
V_{DD} = 3.3 V
V_{BB} – Output Reference Voltage – V
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
–5
0
5
10
15
20
25
30
35
I – Load – mA
G006

Figure 7.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Output skew, $t_{sk(o)}$, is calculated as the greater of:
- The difference between the fastest and the slowest $t_{pd(LH)n}$ (n = 0…2)
- The difference between the fastest and the slowest $t_{pd(HL)n}$ (n = 0…2)

B. Part-to-part skew, $t_{sk(pp)}$, is calculated as the greater of:
- The difference between the fastest and the slowest $t_{pd(LH)n}$ (n = 0…2 for LVPECL, n = 3 for LVCMOS) across multiple devices
- The difference between the fastest and the slowest $t_{pd(HL)n}$ (n = 0…2 for LVPECL, n = 3 for LVCMOS) across multiple devices

C. Pulse skew, $t_{sk(p)}$, is calculated as the magnitude of the absolute time difference between the high-to-low ($t_{pd(HL}$) and the low-to-high ($t_{pd(LH)}$) propagation delays when a single switching input causes one or more outputs to switch, $t_{sk(p)} = | t_{pd(HL)} - t_{pd(LH)} |$. Pulse skew is sometimes referred to as *pulse width distortion or duty cycle skew.*

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Figure 8. Waveforms for Calculation of $t_{sk(o)}$ and $t_{sk(pp)}$

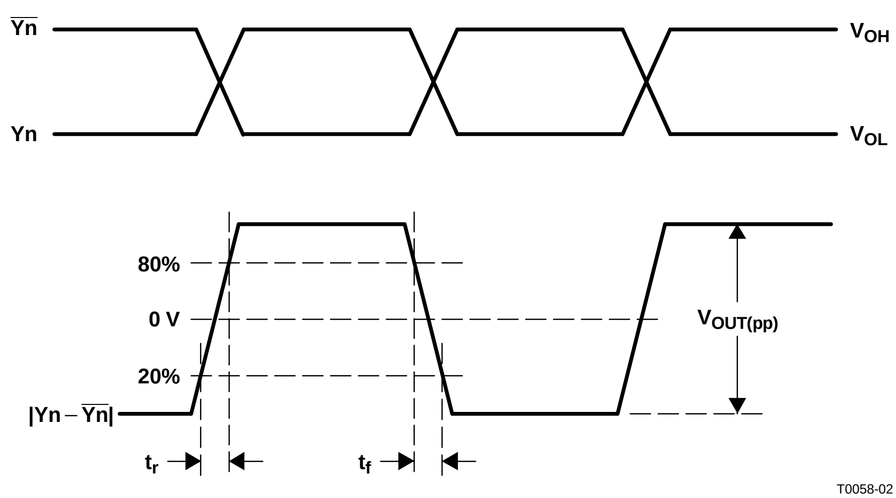


Figure 9. LVPECL Differential Output Voltage and Rise/Fall Time

PARAMETER MEASUREMENT INFORMATION (continued)

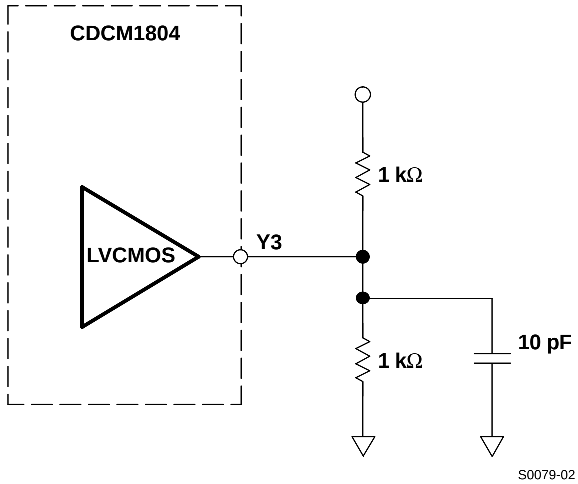


Figure 10. LVCMOS Output Loading During Device Test

PCB DESIGN FOR THERMAL FUNCTIONALITY

It is recommended to take special care of the PCB design for good thermal flow from the QFN-24 terminal package to the PCB.

Due to the three LVPECL outputs, the current consumption of the CDCM1804 is fixed.

JEDEC JESD51-7 specifies thermal conductivity for standard PCB boards.

Modeling the CDCM1804 with a standard 4-layer JEDEC board results in a 67.22°C maximum temperature with $R_{\theta JA}$ of 106.62°C/W for 25°C ambient temperature.

When deploying four thermal vias (one per quadrant), the thermal flow improves significantly, yielding 46.94°C maximum temperature with $R_{\theta JA}$ of 55.4°C/W for 25°C ambient temperature.

To ensure sufficient thermal flow, it is recommended to design with four thermal vias in applications enabling all four outputs at once.

PARAMETER MEASUREMENT INFORMATION (continued)

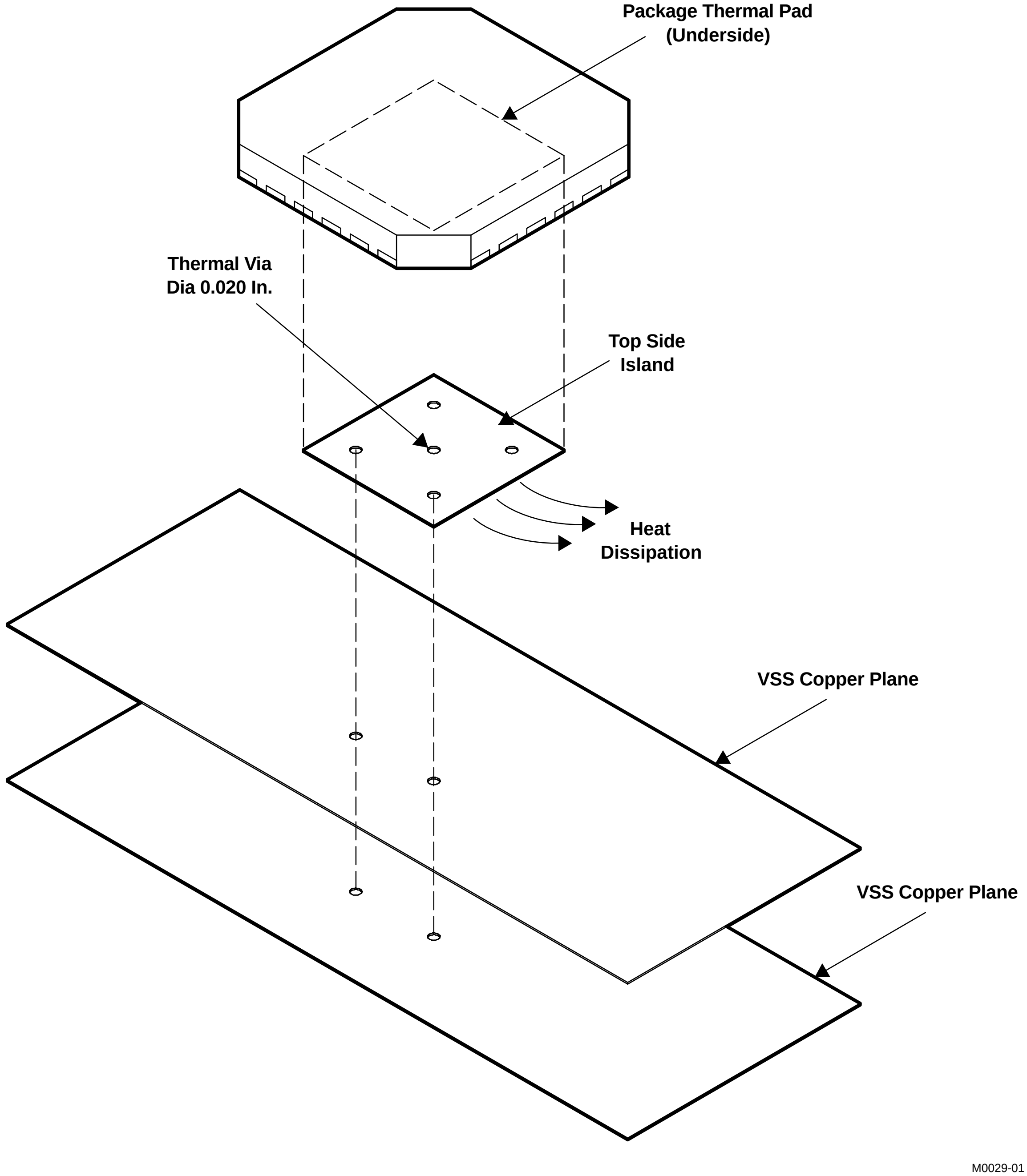


Figure 11. Recommended Thermal Via Placement

See the application reports *Quad Flatpack No-Lead Logic Packages* (SCBA017) and *QFN/SON PCB Attachment* (SLUA271) for further package-related information.

APPLICATION INFORMATION

LVPECL RECEIVER INPUT TERMINATION

The input of the CDCM1804 has a high impedance and comes with a large common-mode voltage range.

For optimized noise performance, it is recommended to properly terminate the PCB trace (transmission line). If a differential signal drives the CDCM1804, then a 100-Ω termination resistor is recommended to be placed as close as possible across the input terminals. An even better approach is to install 2 × 50 Ω, with the center tap connected to a capacitor (C) to terminate odd-mode noise and make up for transmission-line mismatches. The VBB output can also be connected to the center tap to bias the input signal to (V_{DD} – 1.3 V) (see Figure 12).

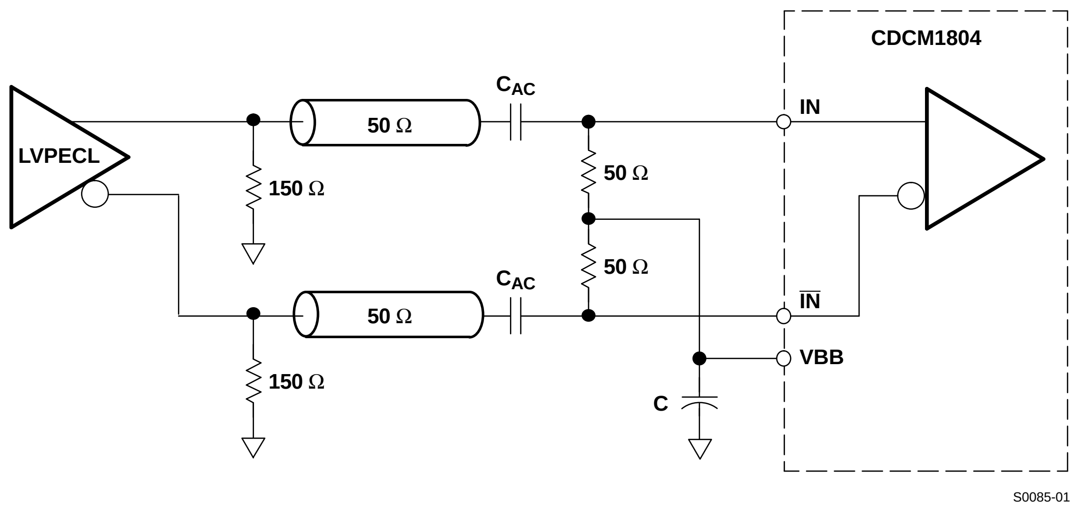


Figure 12. Recommended AC-Coupling LVPECL Receiver Input Termination

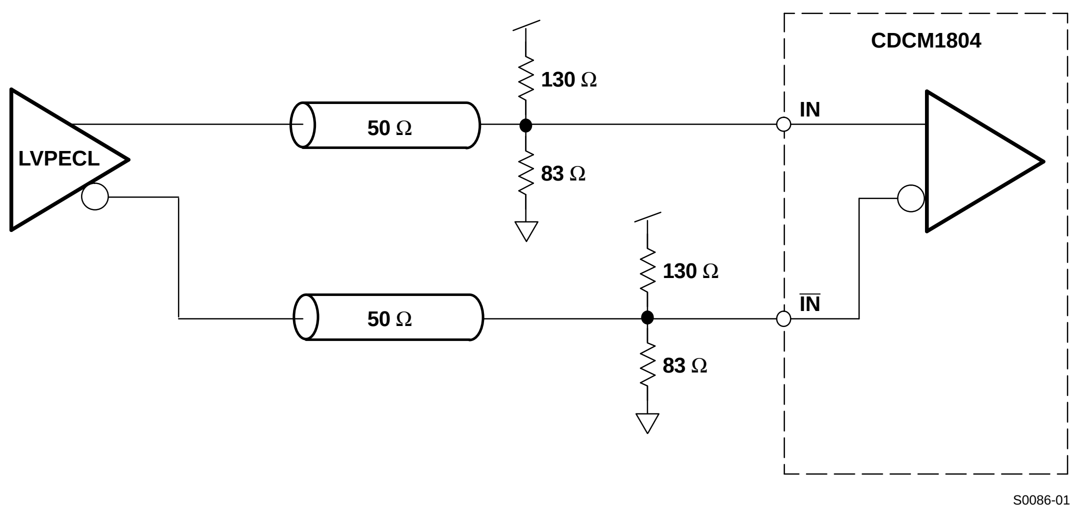
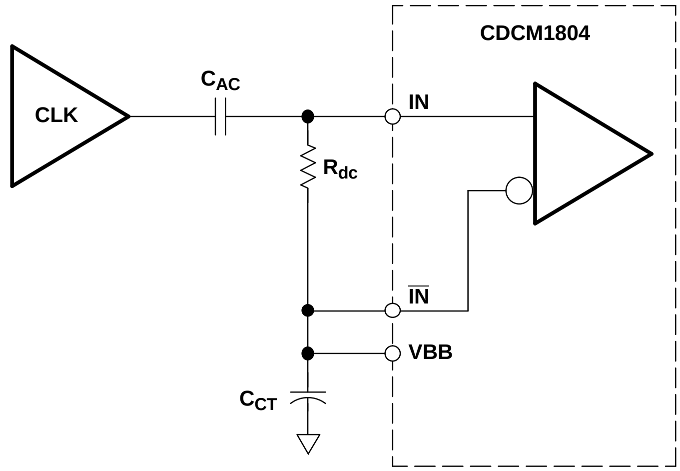


Figure 13. Recommended DC-Coupling LVPECL Receiver Input Termination

The CDCM1804 can also be driven by single-ended signals. Typically, the input signal becomes connected to one input, while the complementary input must be properly biased to the center voltage of the incoming input signal. For LVCMOS signals, this would be $V_{CC}/2$, realized by a simple voltage divider (e.g., two 10-kΩ resistors). The best option (especially if the dc offset of the input signal might vary) is to ac-couple the input signal and then rebias the signal using the VBB reference output. See Figure 14.

APPLICATION INFORMATION (continued)



NOTE: C_{AC} − AC-coupling capacitor (e.g., 10 nF)
C_{CT} − Capacitor keeps voltage at $\overline{IN}$ constant (e.g., 10 nF)
R_{dc} − Load and correct duty cycle (e.g., 50 Ω)
VBB − Bias voltage output

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Figure 14. Typical Application Setting for Single-Ended Input Signals Driving the CDCM1804

DEVICE BEHAVIOR DURING RESET AND CONTROL-TERMINAL SWITCHING

Output Behavior From Enabling the Device (EN = 0 → 1)

In disable mode (EN = 0), all output drivers are switched in high-Z mode. The S[2:0] control inputs are also switched off. In the same mode, all flip-flops are reset. The typical current consumption is below 500 µA.

When the device is enabled again, it takes typically 1 µs for the settling of the reference voltage and currents. During this time, the outputs Y[2:0] and $\overline{Y[2:0]}$ drive a high signal. Y3 is unknown (could be high or low). After the settle time, the outputs go into the low state. Due to the synchronization of each output driver signal with the input clock, the state of the waveforms after enabling the device is as shown in Figure 15. The inverting input and output signal are not included. The Y:/1 waveform is the undivided output driver state.

APPLICATION INFORMATION (continued)

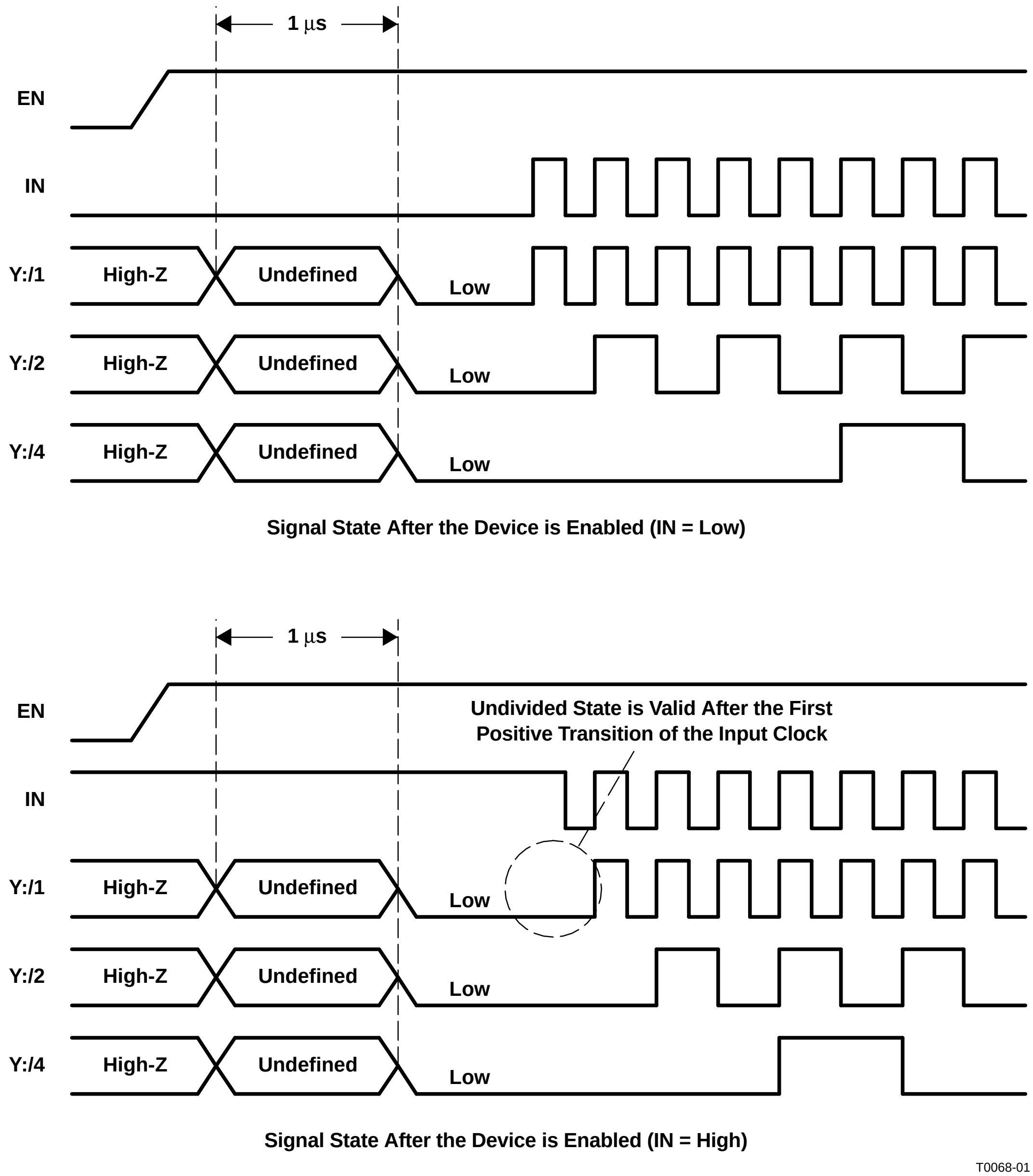

Figure 15. Waveforms

Enabling a Single Output Stage

If a single output stage becomes enabled:

- Y[2:0] is either low or high (undefined).
- $\overline{\text{Y[2:0]}}$ is the inverted signal of Y[2:0].

With the first positive clock transition, the undivided output becomes the input clock state. The divided output states are equal to the actual internal divider. The internal divider is not reset while enabling single-output drivers.

APPLICATION INFORMATION (continued)

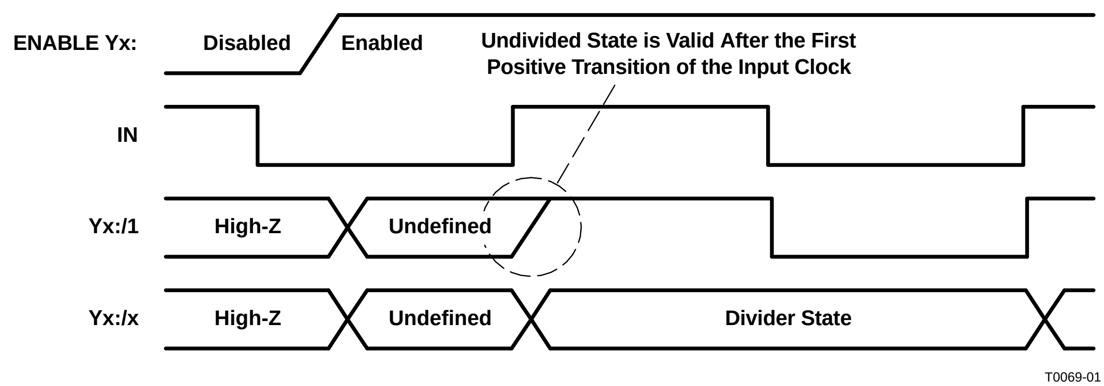

Figure 16. Signal State After an Output Driver Becomes Enabled While IN = 0

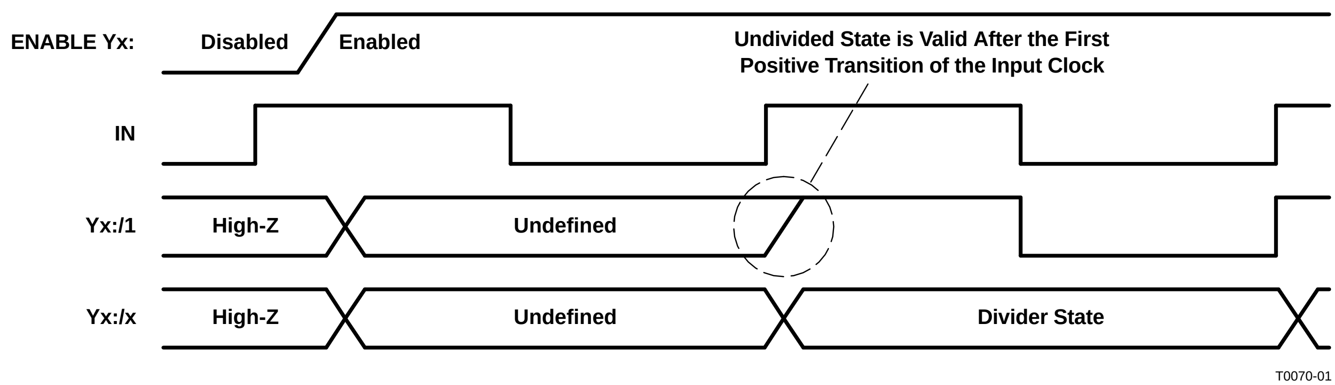

Figure 17. Signal State After an Output Driver Becomes Enabled While IN = 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCM1804RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCM 1804	Samples
CDCM1804RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCM 1804	Samples
SN0305042RTHR	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCM 1804	Samples
SN0305042RTHT	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CDCM 1804	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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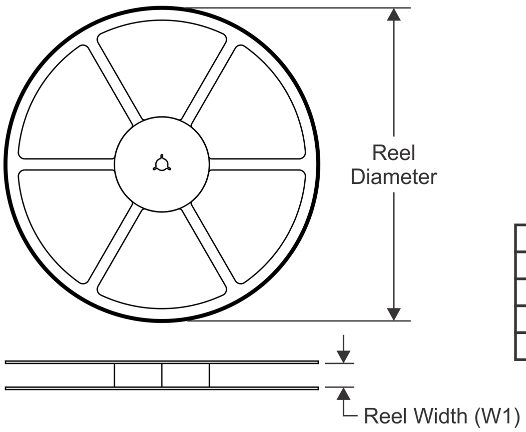
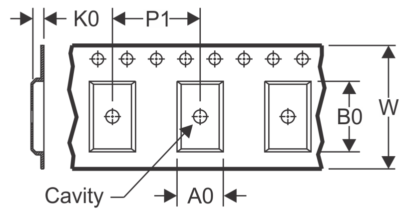
TAPE AND REEL INFORMATION

REEL DIMENSIONS

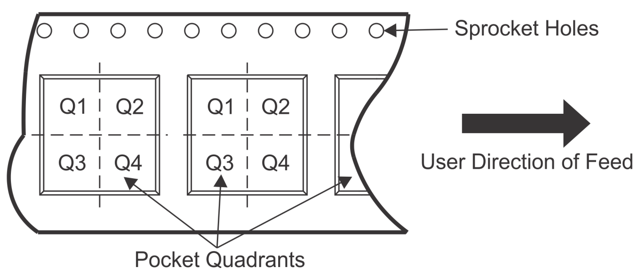


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

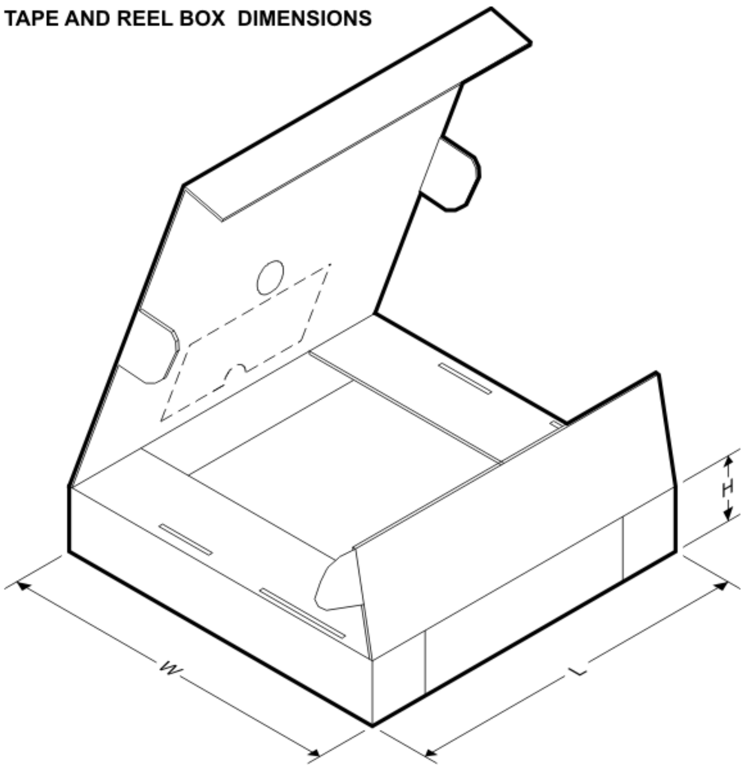
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

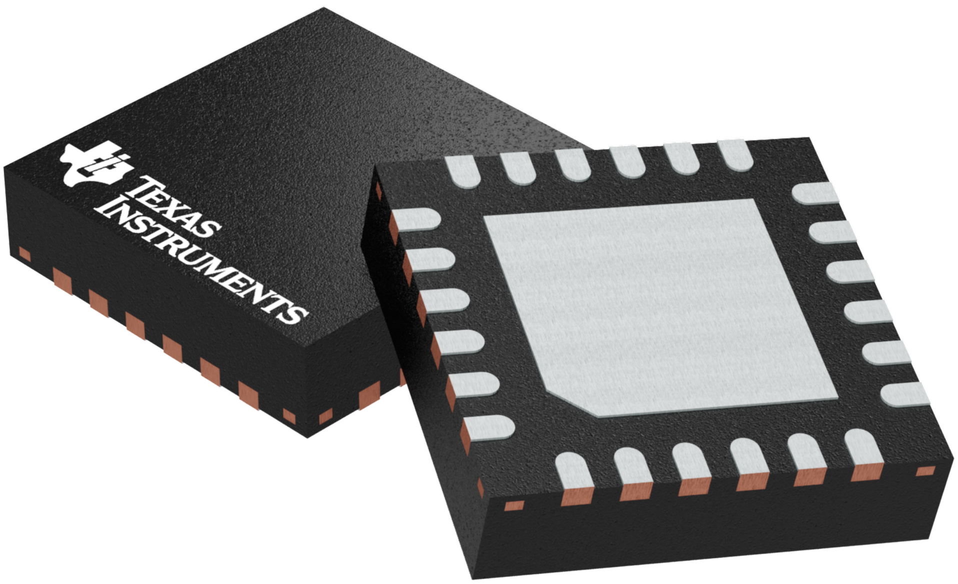
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCM1804RGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
CDCM1804RGET	VQFN	RGE	24	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



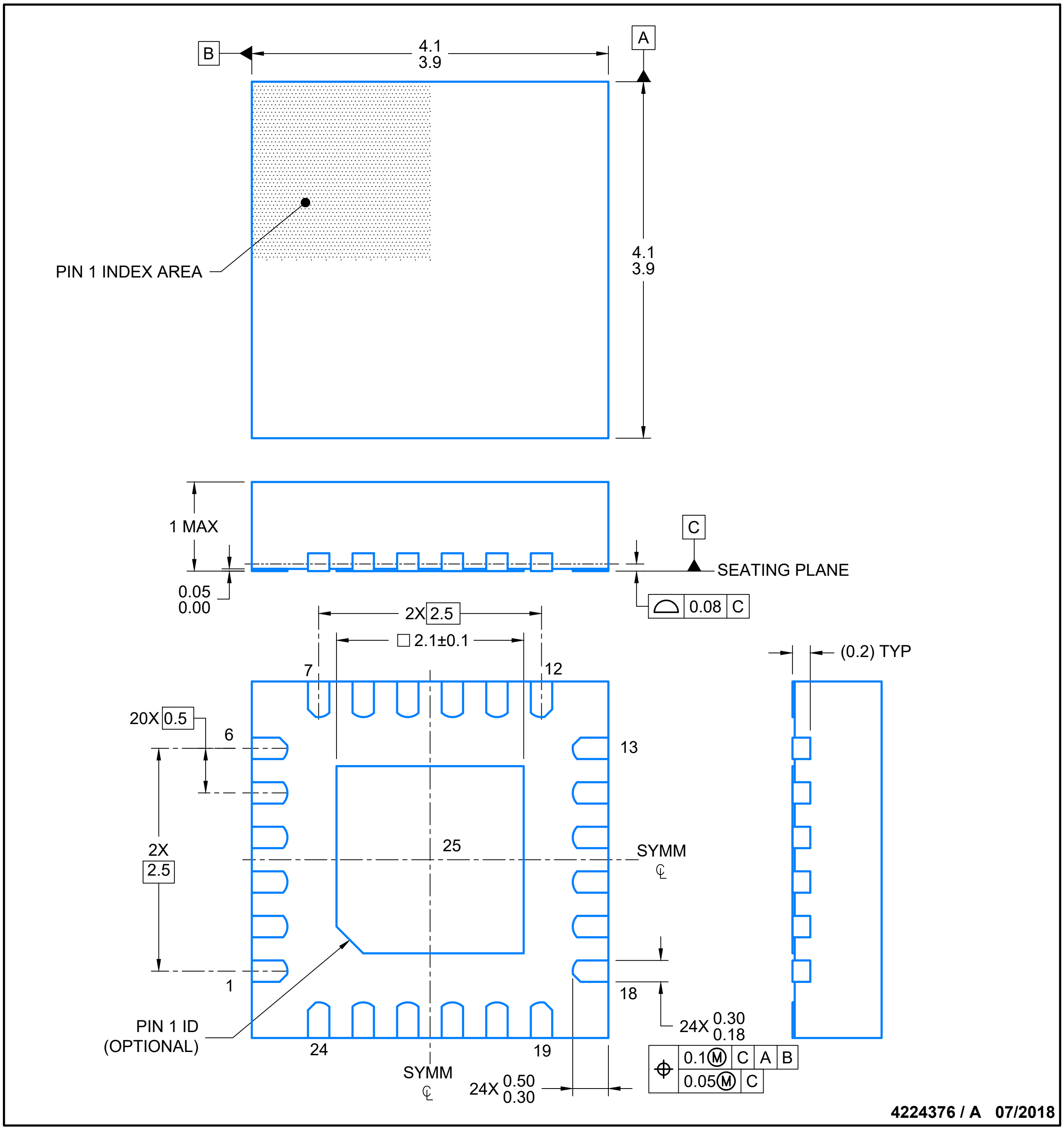
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCM1804RGER	VQFN	RGE	24	3000	350.0	350.0	43.0
CDCM1804RGET	VQFN	RGE	24	250	210.0	185.0	35.0



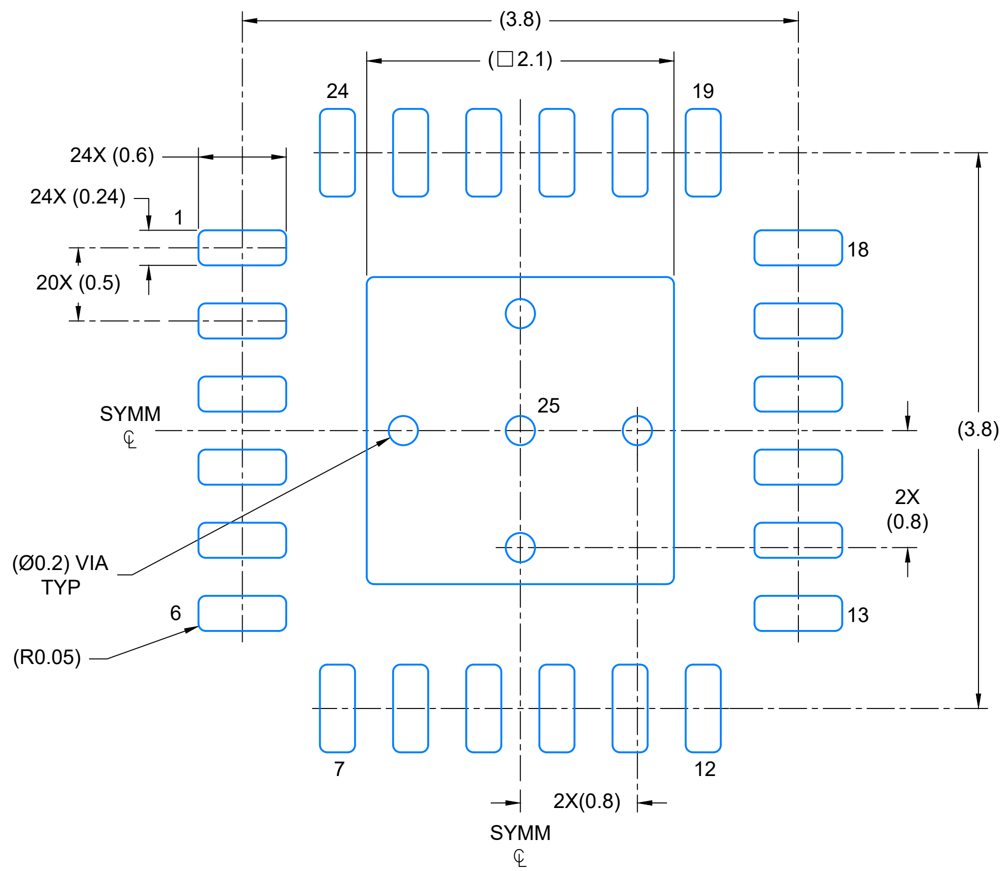
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

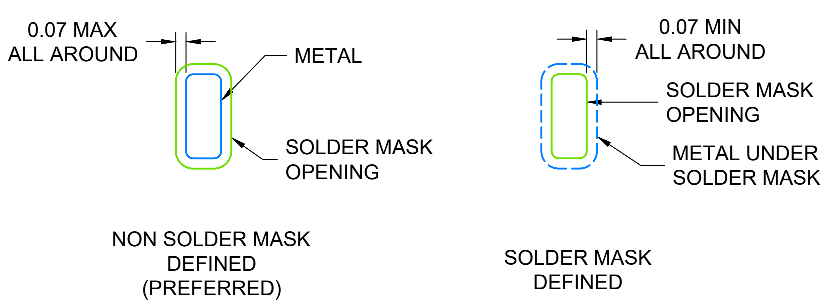


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X



SOLDER MASK DETAILS

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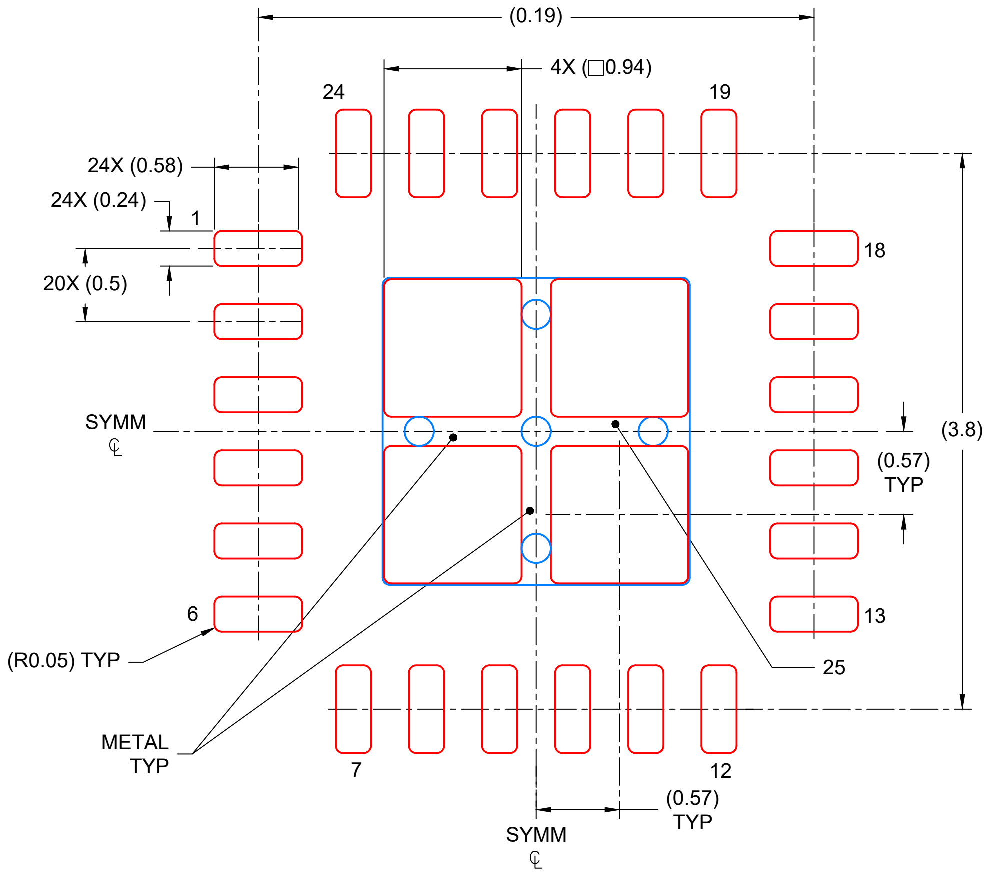
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 20X

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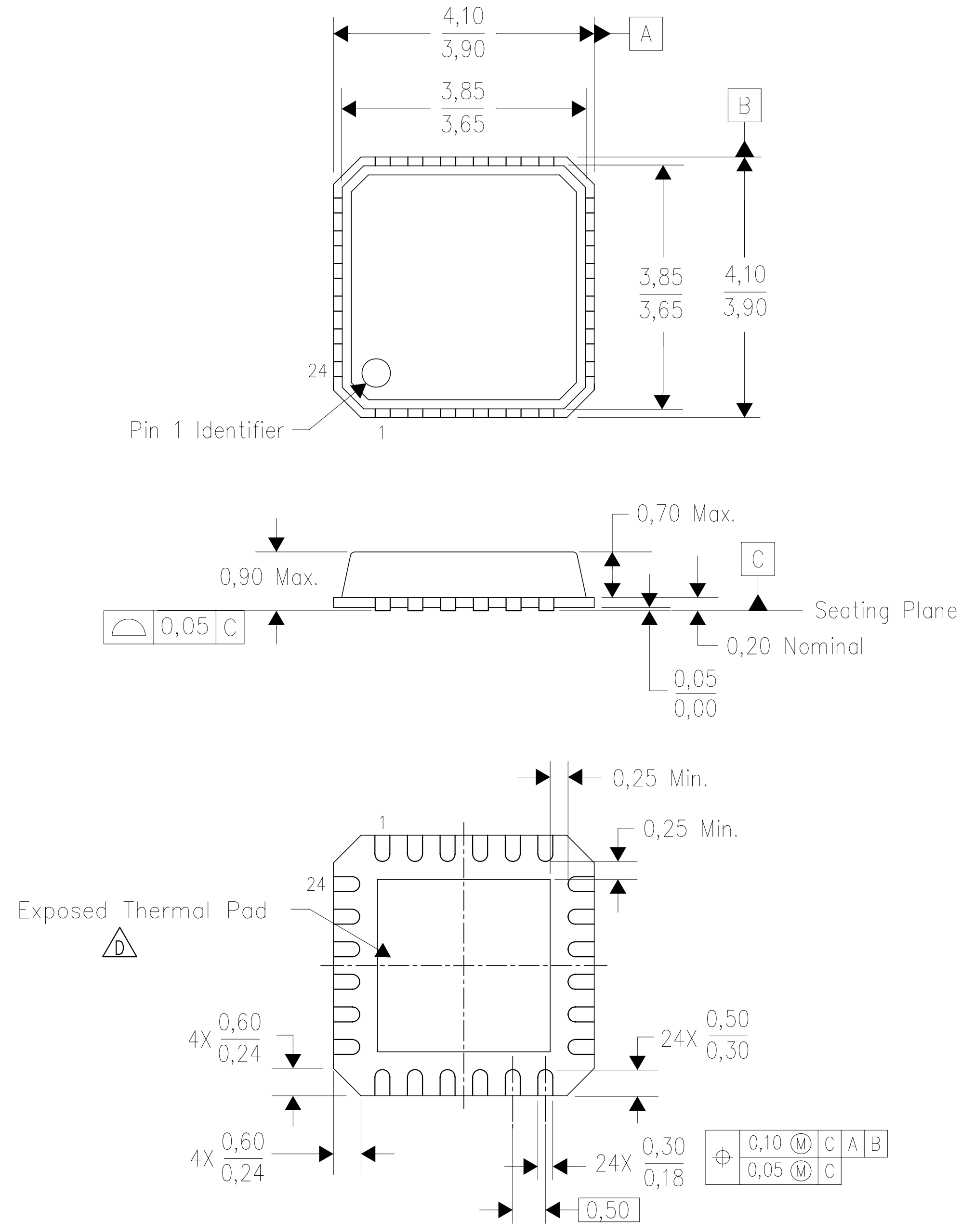
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

RTH (S-PVQFN-N24) PLASTIC QUAD FLATPACK



4205481/C 02/11

NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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