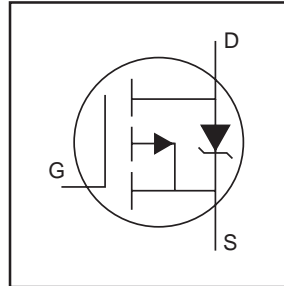


IRFR/U5305

HEXFET® Power MOSFET

- Ultra Low On-Resistance
- Surface Mount (IRFR5305)
- Straight Lead (IRFU5305)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated

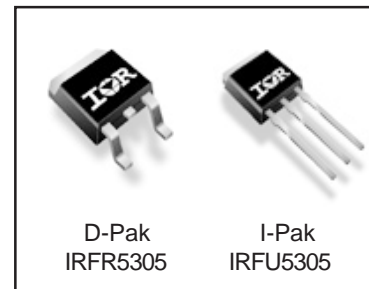


$V_{DSS} = -55V$
$R_{DS(on)} = 0.065\Omega$
$I_D = -31A$

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET® Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-31	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-22	
I_{DM}	Pulsed Drain Current ①⑥	-110	
$P_D @ T_C = 25^\circ C$	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②⑥	280	mJ
I_{AR}	Avalanche Current ①⑥	-16	A
E_{AR}	Repetitive Avalanche Energy ①	11	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑥	-5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
$R_{\theta JA}$	Junction-to-Ambient**	—	110	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
	$V_{(BR)DSS}$	-55	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
	$\Delta V_{(BR)DSS}/\Delta T_J$	—	-0.034	—	V/°C	Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
	$R_{DS(on)}$	—	—	0.065	Ω	$V_{GS} = -10V, I_D = -16A$ ④
	$V_{GS(th)}$	-2.0	—	-4.0	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
	g_{fs}	8.0	—	—	S	$V_{DS} = -25V, I_D = -16A$ ⑥
	I_{DSS}	—	—	-25	μA	$V_{DS} = -55V, V_{GS} = 0V$
		—	—	-250		$V_{DS} = -44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
	I_{GSS}	—	—	100	nA	$V_{GS} = 20V$
		—	—	-100		$V_{GS} = -20V$
	Q_g	—	—	63	nC	$I_D = -16A$
	Q_{gs}	—	—	13		$V_{DS} = -44V$
	Q_{gd}	—	—	29		$V_{GS} = -10V$, See Fig. 6 and 13 ④⑥
	$t_{d(on)}$	—	14	—	ns	$V_{DD} = -28V$ $I_D = -16A$ $R_G = 6.8\Omega$ $R_D = 1.6\Omega$, See Fig. 10 ④⑥
	t_r	—	66	—		
	$t_{d(off)}$	—	39	—		
	t_f	—	63	—		
	L_D	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact ⑤
	L_S	—	7.5	—		
	C_{iss}	—	1200	—	pF	$V_{GS} = 0V$ $V_{DS} = -25V$ $f = 1.0\text{MHz}$, See Fig. 5 ⑥
	C_{oss}	—	520	—		
	C_{rss}	—	250	—		

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
	I_S	—	—	-31	A	MOSFET symbol showing the integral reverse p-n junction diode.
	I_{SM}	—	—	-110		
	V_{SD}	—	—	-1.3	V	$T_J = 25^\circ\text{C}, I_S = -16A, V_{GS} = 0V$ ④
	t_{rr}	—	71	110	ns	$T_J = 25^\circ\text{C}, I_F = -16A$
	Q_{rr}	—	170	250	nC	$di/dt = -100A/\mu s$ ④⑥

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② $V_{DD} = -25V$, starting $T_J = 25^\circ\text{C}$, $L = 2.1\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = -16A$. (See Figure 12)
- ③ $I_{SD} \leq -16A$, $di/dt \leq -280A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

⑤ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact.

⑥ Uses IRF5305 data and test conditions.

* When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

** Uses typical socket mount.

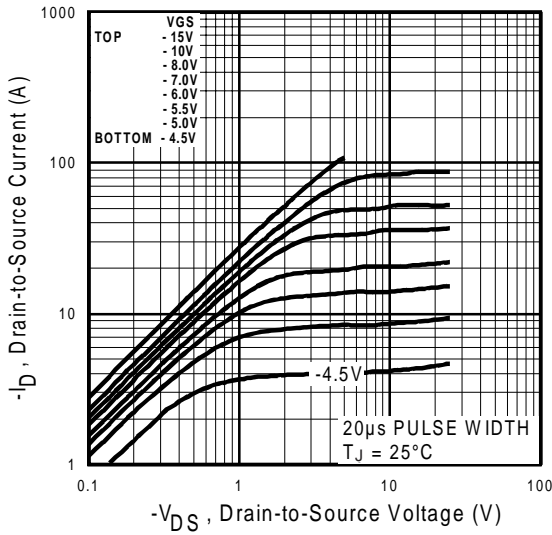


Fig 1. Typical Output Characteristics

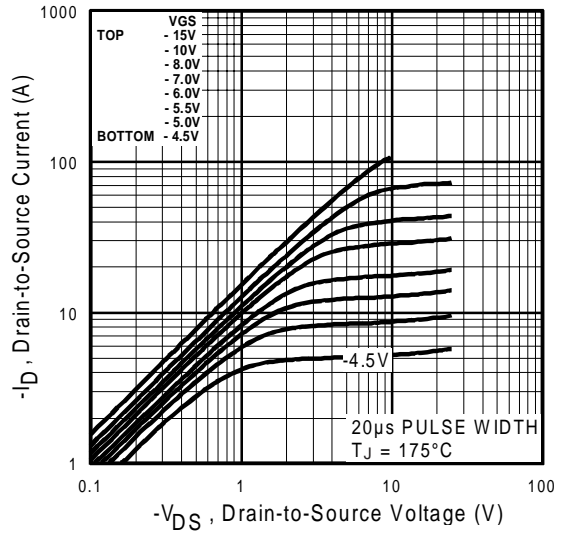


Fig 2. Typical Output Characteristics

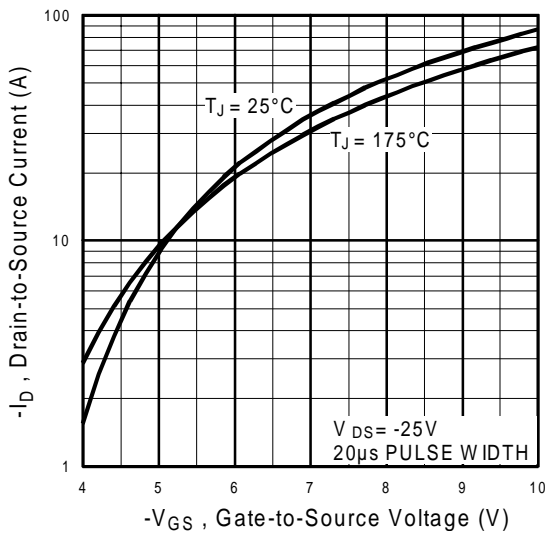


Fig 3. Typical Transfer Characteristics

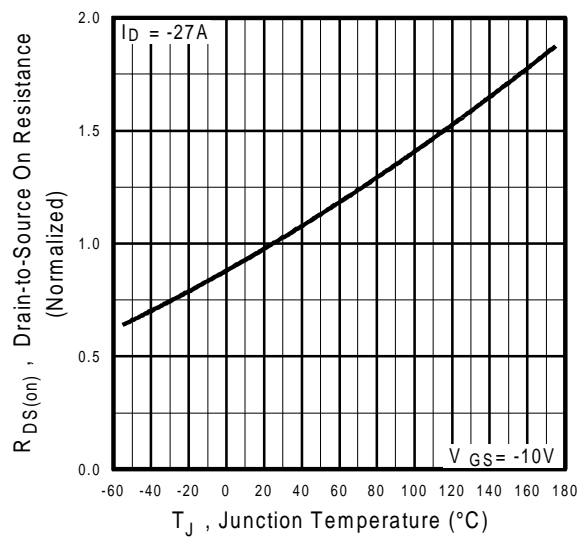


Fig 4. Normalized On-Resistance Vs. Temperature

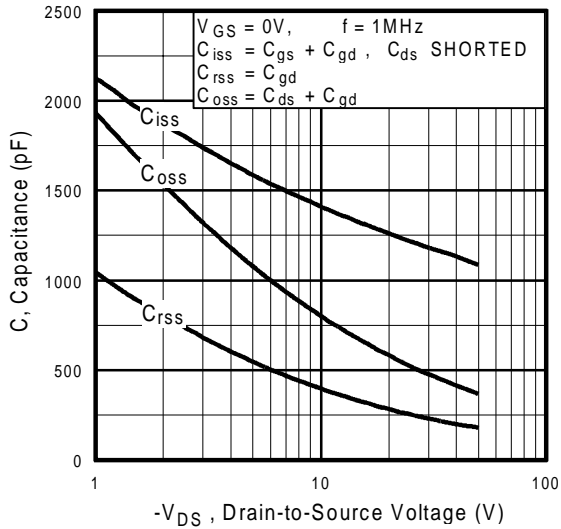


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

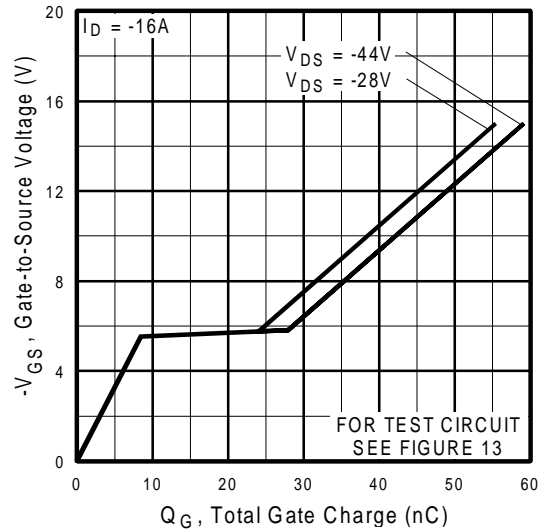


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

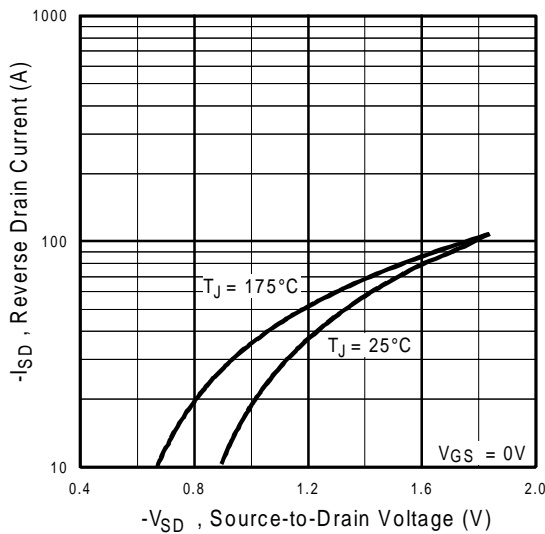


Fig 7. Typical Source-Drain Diode Forward Voltage

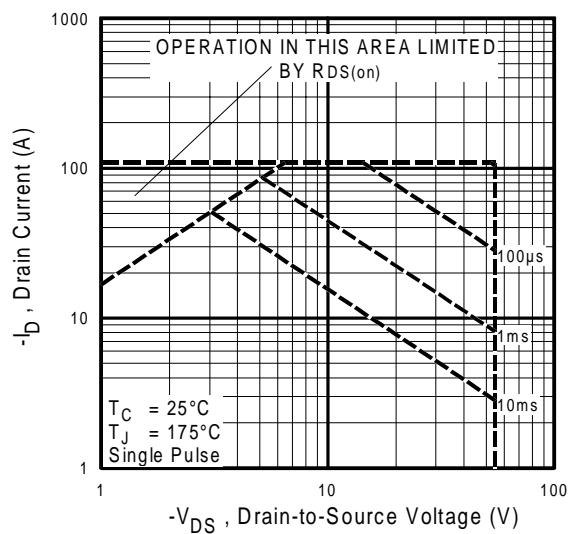


Fig 8. Maximum Safe Operating Area

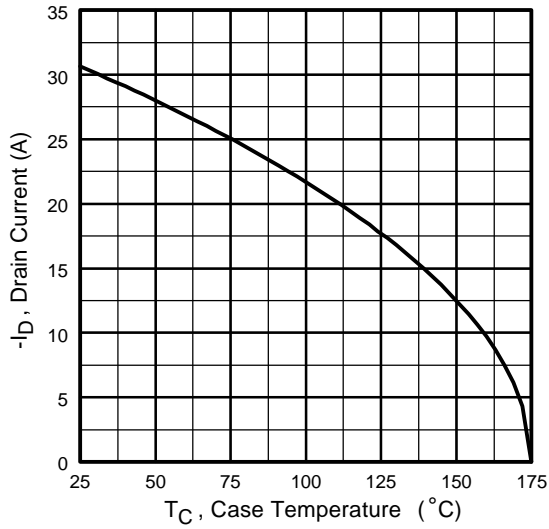


Fig 9. Maximum Drain Current Vs. Case Temperature

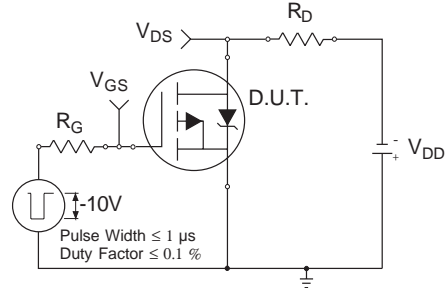


Fig 10a. Switching Time Test Circuit

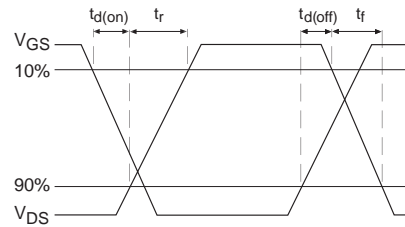


Fig 10b. Switching Time Waveforms

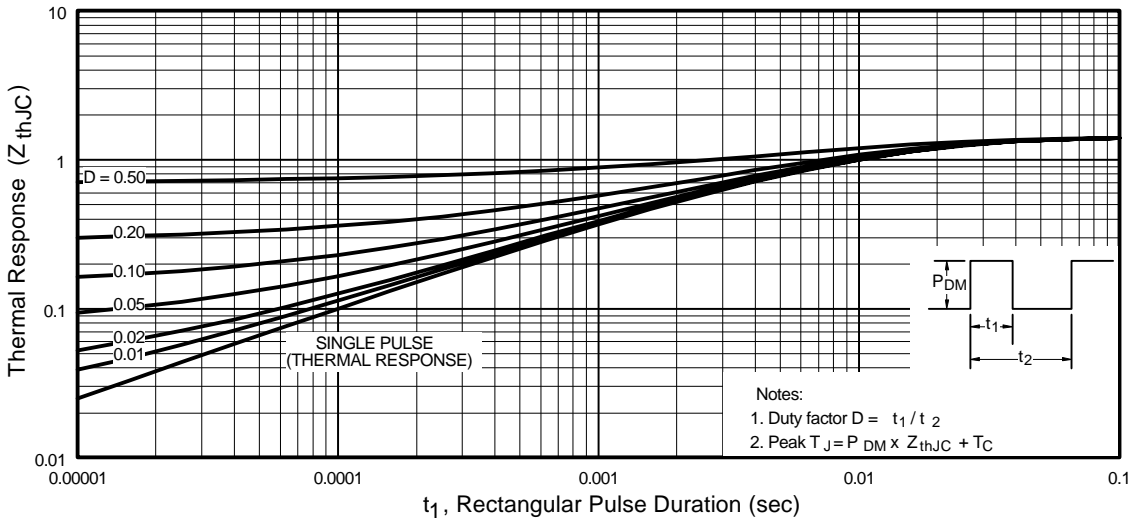


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

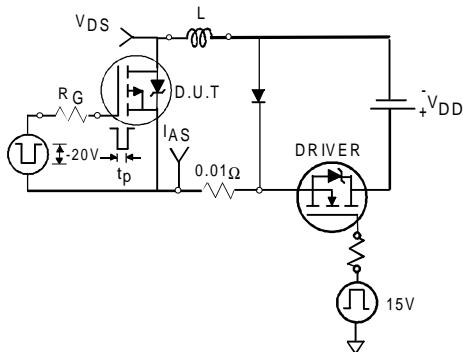


Fig 12a. Unclamped Inductive Test Circuit

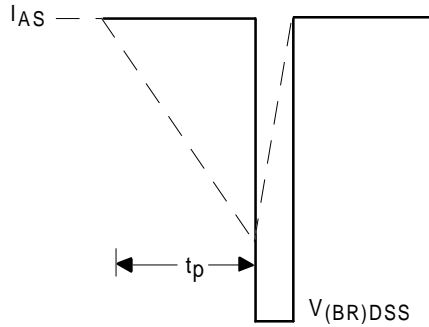


Fig 12b. Unclamped Inductive Waveforms



Fig 13a. Basic Gate Charge Waveform

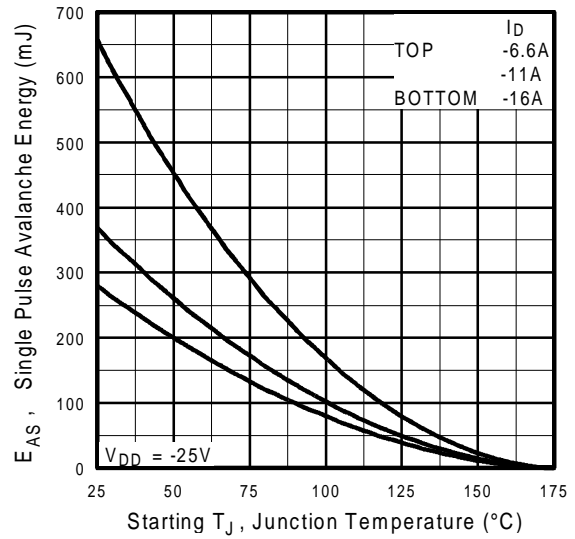
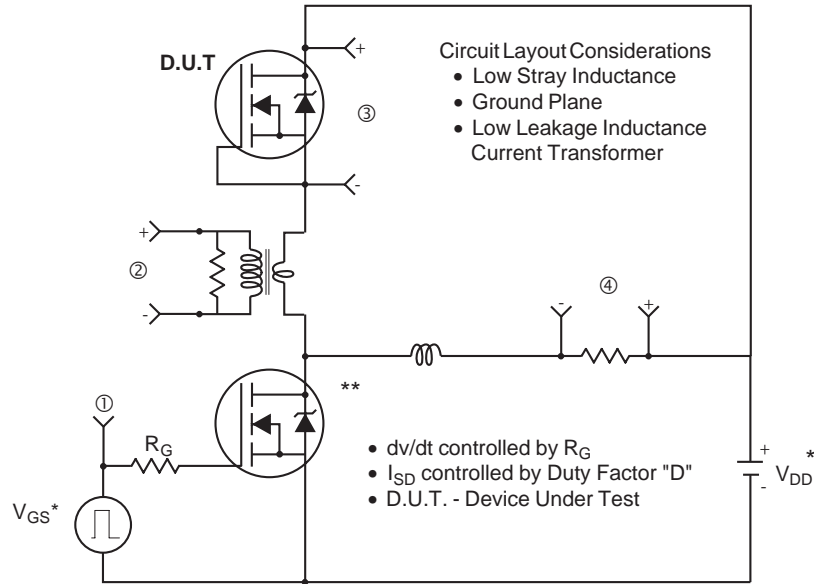


Fig 12c. Maximum Avalanche Energy Vs. Drain Current



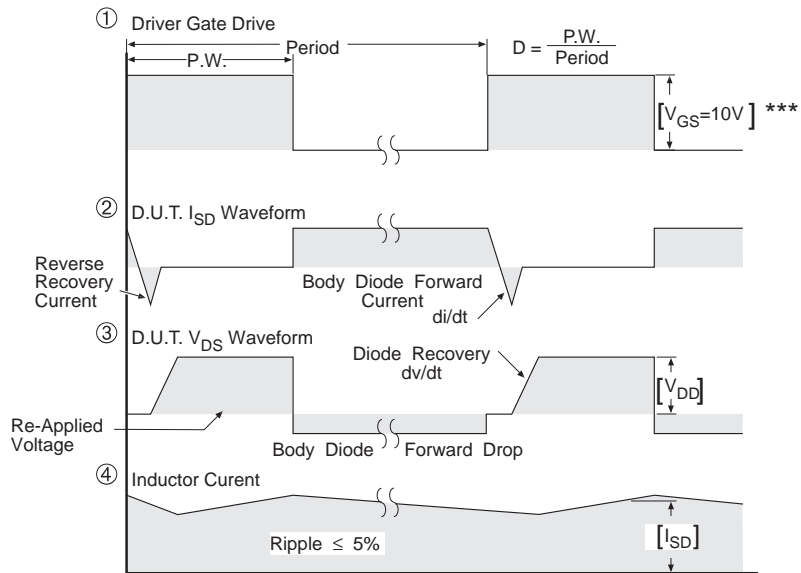
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



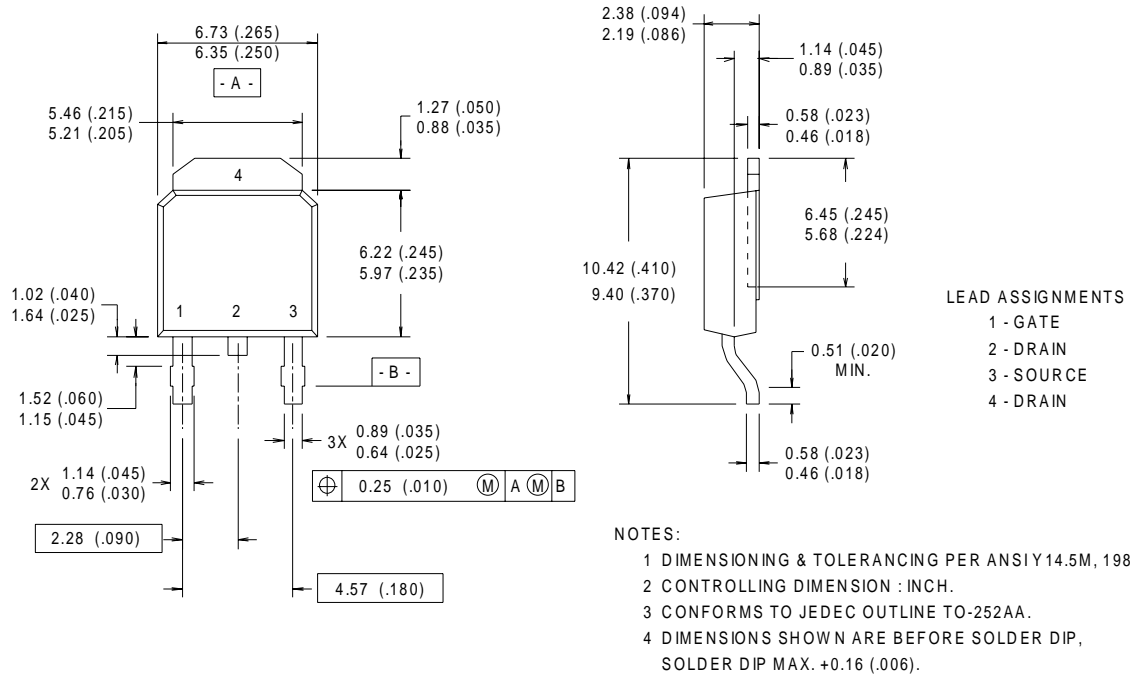
*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

IRFR/U5305

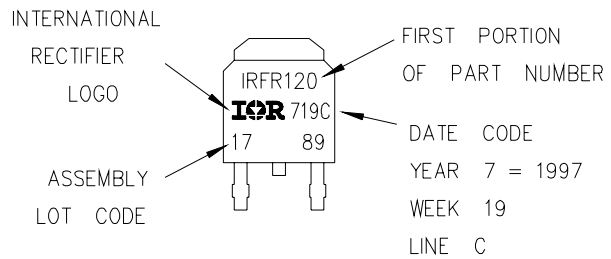
D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



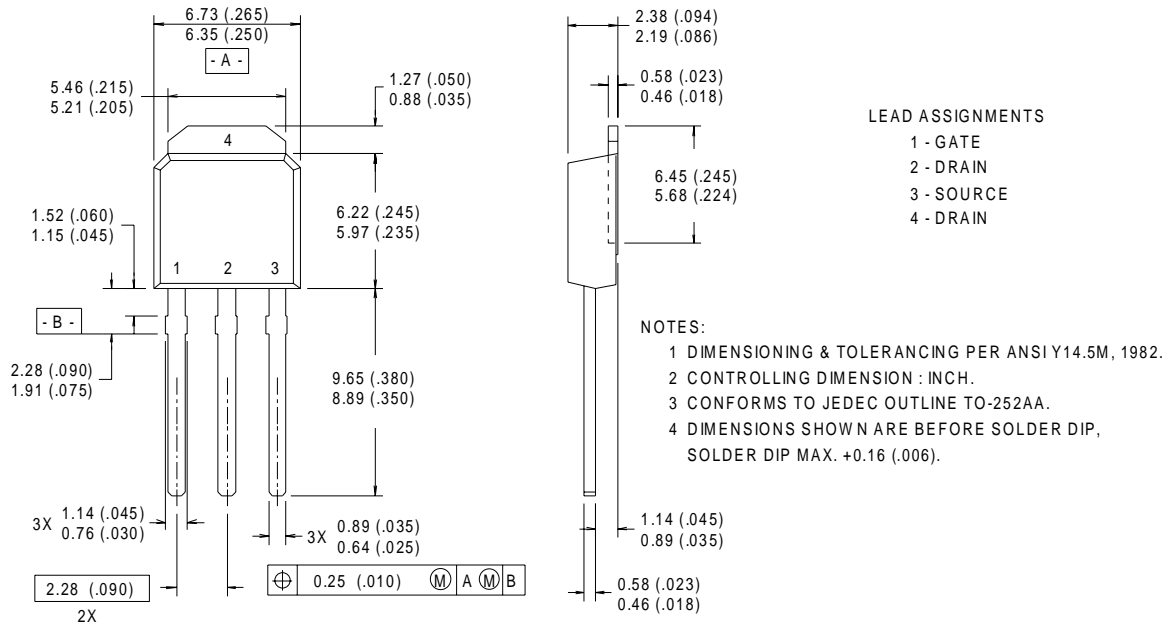
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



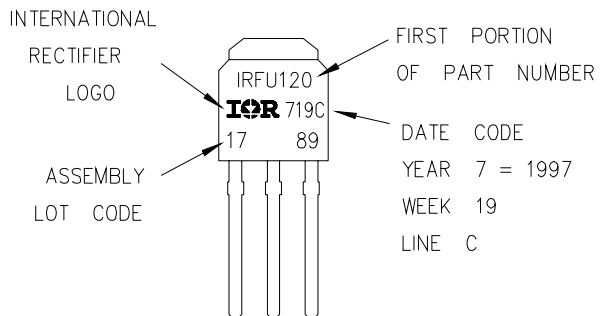
I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



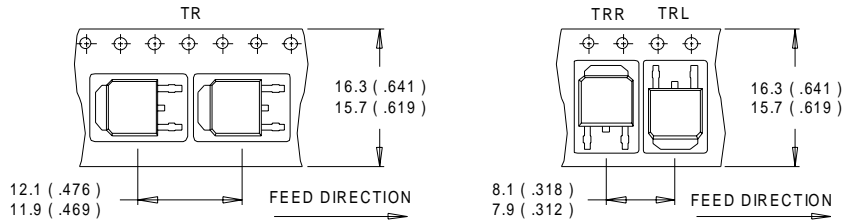
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



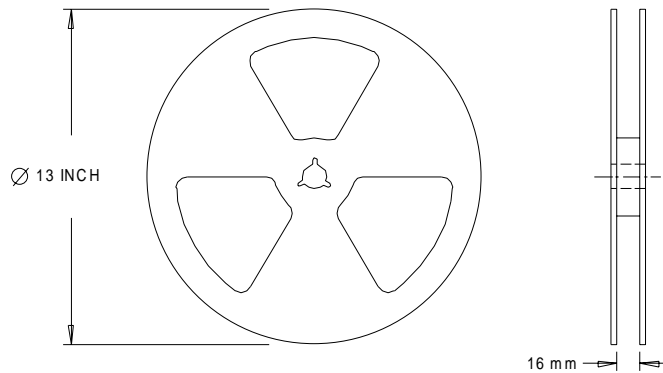
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>