CS2842A, CS3842A, CS2843A, CS3843A

Off-Line Current Mode PWM Control Circuit with Undervoltage Lockout

The CS284XA, CS384XA provides all the necessary features to implement off−line fixed frequency current−mode control with a minimum number of external components.

The CS384XA family incorporates a new precision temperature−controlled oscillator with an internally trimmed discharge current to minimize variations in frequency. A precision duty−cycle clamp eliminates the need for an external oscillator when a 50% duty−cycle is used. Duty−cycles greater than 50% are also possible. On board logic ensures that V_{REF} is stabilized before the output stage is enabled. Ion implant resistors provide tighter control of undervoltage lockout.

Other features include low startup current, pulse−by−pulse current limiting, and a high−current totem pole output for driving capacitive loads, such as the gate of power MOSFET. The output is LOW in the off state, consistent with N−channel devices.

The CS384XA series of current−mode control ICs are available in 8 and14 lead packages for surface mount (SO) applications as well as 8 lead PDIP packages.

Features

- Optimized for Off−line Control
- Internally Trimmed Temperature Compensated Oscillator
- Maximum Duty−Cycle Clamp
- V_{REF} Stabilized Before Output Stage is Enabled
- Low Startup Current
- Pulse−By−Pulse Current Limiting
- Improved Undervoltage Lockout
- Double Pulse Suppression
- 1.0% Trimmed Bandgap Reference
- High Current Totem Pole Output

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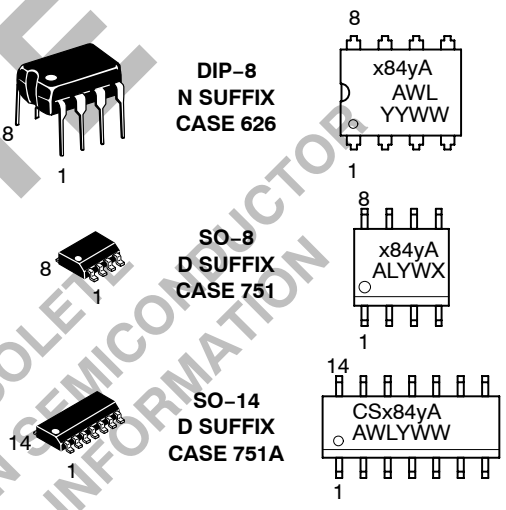
MARKING DIAGRAM



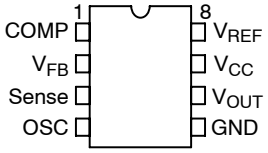
x	= 2 or 3
y	= 2 or 3
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week

ORDERING INFORMATION

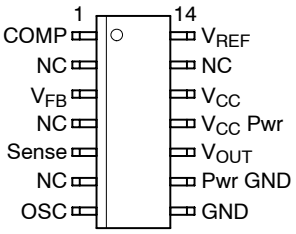
See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

PIN CONNECTIONS

DIP−8 & SO−8



SO−14



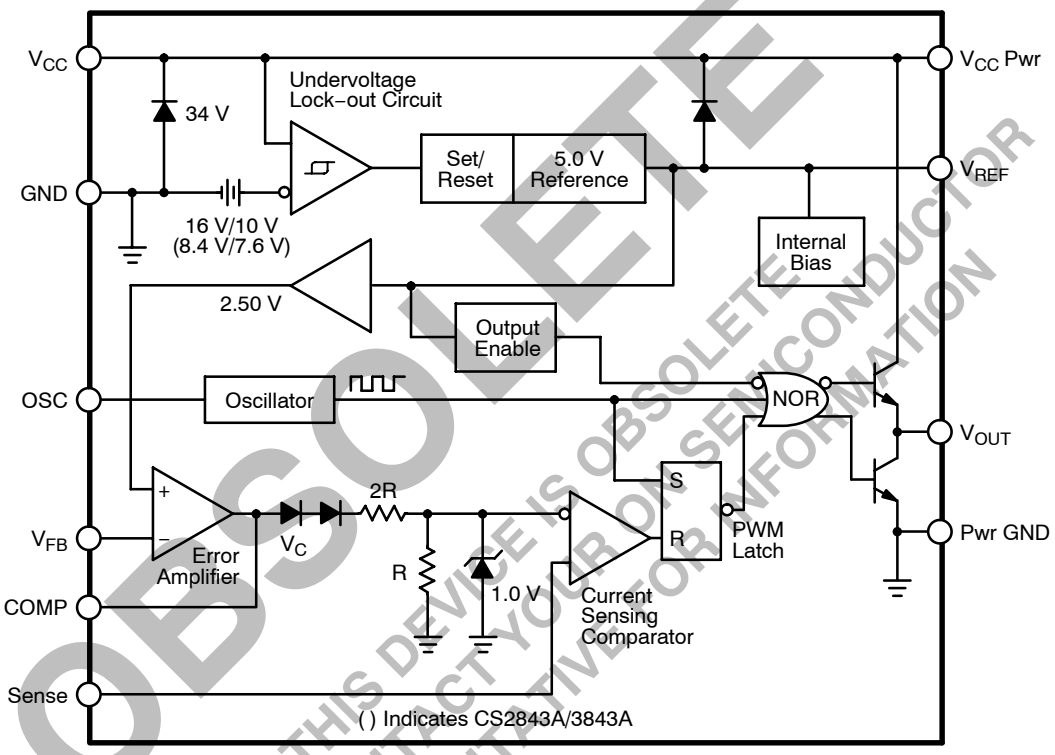


Figure 1. Block Diagram

MAXIMUM RATINGS*

Rating	Value	Unit
Supply Voltage (I_{CC} < 30 mA)	Self Limiting	–
Supply Voltage (Low Impedance Source)	30	V
Output Current	±1.0	A
Output Energy (Capacitive Load)	5.0	μJ
Analog Inputs (V_{FB}, Sense)	−0.3 to + 5.5	V
Error Amp Output Sink Current	10	mA
Package Thermal Resistance, PDIP−8 Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	 52 100	 °CW °CW
Package Thermal Resistance, SO−8 Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	 45 165	 °CW °CW
Package Thermal Resistance, SO−14 Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	 30 125	 °CW °CW
Lead Temperature Soldering: Wave Solder (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2)	260 peak 230 peak	°C °C

1. 10 second maximum.
2. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (−25° ≤ T_A ≤ 85° for CS2842A/CS2843A, 0° ≤ T_A ≤ 70° for CS3842A/CS3843A. V_{CC} = 15 V*; R_T = 680 Ω, C_T = 0.022 μF for triangular mode, R_T = 10 kΩ, C_T = 3.3 nF for sawtooth mode (see Figure 7); unless otherwise stated.)

Characteristic	Test Conditions	CS2842A/CS2843A Min	CS2842A/CS2843A Typ	CS2842A/CS2843A Max	CS3842A/CS3843A Min	CS3842A/CS3843A Typ	CS3842A/CS3843A Max	Unit
Reference Section								
Output Voltage	T_J = 25°C, I_{OUT} = 1.0 mA	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	12 ≤ V_{IN} ≤ 25 V	–	6.0	20	–	6.0	20	mV
Load Regulation	1.0 ≤ I_{OUT} ≤ 20 mA	–	6.0	25	–	6.0	25	mV
Temperature Stability	Note 3.	–	0.2	0.4	–	0.2	0.4	mV/°C
Total Output Variation	Line, Load, Temperature (Note 3.)	4.90	–	5.10	4.82	–	5.18	V
Output Noise Voltage	10 Hz ≤ f ≤ 10 kHz, T_J = 25°C (Note 3.)	–	50	–	–	50	–	μV
Long Term Stability	T_A = 125°C, 1.0 kHrs. (Note 3.)	–	5.0	25	–	5.0	25	mV
Output Short Circuit	T_A = 25°C	−30	−100	−180	−30	−100	−180	mA
Oscillator Section								
Initial Accuracy	Sawtooth Mode (see Figure 7), T_J = 25°C Triangular Mode (see Figure 7), T_J = 25°C	47 47	52 52	57 57	47 44	52 52	57 60	kHz kHz
Voltage Stability	12 ≤ V_{CC} ≤ 25 V	–	0.2	1.0	–	0.2	1.0	%
Temperature Stability	Sawtooth Mode T_{MIN} ≤ T_A ≤ T_{MAX} (Note 3.) Triangular Mode T_{MIN} ≤ T_A ≤ T_{MAX} (Note 3.)	– –	5.0 8.0	– –	– –	5.0 8.0	– –	% %
Amplitude	OSC peak to peak	–	1.7	–	–	1.7	–	V
Discharge Current	T_J = 25°C T_{MIN} ≤ T_A ≤ T_{MAX}	7.5 7.2	8.3 –	9.3 9.5	7.5 7.2	8.3 –	9.3 9.5	mA mA

3. These parameters, although guaranteed, are not 100% tested in production.

*Adjust V_{CC} above the start threshold before setting at 15 V.

ELECTRICAL CHARACTERISTICS (continued) ($-25° \le T_A \le 85°$ for CS2842A/CS2843A, $0° \le T_A \le 70°$ for CS3842A/CS3843A. V_{CC} = 15 V*; R_T = 680 Ω, C_T = 0.022 μF for triangular mode, R_T = 10 kΩ, C_T = 3.3 nF for sawtooth mode (see Figure 7); unless otherwise stated.)

Characteristic	Test Conditions	CS2842A/CS2843A			CS3842A/CS3843A			Unit
		Min	Typ	Max	Min	Typ	Max	
Error Amp Section								
Input Voltage	V_{COMP} = 2.5 V	2.45	2.50	2.55	2.42	2.50	2.58	V
Input Bias Current	V_{FB} = 0	–	−0.3	−1.0	–	−0.3	−2.0	μA
A_{VOL}	$2.0 \le V_{OUT} \le 4.0$ V	65	90	–	65	90	–	dB
Unity Gain Bandwidth	Note 4.	0.7	1.0	–	0.7	1.0	–	MHz
PSRR	$12 \le V_{CC} \le 25$ V	60	70	–	60	70	–	dB
Output Sink Current	V_{FB} = 2.7 V, V_{COMP} = 1.1 V	2.0	6.0	–	2.0	6.0	–	mA
Output Source Current	V_{FB} = 2.3 V, V_{COMP} = 5.0 V	−0.5	−0.8	–	−0.5	−0.8	–	mA
V_{OUT} High	V_{FB} = 2.3 V, 15 kΩ to ground	5.0	6.0	–	5.0	6.0	–	V
V_{OUT} Low	V_{FB} = 2.7 V, 15 kΩ to V_{REF}	–	0.7	1.1	–	0.7	1.1	V
Current Sense Section								
Gain	Notes 5 & 6.	2.85	3.00	3.15	2.85	3.00	3.15	V/V
Maximum Input Signal	V_{COMP} = 5.0 V (Note 5.)	0.9	1.0	1.1	0.9	1.0	1.1	V
PSRR	$12 \le V_{CC} \le 25$ V (Note 5.)	–	70	–	–	70	–	dB
Input Bias Current	V_{SENSE} = 0	–	−2.0	−10	–	−2.0	−10	μA
Delay to Output	T_J = 25°C (Note 4.)	–	150	300	–	150	300	ns
Output Section								
Output Low Level	I_{SINK} = 20 mA I_{SINK} = 200 mA	– –	0.1 1.5	0.4 2.2	– –	0.1 1.5	0.4 2.2	V V
Output High Level	I_{SOURCE} = 20 mA I_{SOURCE} = 200 mA	13 12	13.5 13.5	– –	13 12	13.5 13.5	– –	V V
Rise Time	T_J = 25°C, C_L = 1.0 nF (Note 4.)	–	50	150	–	50	150	ns
Fall Time	T_J = 25°C, C_L = 1.0 nF (Note 4.)	–	50	150	–	50	150	ns
Output Leakage	UVLO Active, V_{OUT} = 0	–	−0.01	−10.00	–	−0.01	−10.00	μA
Total Standby Current								
Startup Current	–	–	0.5	1.0	–	0.5	1.0	mA
Operating Supply Current	V_{FB} = V_{SENSE} = 0 V, R_T = 10 kΩ, C_T = 3.3 nF	11	17	–	11	17	–	mA
V_{CC} Zener Voltage	I_{CC} = 25 mA	–	34	–	–	34	–	V

4. These parameters, although guaranteed, are not 100% tested in production.
5. Parameters measured at trip point of latch with V_{FB} = 0.
6. Gain defined as: $A = \Delta V_{COMP}/\Delta V_{SENSE}$; $0 \le V_{SENSE} \le 0.8$ V.

*Adjust V_{CC} above the start threshold before setting at 15 V.

ELECTRICAL CHARACTERISTICS (continued) ($-25° \le T_A \le 85°$ for CS2842A/CS2843A, $0° \le T_A \le 70°$ for CS3842A/CS3843A. V_{CC} = 15 V*; R_T = 680 Ω, C_T = 0.022 μF for triangular mode, R_T = 10 kΩ, C_T = 3.3 nF for sawtooth mode (see Figure 7); unless otherwise stated.)

Characteristic	Test Conditions	CS2842A			CS3842A			CS2843A/CS3843A			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Undervoltage Lockout Section											
Start Threshold	–	15	16	17	14.5	16	17.5	7.8	8.4	9.0	V
Min. Operating Voltage	After Turn On	9.0	10	11	8.5	10	11.5	7.0	7.6	8.2	V

*Adjust V_{CC} above the start threshold before setting at 15 V.

PACKAGE PIN DESCRIPTION

Package Pin Number			Symbol	Description
DIP–8	SO–8	SO–14		
1	1	1	COMP	Error amp output, used to compensate error amplifier.
2	2	3	V_{FB}	Error amp inverting input.
3	3	5	Sense	Noninverting input to Current Sense Comparator.
4	4	7	OSC	Oscillator timing network with capacitor to ground, resistor to V_{REF}.
5	5	8	GND	Ground.
–	–	9	Pwr GND	Output driver ground.
6	6	10	V_{OUT}	Output drive pin.
–	–	11	V_{CC} Pwr	Output driver positive supply.
7	7	12	V_{CC}	Positive power supply.
8	8	14	V_{REF}	Output of 5.0 V internal reference.
–	–	2, 4, 6, 13	NC	No connection.

TYPICAL PERFORMANCE CHARACTERISTICS

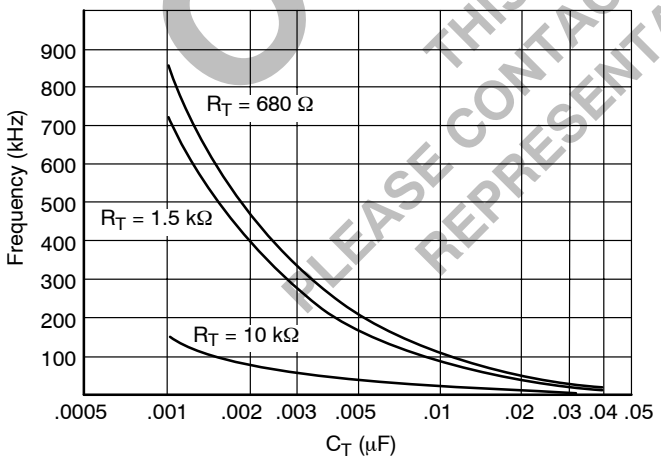


Figure 2. Oscillator Frequency vs. C_T

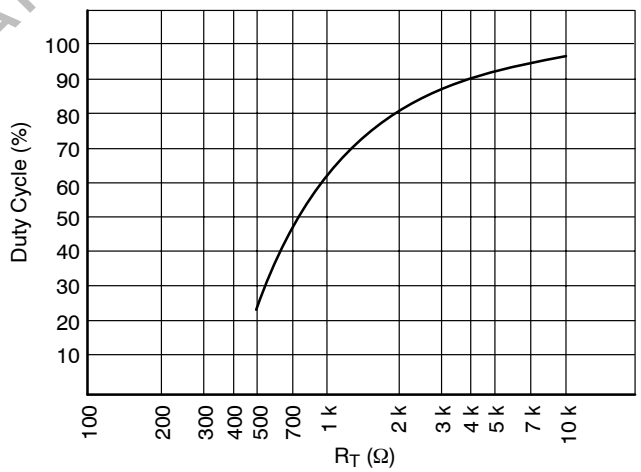


Figure 3. Oscillator Duty Cycle vs. R_T

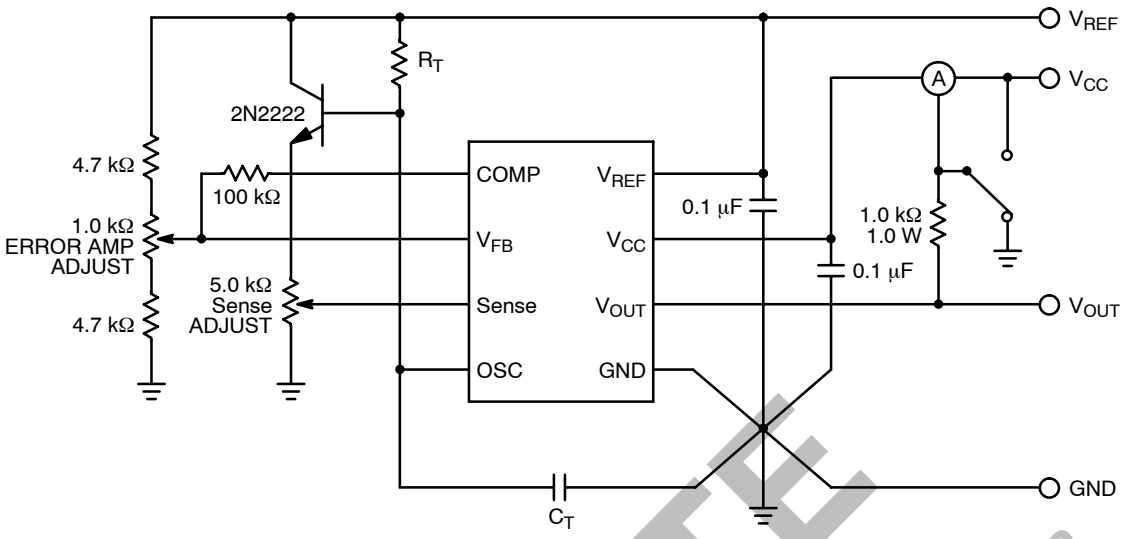


Figure 4. Test Circuit

CIRCUIT DESCRIPTION

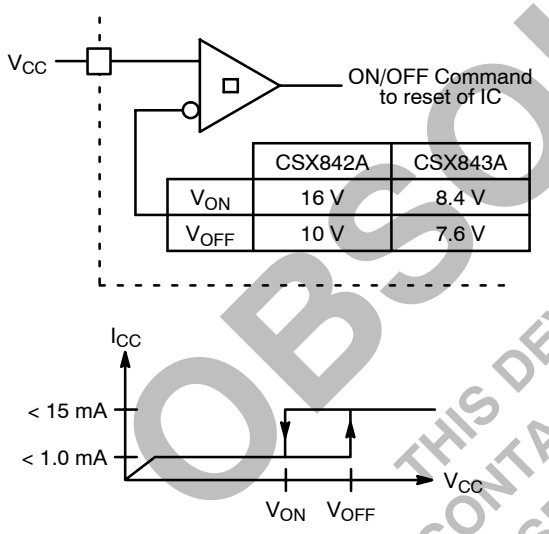


Figure 5. Typical Undervoltage Characteristics

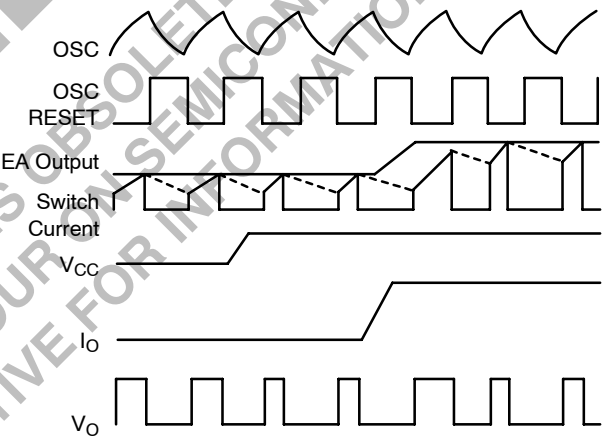


Figure 6. Timing Diagram for Key CS2841B Parameters

Undervoltage Lockout

During Undervoltage Lockout (Figure 5), the output driver is biased to a high impedance state. The output should be shunted to ground with a resistor to prevent output leakage current from activating the power switch.

PWM Waveform

To generate the PWM waveform, the control voltage from the error amplifier is compared to a current sense signal which represents the peak output inductor current (Figure 6). An increase in V_{CC} causes the inductor current slope to increase, thus reducing the duty cycle. This is an inherent feed−forward characteristic of current mode control, since the control voltage does not have to change during changes of input supply voltage.

When the power supply sees a sudden large output current increase, the control voltage will increase allowing the duty cycle to momentarily increase. Since the duty cycle tends to exceed the maximum allowed to prevent transformer saturation in some power supplies, the internal oscillator waveform provides the maximum duty cycle clamp as programmed by the selection of oscillator components.

Setting the Oscillator

Oscillator timing capacitor, C_T, is charged by V_{REF} through R_T and discharged by an internal current source. During the discharge time, the internal clock signal blanks out the output to the Low state, thus providing a user selected maximum duty cycle clamp. Charge and discharge times are determined by the formula:

$$t_c = R_T C_T \ln\left(\frac{V_{REF} - V_{lower}}{V_{REF} - V_{upper}}\right)$$

$$t_d = R_T C_T \ln\left(\frac{V_{REF} - I_d R_T - V_{lower}}{V_{REF} - I_d R_T - V_{upper}}\right)$$

Substituting in typical values for the parameters in the above formulas:

V_{REF} = 5.0 V
V_{upper} = 2.7 V
V_{lower} = 1.0 V
I_d = 8.3 mA
$t_c \approx 0.5534 R_T C_T$

$$t_d = R_T C_T \ln\left(\frac{2.3 - 0.0083 R_T}{4.0 - 0.0083 R_T}\right)$$

The frequency and maximum duty cycle can be determined using the Typical Performance Characteristic graphs.

Grounding

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to GND pin in a single point ground.

The transistor and 5.0 kΩ potentiometer, shown in the test circuit, are used to sample the oscillator waveform and apply and adjustable ramp to Sense.

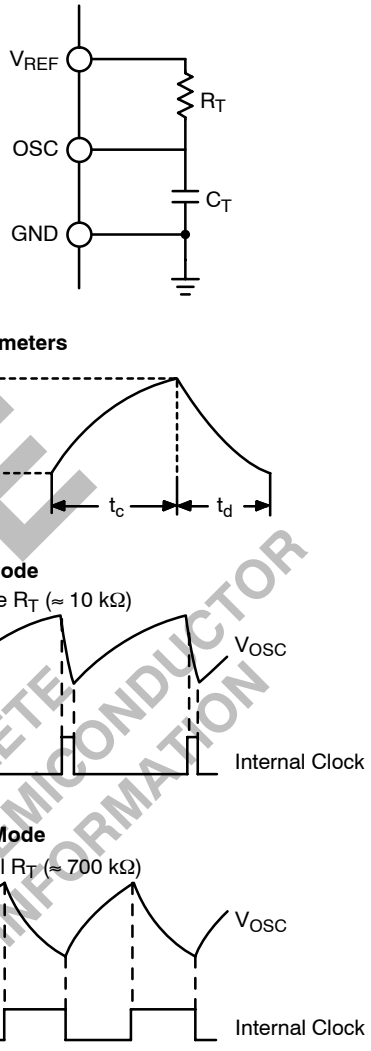


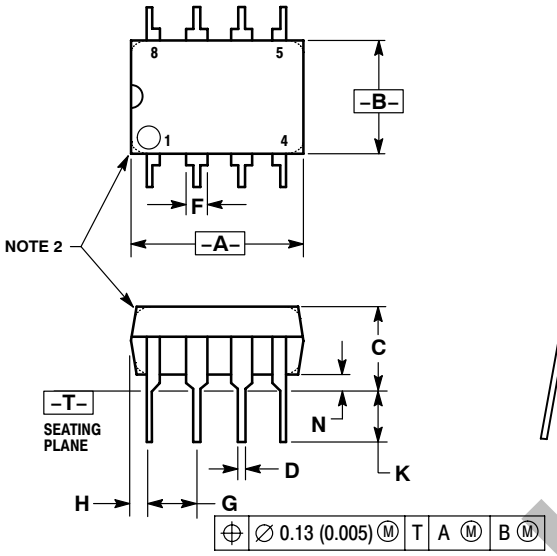
Figure 7. Oscillator Timing Network and Parameters

ORDERING INFORMATION

Device	Temperature Range	Package	Shipping
CS2842ALN8	−25°C to 85°C	DIP−8	50 Units/Rail
CS2843ALN8		DIP−8	50 Units/Rail
CS2842ALD14		SO−14	55 Units/Rail
CS2842ALDR14		SO−14	2500 Tape & Reel
CS3842AGN8	0°C to 70°C	DIP−8	50 Units/Rail
CS3842AGD8		SO−8	98 Units/Rail
CS3842AGDR8		SO−8	2500 Tape & Reel
CS3842AGD14		SO−14	55 Units/Rail
CS3842AGDR14		SO−14	2500 Tape & Reel
CS3843AGN8		DIP−8	50 Units/Rail
CS3843AGD8		SO−8	98 Units/Rail
CS3843AGDR8		SO−8	2500 Tape & Reel
CS3843AGD14		SO−14	55 Units/Rail
CS3843AGDR14		SO−14	2500 Tape & Reel

PACKAGE DIMENSIONS

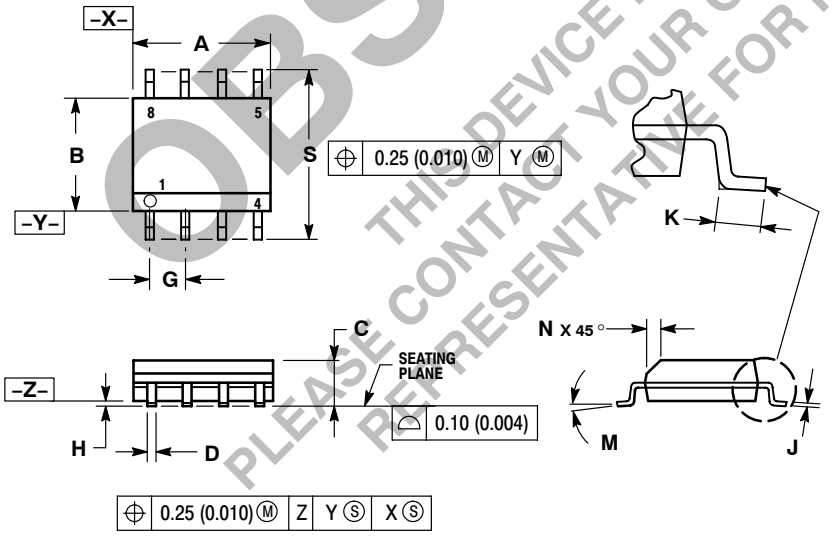
DIP−8
N SUFFIX
CASE 626−05
ISSUE L



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	---	10°	---	10°
N	0.76	1.01	0.030	0.040

SO−8
D SUFFIX
CASE 751−07
ISSUE W

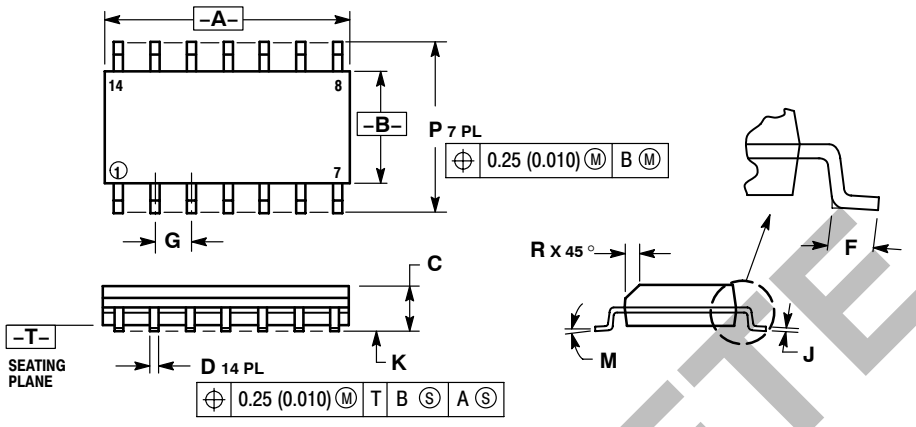


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

PACKAGE DIMENSIONS

SO–14
D SUFFIX
CASE 751A–03
ISSUE F



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	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PUBLICATION ORDERING INFORMATION

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