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April 2010

# FUSB2500
# USB2.0 High-Speed OTG Transceiver with ULPI Interface

## Features

- Complies with USB 2.0 OTG Rev 1.3 Supplement and ULPI Rev 1.1 Specifications
- Supports 480Mbps, 12Mbps, and 1.5Mbps USB2.0 Speeds
  - Integrated Termination Resistors Meet USB2.0 Resistor ECN
  - Integrated Serializer and Deserializer
  - Insertion and Removal of Stuffed Bits as Appropriate
  - USB Clock and Data Recovery to ±150ppm
- Supports USB OTG Rev 1.3 Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)

## Applications

- Cell phones, Digital Still Camera, PDA
- DVD Recorder, Scanner, Printer
- Video Camera, Set-Top Box, MP3 Player

## IMPORTANT NOTE:

*For additional performance information, please contact analogswitch@fairchildsemi.com.*

## Description

The FUSB2500 is a UTMI+ Low-Pin Interface (ULPI) USB2.0 On-The-Go (OTG) transceiver. It is compliant with the Universal Serial Bus Specification Rev 2.0 (USB2.0), the ULPI Specification Rev. 1.1, and the OOTG Supplement to USB2.0, Rev. 1.3.

The FUSB2500 is optimized to connect the USB2.0 host, peripheral, or OTG-controller to the USB connector via the ULPI link. Data can be transmitted and received at high speed (480Mbps), full speed (12Mbps), and low speed (1.5Mbps) through a 12-bit (SDR) interface.

The FUSB2500 also includes a charger-detection functional block that enables automatic detection for charging USB2.0 host ports or dedicated chargers. The FUSB2500 is compliant with Battery Charging Specification Rev. 1.0.

## Related Resources

- *UTMI+ Low Pin Interface Specification (ULPI), Revision 1.1, October 20, 2004.* http://www.ulpi.org
- *UTMI+ Specification, Revision 1.0, February 22, 2004.* http://www.ulpi.org

## Ordering Information

| Part Number | Top Mark | Operating Temperature Range | Package |
|---|---|---|---|
| FUSB2500GFX | FUSB2500 | -40 to +85°C | 36-Ball, Ball Grid Array (BGA), 3.5 x 3.5 x 1.0mm, 0.5mm Pitch |

## Block Diagram

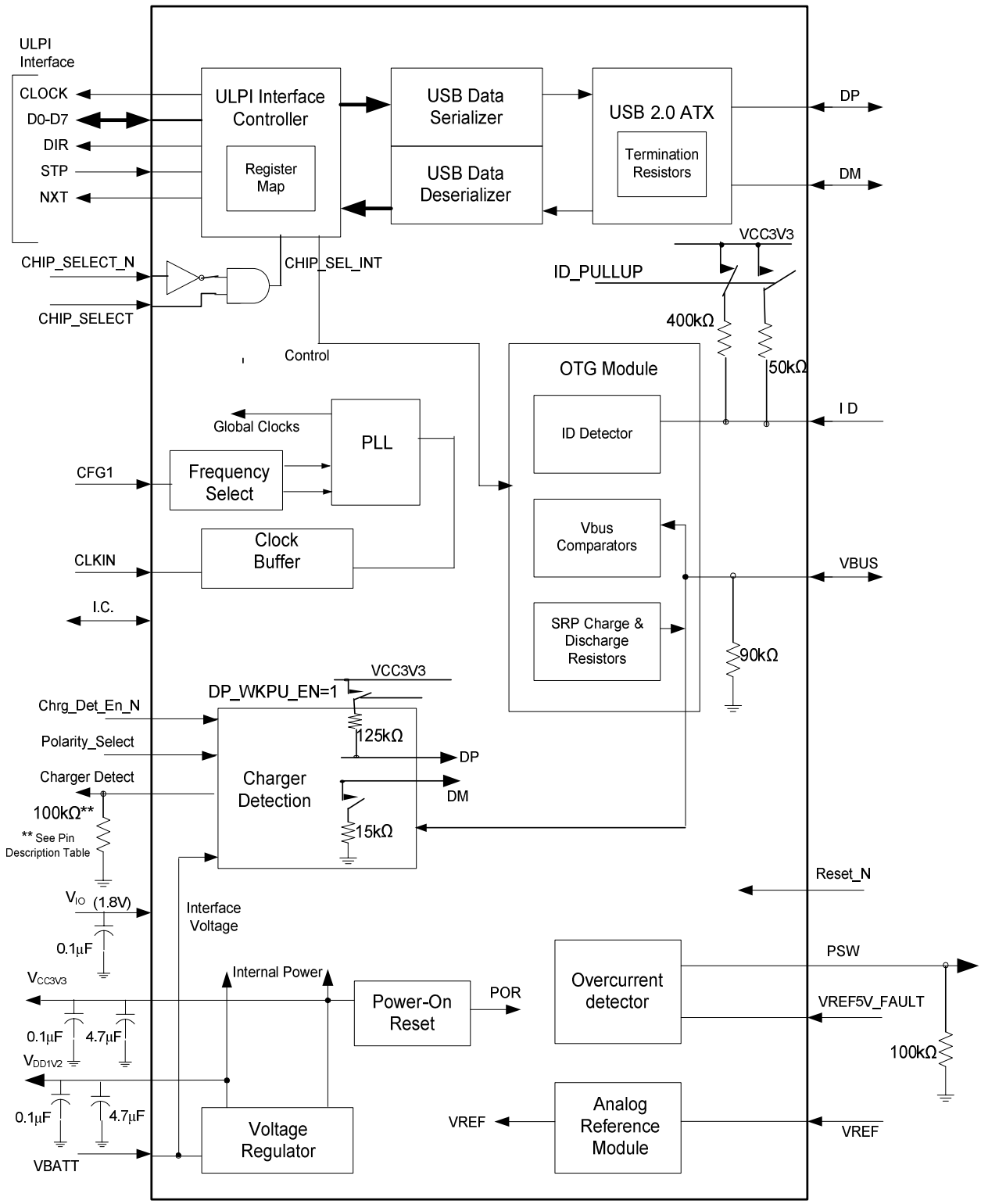


**Figure 1. Functional Block Diagram**

## Ball Configuration

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| F | Polarity Select | Charger Detect | VBATT | VBUS | CLKIN (19.2MHz) | I.C. |
| E | Charger Detect Enable_N | VREF5V_ FAULT | VCC3V3 | GND | DIR | VDD1V2 |
| D | DP | GND | ID | PSW | NXT | STP |
| C | DM | RREF | Chip Select_N | Reset_N | GND | D7 |
| B | D0 | VIO (1.8V) | Chip_Select | CFG1 (GND 19.2MHz) | VIO (1.8V) | D6 |
| A | D1 | D2 | D3 | CLOCK | D4 | D5 |

**Figure 2. Ball Configuration (Bottom Up View)**

## Pin Definitions

| Symbol[1] | Ball | Type[2] | Description |
|---|---|---|---|
| Chip_Select | B3 | I | Active HIGH. LOW – ULPI pin three-stated; HIGH – ULPI operates normally. TTL compatible; CMOS input with hysteresis. If either Chip_Select or Chip_Select_N are de-asserted, the FUSB2500 is in power down and the ULPI bus is three-stated. For ULPI to operate, both signals need to be active. |
| Chip Select_N | C3 | I | Active LOW. HIGH – ULPI pin three-stated; LOW – ULPI operates normally. TTL compatible; CMOS input with hysteresis. If either Chip_Select or Chip_Select_N are de-asserted, the FUSB2500 is in power down and the ULPI bus is three-stated. For ULPI to operate, both signals need to be active. |
| $R_{REF}$ | C2 | AI/O | Resistor reference. Connect through 12kΩ ±1% to GND. |
| DM | C1 | AI/O | USB D- pin. This pin is 5V tolerant.<br>USB mode: data minus (D-) pin of the USB cable. |
| DP[3] | D1 | AI/O | USB D+ pin. This pin is 5V tolerant.<br>USB mode: data plus (D+) pin of the USB cable. |
| VREF5V_FAULT | E2 | I | VREF5V_FAULT is used to signal a $V_{BUS}$ over-current/over-voltage condition from an external SMPS or power management IC. The link must enable this function via the ExternalVbusFault register bit and the polarity must be set via the ExternalVbusActiveLow register bit. |
| ID | D3 | I | Identification (ID) pin of the micro-USB cable. TTL, If not used, connect to the $V_{CC3V3}$ pin. |
| Charger Detect | F2 | O | If polarity is to be active LOW, connect 100KΩ to $V_{BATT}$ (in open-drain mode). If polarity is to be active HIGH, 100KΩ to GND is needed (open source). This is a 5V-tolerant pin referenced to an internal 3.3V rail generated from $V_{BATT}$ for charger detection when in power-down mode. |
| Polarity Select | F1 | I | When connected to GND, the charger-detect signal is active LOW. When connected to $V_{BATT}$, the charger detect signal is active HIGH. This is a 5V-tolerant pin referenced to an internal 3.3V rail generated from $V_{BATT}$ for charger detection when in power-down mode. |
| Charger Detect Enable_N | E1 | I | Active LOW. Connect to GND to activate. Connect to $V_{BATT}$ when charger detection is not required. This is a 5V-tolerant pin referenced to an internal 3.3V rail generated from $V_{BATT}$ for charger detection when in power-down mode. |
| $V_{BATT}$ | F3 | P | Input supply voltage or battery source. Nominally 2.7V to 4.5V. Operation of USB should function down to $V_{BATT}$ of 3.0V. Products may stop operating at $V_{BATT}$ of 3.1V.[4] |
| PSW | D4 | O | Controls an external, active HIGH, $V_{BUS}$ power switch/charge pump and/or an SMPS charger IC. An external 100KΩ pull-down resistor is required. Open source, this pin is referenced to $V_{CC3V3}$. |
| $V_{BUS}$ | F4 | AI/O | Should be connected to the $V_{BUS}$ pin of the USB cable. Leave open circuit if not used. An internal 90KΩ ±11% pull-down resistor is present on this pin. |
| $V_{CC3V3}$ | E3 | P | 3.3V regulator output requiring capacitors. Internally powers OTG, analog core, and ATX. External capacitors are 0.1µF and 4.7µF. |
| CLKIN | F5 | I | Clock input; 1.8V peak input allowed; frequency depends on the CFG1 pin. This is a digital input buffer, not analog for a crystal. |
| I.C. | F6 | I/O | Internally connected; leave OPEN. |

*Continued on the following page...*

## Pin Definitions (Continued)

| Symbol[1] | Ball | Type[2] | Description |
|---|---|---|---|
| CFG1 | B4 | I | Configures the clock frequency;<br>0: input is 19.2MHz.<br>1: input is 26MHz. |
| $V_{DD1V2}$ | E6 | P | 1.2V regulator output requiring capacitors. Internally powers the digital core. External capacitors are 0.1µF and 4.7µF. |
| DIR | E5 | O | ULPI direction output signal; slew-rate-controlled output (2ns typical). |
| STP | D6 | I | ULPI stop input signal; CMOS input. |
| NXT | D5 | O | ULPI next output signal; slew-rate-controlled output (2ns typical). |
| D7 | C6 | I/O | ULPI data pin 7; three-state output; slew-rate-controlled output (2ns typical); CMOS input. |
| D6 | B6 | I/O | ULPI data pin 6; three-state output; slew-rate-controlled output (2ns typical); CMOS input. |
| D5 | A6 | I/O | ULPI data pin 5; three-state output; slew-rate-controlled output (2ns typical); CMOS input. |
| D4 | A5 | I/O | ULPI data pin 4; three-state output; slew-rate-controlled output (2ns typical); CMOS input. |
| D3 | A3 | I/O | ULPI data pin 3; three-state output; slew-rate-controlled output (2ns typical); CMOS input. |
| D2 | A2 | I/O | ULPI data pin 2; three-state output; slew-rate-controlled output ( 2ns typical); CMOS input. |
| D1 | A1 | I/O | ULPI data pin 1; three-state output; slew-rate-controlled output ( 2ns typical); CMOS input. |
| D0 | B1 | I/O | ULPI data pin 0; three-state output; slew-rate-controlled output ( 2ns typical); CMOS input. |
| CLOCK | A4 | O | 60MHz clock output when digital 19.2MHz (or 26MHz) clock is applied; Push-pull output; slew-rate-controlled output (2ns). |
| $V_{IO}$ | B2, B5 | P | Input I/O supply rail; 1.65V-1.95V; nominally 1.8V. 0.1µF capacitor connected to power input. |
| Reset_N | C4 | I | Connect to $V_{IO}$ 1.8V when not used. Resets the transceiver; active LOW. |
| GND | E4,D2, C5 | P | Connect to ground. |

**Notes:**

1. Symbol names ending with underscore N (for example, NAME_N) indicate active LOW signals.
2. I=input; O=output; I/O=digital input/output; OD=open-drain output; AI/O=analog input/output; P=power or ground pin.
3. A 125KΩ resistor is used for basic charger detection.
4. Per the USB2.0 specification, below a supply of 2.97V, USB full-speed and low-speed transactions are not guaranteed; although some devices may continue to function with the FUSB2500 at the lower supply rail.

## Physical Dimensions

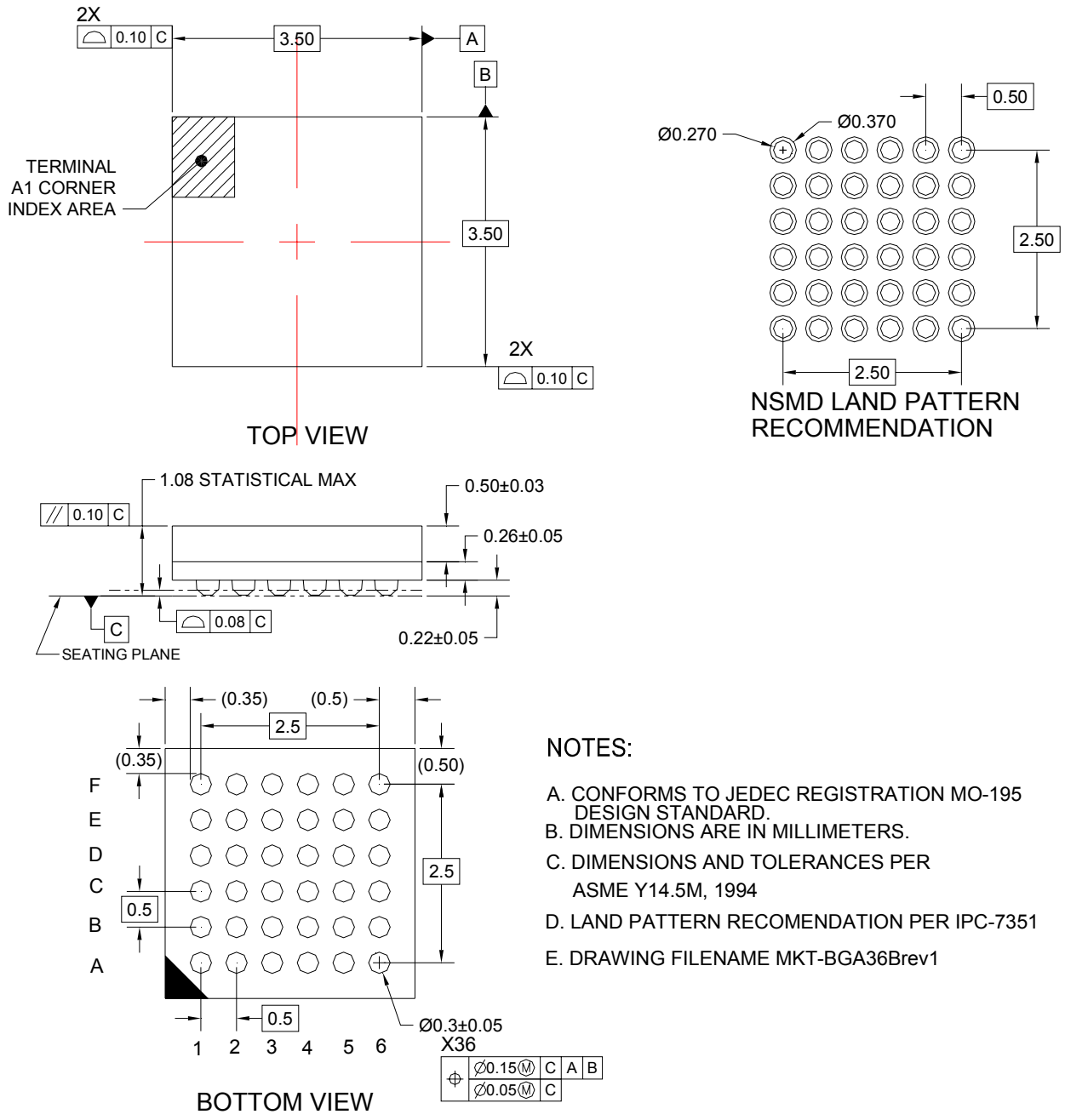


**Figure 24. 36-Ball BGA Package**

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