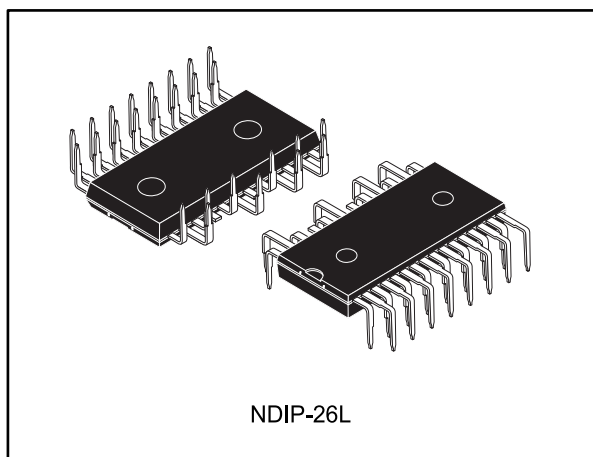


## SLLIMM™-nano small low-loss intelligent molded module IPM, 3 A, 600 V, 3-phase IGBT inverter bridge

Datasheet - production data



### Features

- IPM 3 A, 600 V, 3-phase IGBT inverter bridge including control ICs for gate driving and freewheeling diodes
- Optimized for low electromagnetic interference
- $V_{CE(sat)}$  negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull down/pull up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Smart shutdown function
- Comparator for fault protection against overtemperature and overcurrent
- Op amp for advanced current sensing
- Optimized pinout for easy board layout

### Applications

- 3-phase inverters for motor drives
- Dish washers, refrigerator compressors, heating systems, air-conditioning fans, draining and recirculation pumps

### Description

This intelligent power module implements a compact, high performance AC motor drive in a simple, rugged design. It is composed of six IGBTs with freewheeling diodes and three half-bridge HVICs for gate driving, providing low electromagnetic interference (EMI) characteristics with optimized switching speed. The package is optimized for thermal performance and compactness in built-in motor applications, or other low power applications where assembly space is limited. This IPM includes an operational amplifier, completely uncommitted, and a comparator that can be used to design a fast and efficient protection circuit. SLLIMM™ is a trademark of STMicroelectronics.

Table 1: Device summary

| Order code   | Marking    | Package  | Packing |
|--------------|------------|----------|---------|
| STGIPN3H60-H | GIPN3H60-H | NDIP-26L | Tube    |

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## Contents

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# 1 Internal schematic diagram and pin configuration

Figure 1: Internal schematic diagram

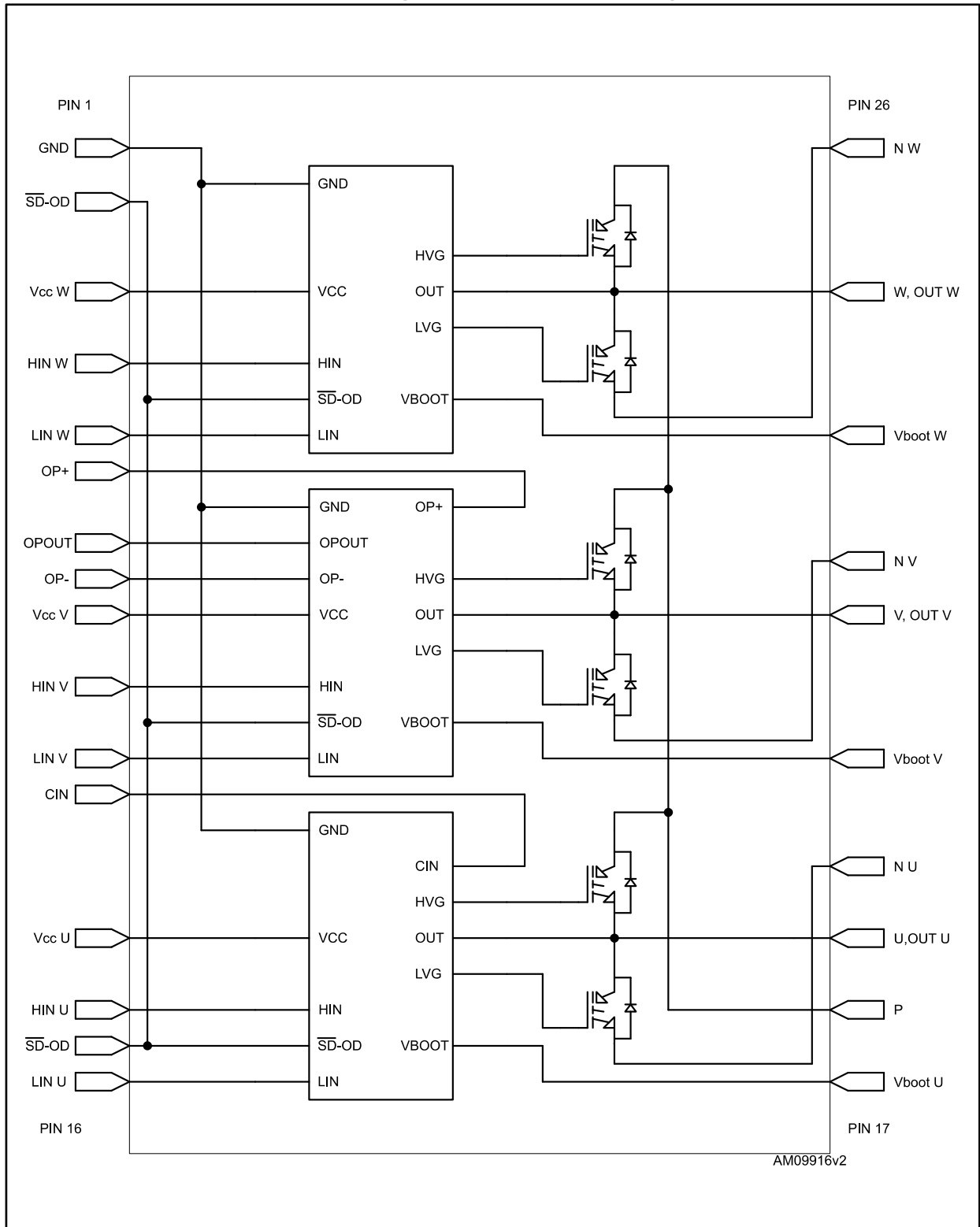
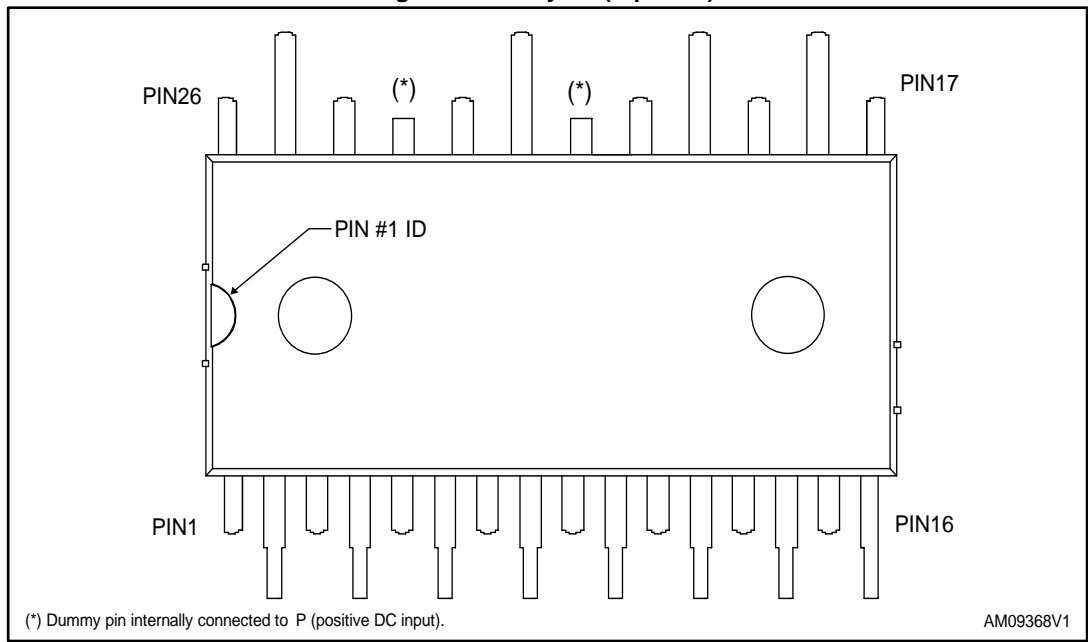


Table 2: Pin description

| Pin | Symbol               | Description   |
|-----|----------------------|---|
| 1   | GND                  | Ground  |
| 2   | $\overline{SD}$ / OD | Shut down logic input (active low) / open drain (comparator output) |
| 3   | V <sub>CC</sub> W    | Low voltage power supply W phase                                    |
| 4   | HIN W                | High side logic input for W phase                                   |
| 5   | LIN W                | Low side logic input for W phase                                    |
| 6   | OP+                  | Op amp non inverting input  |
| 7   | OP <sub>OUT</sub>    | Op amp output   |
| 8   | OP-                  | Op amp inverting input  |
| 9   | V <sub>CC</sub> V    | Low voltage power supply V phase                                    |
| 10  | HIN V                | High side logic input for V phase                                   |
| 11  | LIN V                | Low side logic input for V phase                                    |
| 12  | CIN                  | Comparator input  |
| 13  | V <sub>CC</sub> U    | Low voltage power supply for U phase                                |
| 14  | HIN U                | High side logic input for U phase                                   |
| 15  | $\overline{SD}$ / OD | Shut down logic input (active low) / open drain (comparator output) |
| 16  | LIN U                | Low side logic input for U phase                                    |
| 17  | V <sub>BOOT</sub> U  | Bootstrap voltage for U phase                                       |
| 18  | P                    | Positive DC input   |
| 19  | U, OUT <sub>U</sub>  | U phase output  |
| 20  | N <sub>U</sub>       | Negative DC input for U phase                                       |
| 21  | V <sub>BOOT</sub> V  | Bootstrap voltage for V phase                                       |
| 22  | V, OUT <sub>V</sub>  | V phase output  |
| 23  | N <sub>V</sub>       | Negative DC input for V phase                                       |
| 24  | V <sub>BOOT</sub> W  | Bootstrap voltage for W phase                                       |
| 25  | W, OUT <sub>W</sub>  | W phase output  |
| 26  | N <sub>W</sub>       | Negative DC input for W phase                                       |

Figure 2: Pin layout (top view)



## 2 Electrical ratings

### 2.1 Absolute maximum ratings

Table 3: Inverter part

| Symbol                           | Parameter  | Value | Unit |
|----------------------------------|--|-------|------|
| V <sub>CES</sub>                 | Each IGBT collector emitter voltage (V <sub>IN</sub> <sup>(1)</sup> = 0) | 600   | V    |
| ± I <sub>C</sub> <sup>(2)</sup>  | Each IGBT continuous collector current at T <sub>C</sub> = 25°C          | 3     | A    |
| ± I <sub>CP</sub> <sup>(3)</sup> | Each IGBT pulsed collector current                                       | 18    | A    |
| P <sub>TOT</sub>                 | Each IGBT total dissipation at T <sub>C</sub> = 25°C                     | 8     | W    |

**Notes:**

(1) Applied between HIN<sub>i</sub>, LIN<sub>i</sub> and GND for i = U, V, W.

(2) Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

(3) Pulse width limited by max junction temperature.

Table 4: Control part

| Symbol               | Parameter   | Min.                   | Max.                    | Unit |
|----------------------|---|------------------------|-------------------------|------|
| V <sub>OUT</sub>     | Output voltage applied between OUT <sub>U</sub> , OUT <sub>V</sub> , OUT <sub>W</sub> - GND | V <sub>boot</sub> - 21 | V <sub>boot</sub> + 0.3 | V    |
| V <sub>CC</sub>      | Low voltage power supply  | - 0.3                  | 21                      | V    |
| V <sub>CIN</sub>     | Comparator input voltage  | - 0.3                  | V <sub>CC</sub> + 0.3   | V    |
| V <sub>op+</sub>     | OPAMP non-inverting input   | - 0.3                  | V <sub>CC</sub> + 0.3   | V    |
| V <sub>op-</sub>     | OPAMP inverting input   | - 0.3                  | V <sub>CC</sub> + 0.3   | V    |
| V <sub>boot</sub>    | Bootstrap voltage   | - 0.3                  | 620                     | V    |
| V <sub>IN</sub>      | Logic input voltage applied between HIN, LIN and GND  | - 0.3                  | 15                      | V    |
| V <sub>SD/OD</sub>   | Open drain voltage  | - 0.3                  | 15                      | V    |
| ΔV <sub>OUT/dT</sub> | Allowed output slew rate  |                        | 50                      | V/ns |

Table 5: Total system

| Symbol           | Parameter   | Value      | Unit |
|------------------|---|------------|------|
| V <sub>ISO</sub> | Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 s.) | 1000       | V    |
| T <sub>j</sub>   | Power chips operating junction temperature range  | -40 to 150 | °C   |
| T <sub>C</sub>   | Module operation case temperature range   | -40 to 125 | °C   |

## 2.2 Thermal data

Table 6: Thermal data

| Symbol            | Parameter                           | Value | Unit |
|-------------------|-------------------------------------|-------|------|
| R <sub>thJA</sub> | Thermal resistance junction-ambient | 50    | °C/W |

### 3 Electrical characteristics

#### 3.1 Inverter part

$T_J = 25\text{ °C}$  unless otherwise specified.

**Table 7: Static**

| Symbol        | Parameter   | Test conditions  | Min. | Typ. | Max. | Unit          |
|---------------|---|--|------|------|------|---------------|
| $V_{CE(sat)}$ | Collector-emitter saturation voltage                          | $V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(1)} = 0\text{ to }5\text{ V}$ , $I_C = 1\text{ A}$                         | -    | 2.15 | 2.6  | V             |
|               |   | $V_{CC} = V_{boot} = 15\text{ V}$ , $V_{IN}^{(1)} = 0\text{ to }5\text{ V}$ , $I_C = 1\text{ A}$ , $T_J = 125\text{ °C}$ | -    | 1.65 |      |               |
| $I_{CES}$     | Collector-cut off current ( $V_{IN}^{(1)} = 0$ "logic state") | $V_{CE} = 550\text{ V}$ , $V_{CC} = V_{Boot} = 15\text{ V}$  | -    |      | 250  | $\mu\text{A}$ |
| $V_F$         | Diode forward voltage   | $V_{IN}^{(1)} = 0$ "logic state", $I_C = 1\text{ A}$   | -    |      | 1.7  | V             |

**Notes:**

<sup>(1)</sup>Applied between  $HIN_i$ ,  $LIN_i$  and  $GND$  for  $i = U, V, W$ .

**Table 8: Inductive load switching time and energy**

| Symbol             | Parameter                 | Test conditions   | Min. | Typ. | Max. | Unit          |
|--------------------|---------------------------|---|------|------|------|---------------|
| $t_{on}^{(1)}$     | Turn-on time              | $V_{DD} = 300\text{ V}$ ,<br>$V_{CC} = V_{boot} = 15\text{ V}$ ,<br>$V_{IN}^{(2)} = 0\text{ to }5\text{ V}$ ,<br>$I_C = 1\text{ A}$<br>(see <a href="#">Figure 4: "Switching time definition"</a> ) | -    | 275  | -    | ns            |
| $t_{c(on)}^{(1)}$  | Crossover time (on)       |   | -    | 90   | -    |               |
| $t_{off}^{(1)}$    | Turn-off time             |   | -    | 890  | -    |               |
| $t_{c(off)}^{(1)}$ | Crossover time (off)      |   | -    | 125  | -    |               |
| $t_{rr}$           | Reverse recovery time     |   | -    | 50   | -    | $\mu\text{J}$ |
| $E_{on}$           | Turn-on switching energy  |   | -    | 18   | -    |               |
| $E_{off}$          | Turn-off switching energy | -   | 13   | -    |      |               |

**Notes:**

<sup>(1)</sup> $t_{ON}$  and  $t_{OFF}$  include the propagation delay time of the internal drive.  $t_{c(ON)}$  and  $t_{c(OFF)}$  are the switching time of IGBT itself under the internally given gate driving condition.

<sup>(2)</sup>Applied between  $HIN_i$ ,  $LIN_i$  and  $GND$  for  $i = U, V, W$ .



Figure 3: Switching time test circuit

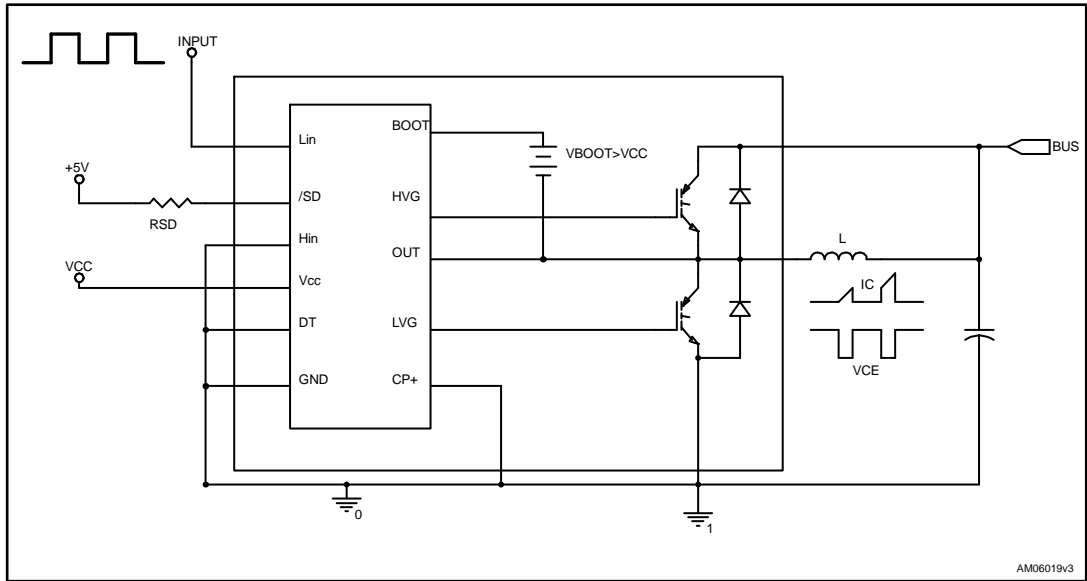
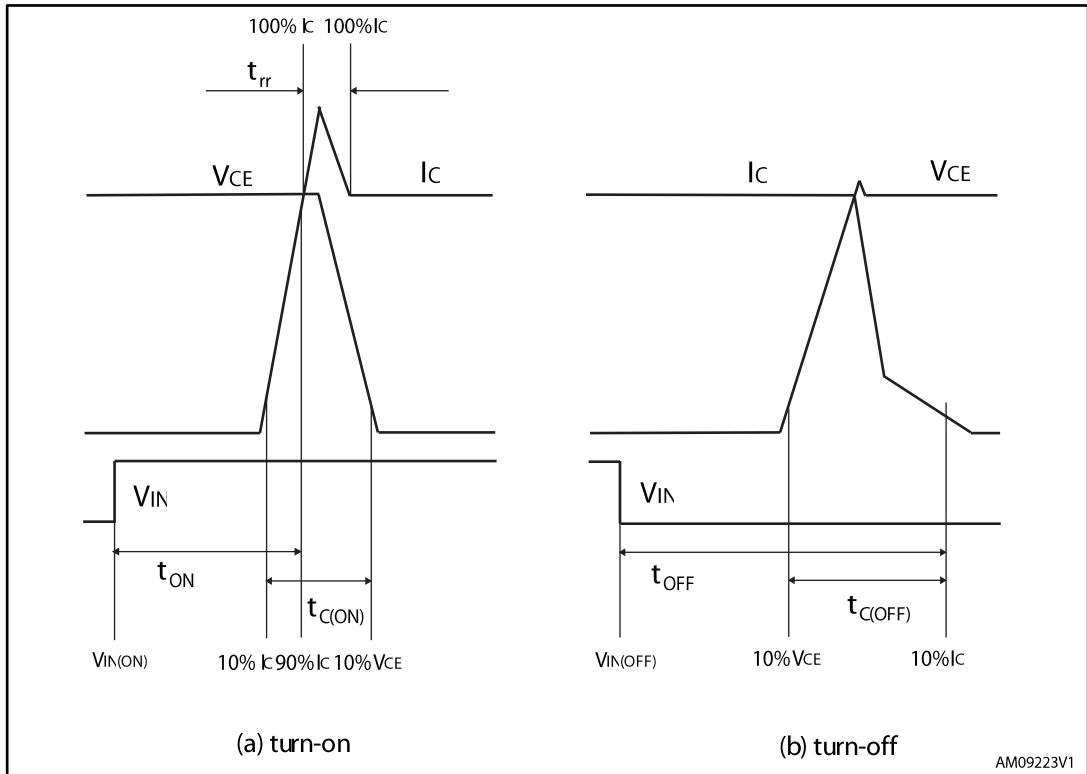


Figure 4: Switching time definition<sup>(1)</sup>



Notes:

<sup>(1)</sup> Figure 4: "Switching time definition" refers to HIN, LIN inputs (active high).

### 3.2 Control part

Table 9: Low voltage power supply ( $V_{CC} = 15\text{ V}$  unless otherwise specified)

| Symbol          | Parameter                                   | Test conditions   | Min. | Typ. | Max. | Unit          |
|-----------------|---|---|------|------|------|---------------|
| $V_{CC\_hys}$   | $V_{CC}$ UV hysteresis                      |   | 1.2  | 1.5  | 1.8  | V             |
| $V_{CC\_thON}$  | $V_{CC}$ UV turn ON threshold               |   | 11.5 | 12   | 12.5 | V             |
| $V_{CC\_thOFF}$ | $V_{CC}$ UV turn OFF threshold              |   | 10   | 10.5 | 11   | V             |
| $I_{qccu}$      | Undervoltage quiescent supply current       | $V_{CC} = 10\text{ V}$ , $\overline{SD} / OD = 5\text{ V}$ , $LIN = 0$ ,<br>$HIN = 0$ , $CIN = 0$ |      |      | 150  | $\mu\text{A}$ |
| $I_{qcc}$       | Quiescent current                           | $V_{CC} = 15\text{ V}$ , $\overline{SD} / OD = 5\text{ V}$ , $LIN = 0$ ,<br>$HIN = 0$ , $CIN = 0$ |      |      | 1    | mA            |
| $V_{ref}$       | Internal comparator (CIN) reference voltage |   | 0.5  | 0.54 | 0.58 | V             |

Table 10: Bootstrapped voltage ( $V_{CC} = 15\text{ V}$  unless otherwise specified)

| Symbol          | Parameter                               | Test conditions  | Min. | Typ. | Max. | Unit          |
|-----------------|---|--|------|------|------|---------------|
| $V_{BS\_hys}$   | $V_{BS}$ UV hysteresis                  |  | 1.2  | 1.5  | 1.8  | V             |
| $V_{BS\_thON}$  | $V_{BS}$ UV turn ON threshold           |  | 11.1 | 11.5 | 12.1 | V             |
| $V_{BS\_thOFF}$ | $V_{BS}$ UV turn OFF threshold          |  | 9.8  | 10   | 10.6 | V             |
| $I_{qBSU}$      | Undervoltage $V_{BS}$ quiescent current | $V_{BS} < 9\text{ V}$ , $\overline{SD} / OD = 5\text{ V}$ , $LIN = 0$ ,<br>$HIN = 5\text{ V}$ , $CIN = 0$  |      | 70   | 110  | $\mu\text{A}$ |
| $I_{qBS}$       | $V_{BS}$ quiescent current              | $V_{BS} = 15\text{ V}$ , $\overline{SD} / OD = 5\text{ V}$ , $LIN = 0$ ,<br>$HIN = 5\text{ V}$ , $CIN = 0$ |      | 150  | 210  | $\mu\text{A}$ |
| $R_{DS(on)}$    | Bootstrap driver on-resistance          | LVG ON   |      | 120  |      | $\Omega$      |

Table 11: Logic inputs ( $V_{CC} = 15\text{ V}$  unless otherwise specified)

| Symbol     | Parameter                                    | Test conditions   | Min. | Typ. | Max. | Unit          |
|------------|--|---|------|------|------|---------------|
| $V_{il}$   | Low logic level voltage                      |   |      |      | 0.8  | V             |
| $V_{ih}$   | High logic level voltage                     |   | 2.25 |      |      | V             |
| $I_{HINH}$ | HIN logic "1" input bias current             | HIN = 15 V  | 20   | 40   | 100  | $\mu\text{A}$ |
| $I_{HINI}$ | HIN logic "0" input bias current             | HIN = 0 V   |      |      | 1    | $\mu\text{A}$ |
| $I_{LINh}$ | LIN logic "1" input bias current             | LIN = 15 V  | 20   | 40   | 100  | $\mu\text{A}$ |
| $I_{LINI}$ | LIN logic "0" input bias current             | LIN = 0 V   |      |      | 1    | $\mu\text{A}$ |
| $I_{SDh}$  | $\overline{SD}$ logic "0" input bias current | $\overline{SD} = 15\text{ V}$   | 30   | 120  | 300  | $\mu\text{A}$ |
| $I_{SDI}$  | $\overline{SD}$ logic "1" input bias current | $\overline{SD} = 0\text{ V}$  |      |      | 3    | $\mu\text{A}$ |
| $D_t$      | Dead time                                    | see <a href="#">Figure 5: "Dead time and interlocking waveform definitions"</a> |      | 180  |      | ns            |

Table 12: OPAMP characteristics ( $V_{CC} = 15\text{ V}$  unless otherwise specified)

| Symbol    | Parameter                         | Test condition  | Min. | Typ. | Max. | Unit             |
|-----------|-----------------------------------|---|------|------|------|------------------|
| $V_{io}$  | Input offset voltage              | $V_{ic} = 0\text{ V}$ , $V_o = 7.5\text{ V}$                |      |      | 6    | mV               |
| $I_{io}$  | Input offset current              | $V_{ic} = 0\text{ V}$ , $V_o = 7.5\text{ V}$                |      | 4    | 40   | nA               |
| $I_{ib}$  | Input bias current <sup>(1)</sup> |   |      | 100  | 200  | nA               |
| $V_{icm}$ | Input common mode voltage range   |   | 0    |      |      | V                |
| $V_{OL}$  | Low level output voltage          | $R_L = 10\text{ k}\Omega$ to $V_{CC}$                       |      | 75   | 150  | mV               |
| $V_{OH}$  | High level output voltage         | $R_L = 10\text{ k}\Omega$ to GND                            | 14   | 14.7 |      | V                |
| $I_o$     | Output short-circuit current      | Source, $V_{id} = +1\text{ V}$ ; $V_o = 0\text{ V}$         | 16   | 30   |      | mA               |
|           |                                   | Sink, $V_{id} = -1\text{ V}$ ; $V_o = V_{CC}$               | 50   | 80   |      | mA               |
| SR        | Slew rate                         | $V_i = 1 - 4\text{ V}$ ; $C_L = 100\text{ pF}$ ; unity gain | 2.5  | 3.8  |      | V/ $\mu\text{s}$ |
| GBWP      | Gain bandwidth product            | $V_o = 7.5\text{ V}$  | 8    | 12   |      | MHz              |
| $A_{vd}$  | Large signal voltage gain         | $R_L = 2\text{ k}\Omega$                                    | 70   | 85   |      | dB               |
| SVR       | Supply voltage rejection ratio    | vs. $V_{CC}$  | 60   | 75   |      | dB               |
| CMRR      | Common mode rejection ratio       |   | 55   | 70   |      | dB               |

**Notes:**

<sup>(1)</sup>The direction of input current is out of the IC.

Table 13: Sense comparator characteristics ( $V_{CC} = 15\text{ V}$  unless otherwise specified)

| Symbol        | Parameter  | Test conditions   | Min. | Typ. | Max. | Unit               |
|---------------|--|---|------|------|------|--------------------|
| $I_{ib}$      | Input bias current   | $V_{CIN} = 1\text{ V}$  |      |      | 3    | $\mu\text{A}$      |
| $V_{ol}$      | Open drain low level output voltage  | $I_{od} = 3\text{ mA}$  |      |      | 0.5  | V                  |
| $t_{d\_comp}$ | Comparator delay   | $\overline{SD}$ /OD pulled to 5 V through 100 k $\Omega$ resistor |      | 90   | 130  | ns                 |
| SR            | Slew rate  | $C_L = 180\text{ pF}$ ; $R_{pu} = 5\text{ k}\Omega$               |      | 60   |      | V/ $\mu\text{sec}$ |
| $t_{sd}$      | Shutdown to high / low side driver propagation delay                       | $V_{OUT} = 0$ , $V_{boot} = V_{CC}$ , $V_{IN} = 0$ to 3.3 V       | 50   | 125  | 200  | ns                 |
| $t_{isd}$     | Comparator triggering to high / low side driver turn-off propagation delay | Measured applying a voltage step from 0 V to 3.3 V to pin CIN     | 50   | 200  | 250  |                    |

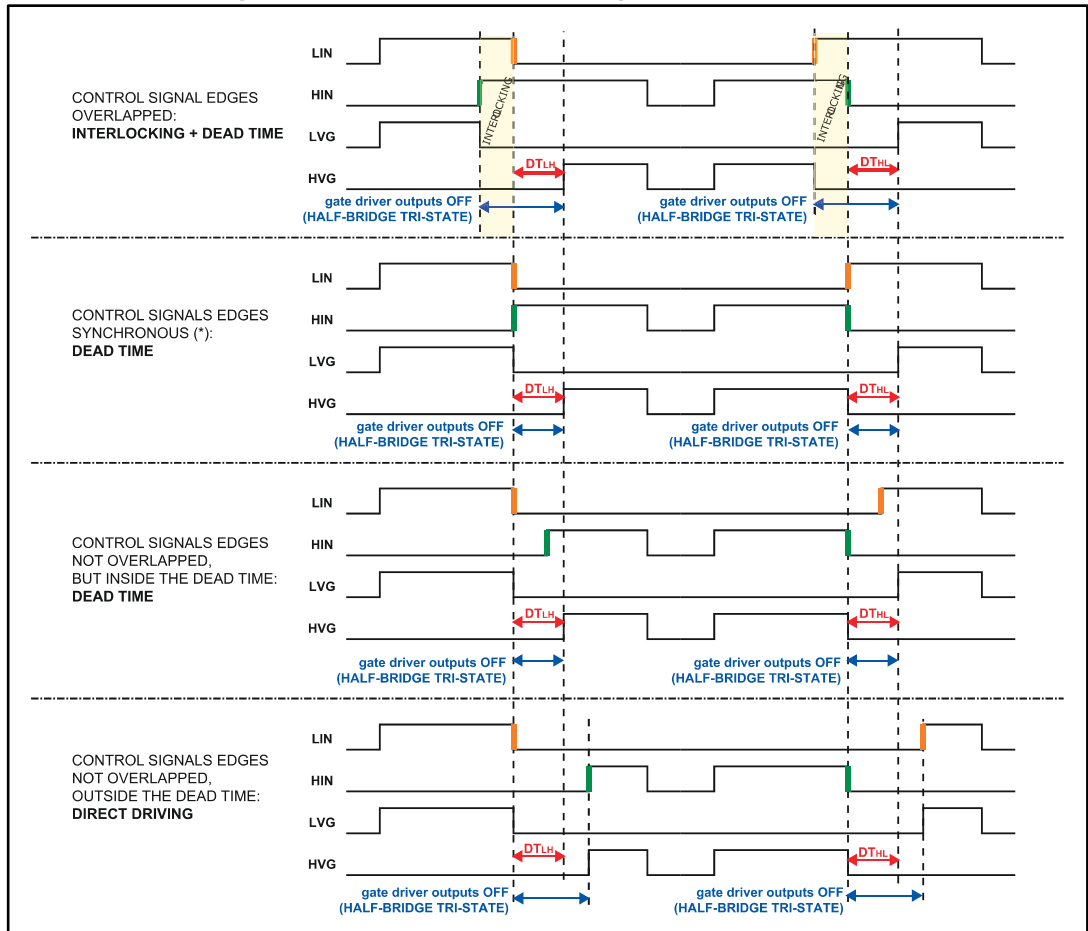
Table 14: Truth table

| Condition                                | Logic input ( $V_i$ ) |                  |                  | Output |     |
|--|-----------------------|------------------|------------------|--------|-----|
|  | $\overline{SD}$ /OD   | LIN              | HIN              | LVG    | HVG |
| Shutdown enable half-bridge tri-state    | L                     | X <sup>(1)</sup> | X <sup>(1)</sup> | L      | L   |
| Interlocking half-bridge tri-state       | H                     | H                | H                | L      | L   |
| 0 "logic state" half-bridge tri-state    | H                     | L                | L                | L      | L   |
| 1 "logic state" low side direct driving  | H                     | H                | L                | H      | L   |
| 1 "logic state" high side direct driving | H                     | L                | H                | L      | H   |

**Notes:**<sup>(1)</sup>X: don't care.

### 3.3 Waveform definitions

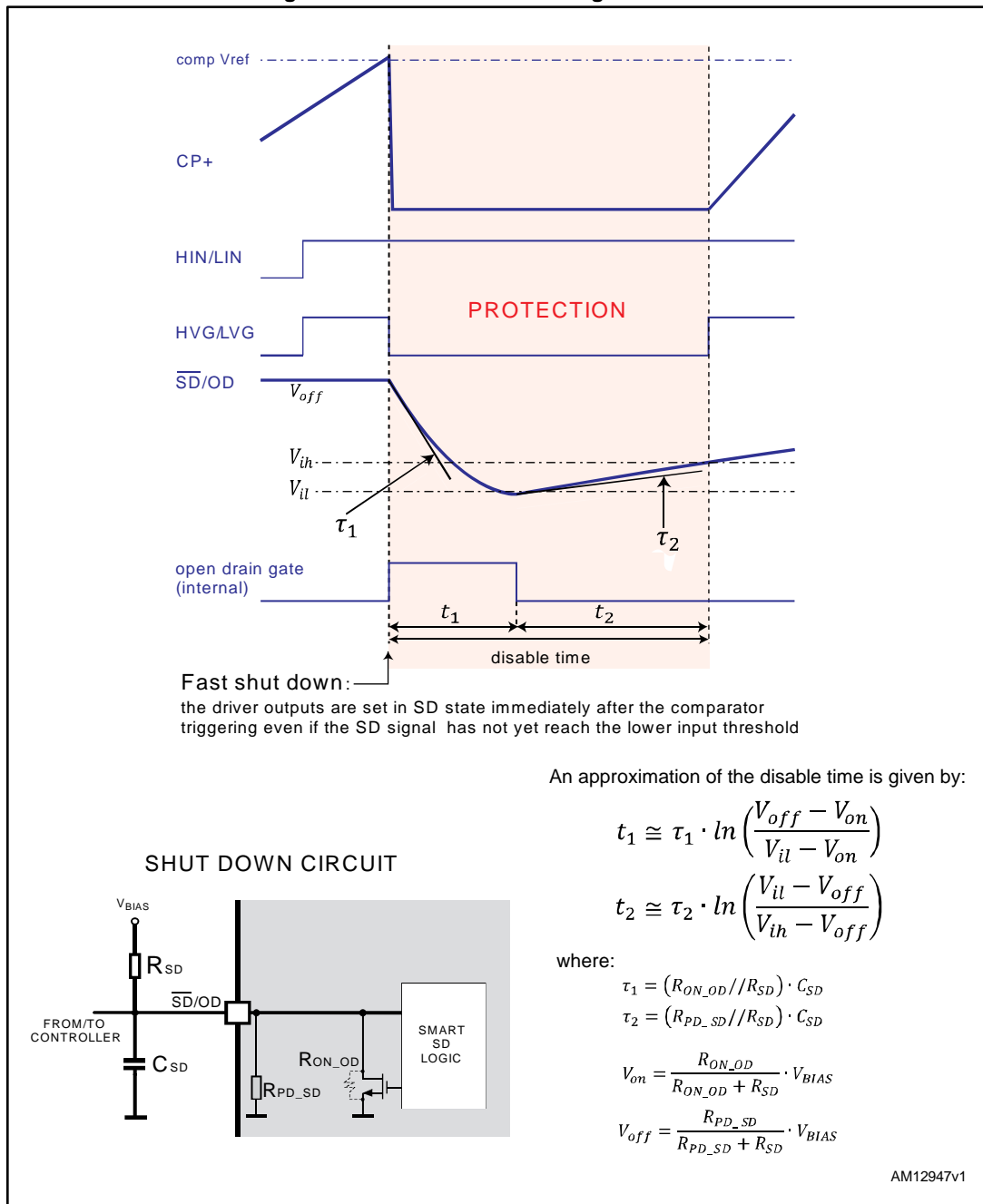
Figure 5: Dead time and interlocking waveform definitions



## 4 Smart shutdown function

The STGIPN3H60-H integrates a comparator for fault sensing purposes. The comparator has an internal voltage reference  $V_{REF}$  connected to the inverting input, while the noninverting input, available on pin (CIN), can be connected to an external shunt resistor in order to implement a simple over-current protection function. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low-level leading the halfbridge in tri-state. In the common overcurrent protection architectures the comparator output is usually connected to the shutdown input through a RC network, in order to provide a mono-stable circuit, which implements a protection time that follows the fault condition. Our smart shutdown architecture allows to immediately turn-off the output gate driver in case of overcurrent, the fault signal has a preferential path which directly switches off the outputs. The time delay between the fault and the outputs turn-off is no more dependent on the RC values of the external network connected to the shutdown pin. At the same time the DMOS connected to the open-drain output is turned on by the internal logic which holds it on until the shutdown voltage is lower than the logic input lower threshold ( $V_{il}$ ). Finally, the smart shutdown function provides the possibility to increase the real disable time without increasing the constant time of the external RC network.

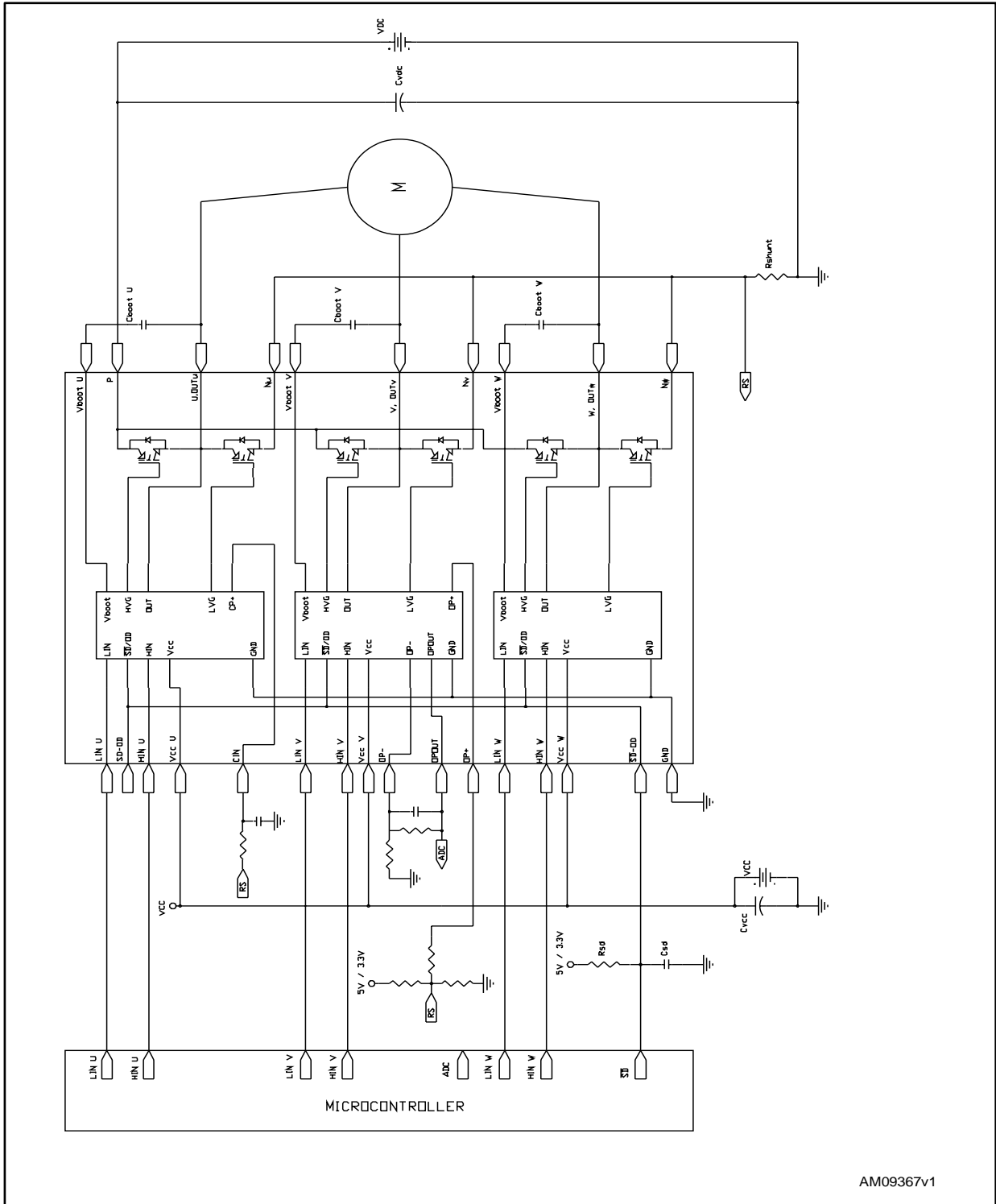
Figure 6: Smart shutdown timing waveforms



Please refer to [Table 13: "Sense comparator characteristics \(VCC = 15 V unless otherwise specified\)"](#) for internal propagation delay time details.

# 5 Application circuit example

Figure 7: Application circuit example



Application designers are free to use a different scheme according with the specifications of the device.



## 5.1 Guidelines

- Input signals HIN, LIN are active high logic. A 375 k $\Omega$  (typ.) pull down resistor is built-in for each input. If an external RC filter is used, for noise immunity, pay attention to the variation of the input signal level.
- To prevent input signal oscillation, the wiring of each input should be as short as possible.
- By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an opto-coupler is possible.
- Each capacitor should be located as close as possible to the pins of the IPM.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitors mounted close to the module pins will further improve performance.
- The  $\overline{\text{SD}}$  /OD signal should be pulled up to 5 V / 3.3 V with an external resistor (see [Section 4: "Smart shutdown function"](#) for detailed info).

These guidelines are useful for application design to ensure the specifications of the device. For further details, please refer to the relevant application note AN4043.

**Table 15: Recommended operating conditions**

| Symbol            | Parameter                          | Test conditions   | Min. | Typ. | Max. | Unit          |
|-------------------|------------------------------------|---|------|------|------|---------------|
| V <sub>PN</sub>   | Supply voltage                     | Applied between P-Nu, Nv, Nw  |      | 300  | 500  | V             |
| V <sub>CC</sub>   | Control supply voltage             | Applied between V <sub>CC</sub> -GND                                    | 13.5 | 15   | 18   | V             |
| V <sub>BS</sub>   | High side bias voltage             | Applied between V <sub>BOOTi</sub> -OUT <sub>i</sub><br>for i = U, V, W | 13   |      | 18   | V             |
| t <sub>dead</sub> | Blanking time to prevent Arm-short | For each input signal   | 1.5  |      |      | $\mu\text{s}$ |
| f <sub>PWM</sub>  | PWM input signal                   | -40°C < T <sub>c</sub> < 100 °C<br>-40°C < T <sub>j</sub> < 125 °C      |      |      | 25   | kHz           |
| T <sub>C</sub>    | Case operation temperature         |   |      |      | 100  | °C            |

## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 6.1 NDIP-26L type C package information

Figure 8: NDIP-26L type C package outline

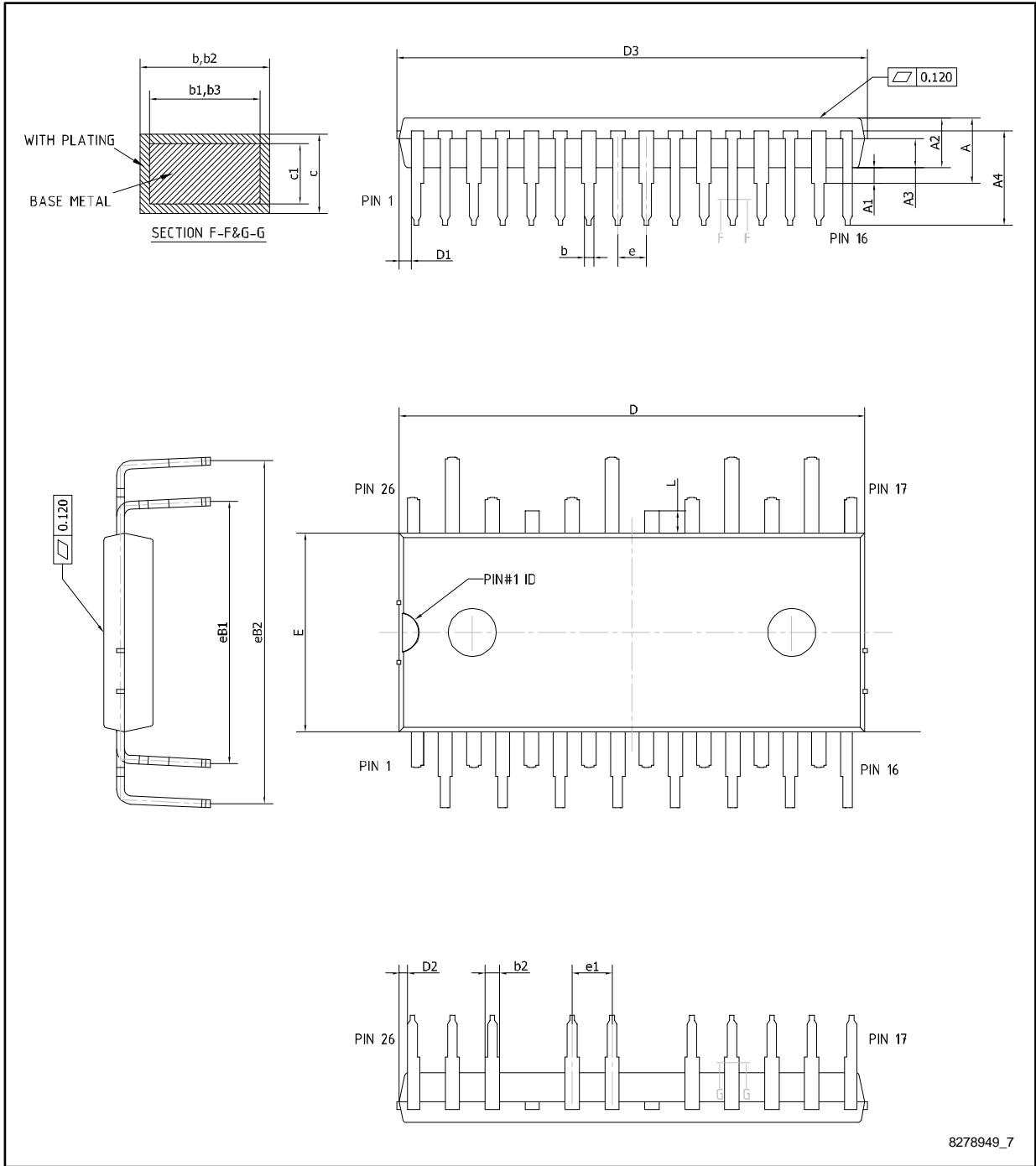


Table 16: NDIP-26L type C mechanical data

| Dim. | mm    |       |       |
|------|-------|-------|-------|
|      | Min.  | Typ.  | Max.  |
| A    |       |       | 4.40  |
| A1   | 0.80  | 1.00  | 1.20  |
| A2   | 3.00  | 3.10  | 3.20  |
| A3   | 1.70  | 1.80  | 1.90  |
| A4   | 5.70  | 5.90  | 6.10  |
| b    | 0.53  |       | 0.72  |
| b1   | 0.52  | 0.60  | 0.68  |
| b2   | 0.83  |       | 1.02  |
| b3   | 0.82  | 0.90  | 0.98  |
| c    | 0.46  |       | 0.59  |
| c1   | 0.45  | 0.50  | 0.55  |
| D    | 29.05 | 29.15 | 29.25 |
| D1   | 0.50  | 0.77  | 1.00  |
| D2   | 0.35  | 0.53  | 0.70  |
| D3   |       |       | 29.55 |
| E    | 12.35 | 12.45 | 12.55 |
| e    | 1.70  | 1.80  | 1.90  |
| e1   | 2.40  | 2.50  | 2.60  |
| eB1  | 16.10 | 16.40 | 16.70 |
| eB2  | 21.18 | 21.48 | 21.78 |
| L    | 1.24  | 1.39  | 1.54  |

## 6.2 NDIP-26L packing information

Figure 9: NDIP-26L tube dimensions (dimensions are in mm)

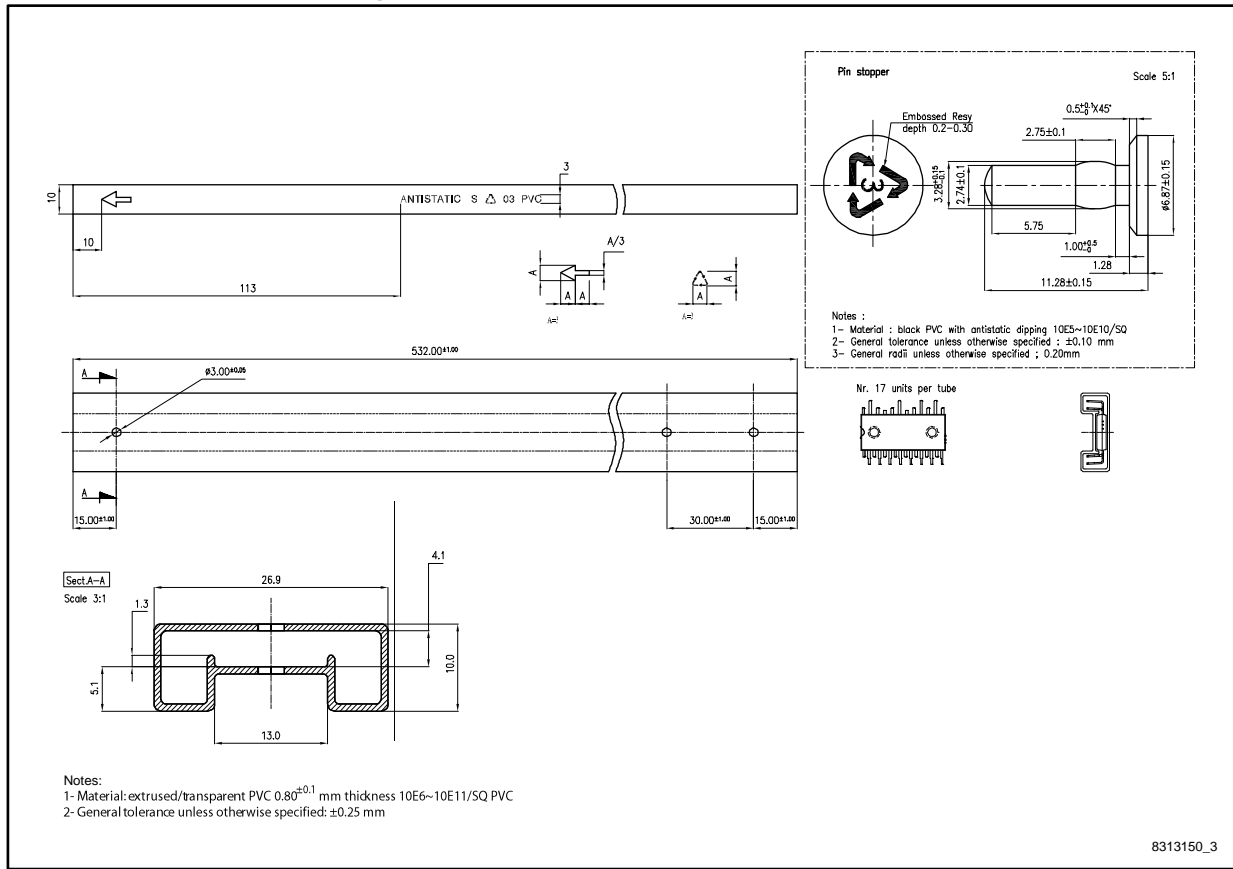


Table 17: Shipping details

| Parameter     | Value   |
|---------------|---------|
| Base quantity | 17 pcs  |
| Bulk quantity | 476 pcs |

## 7 Revision history

**Table 18: Document revision history**

| Date        | Revision | Changes   |
|-------------|----------|---|
| 15-Jan-2013 | 1        | Initial release.  |
| 02-May-2013 | 2        | Modified: <i>Figure 3 on page 8, Section 4 on page 14 and Figure 6 on page 15.</i>  |
| 14-Mar-2014 | 3        | Updated <i>Figure 3: Switching time test circuit, Table 9: Bootstrapped voltage (VCC = 15 V unless otherwise specified) and Table 10: Logic inputs (VCC = 15 V unless otherwise specified).</i><br>Updated <i>Section 6: Package mechanical data.</i> |
| 08-Sep-2016 | 4        | Updated <i>Section 6.1: "NDIP-26L type C package information" and Section 6.2: "NDIP-26L packing information"</i><br>Minor text changes   |

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