

SN74S1056

8-BIT SCHOTTKY BARRIER DIODE BUS-TERMINATION ARRAY

SDLS019B – APRIL 1990 – REVISED JULY 1997

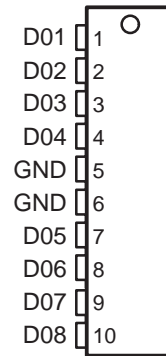
- Designed to Reduce Reflection Noise
- Repetitive Peak Forward Current 300 mA
- 8-Bit Array Structure Suited for Bus-Oriented Systems

description

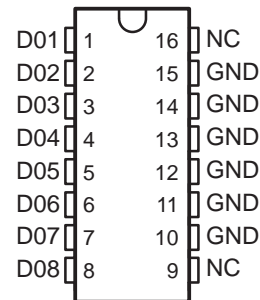
This Schottky barrier diode bus-termination array is designed to reduce reflection noise on memory bus lines. This device consists of an 8-bit high-speed Schottky diode array suitable for a clamp to GND.

The SN74S1056 is characterized for operation from 0°C to 70°C.

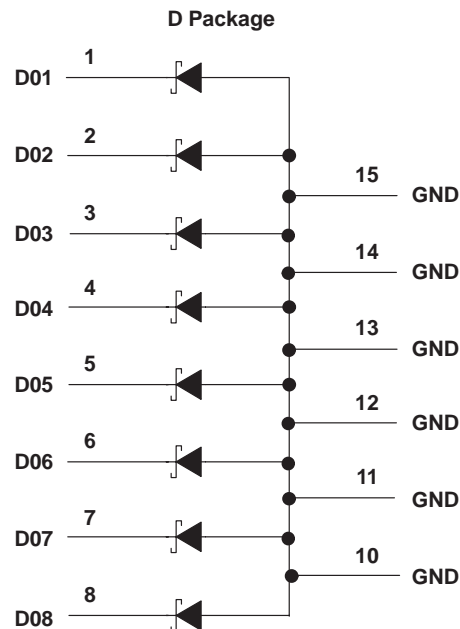
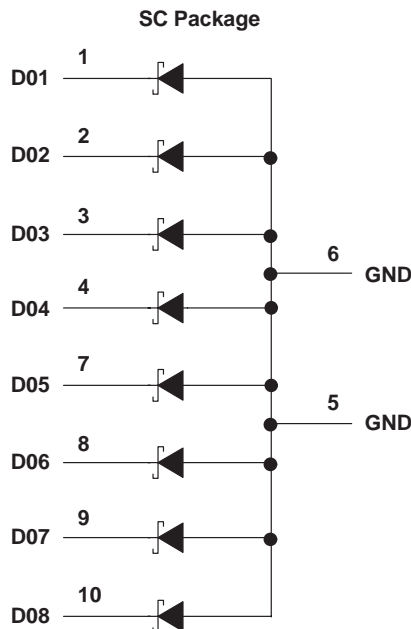
**SC PACKAGE
(TOP VIEW)**



**D PACKAGE
(TOP VIEW)**



schematic diagrams



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**TEXAS
INSTRUMENTS**

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BUS-TERMINATION ARRAY

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, V_R	7 V
Continuous forward current, I_F : Any D terminal from GND	50 mA
Total through all GND terminals	170 mA
Repetitive peak forward current, I_{FRM} (see Note 1): Any D terminal from GND	300 mA
Total through all GND terminals	1.2 A
Continuous total power dissipation at (or below) 25°C free-air temperature	1000 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: These values apply for $t_W \leq 100 \mu s$, duty cycle $\leq 20\%$.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 2)

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_R Static reverse current	$V_R = 7 V$			10	μA
V_F Static forward voltage	$I_F = 18 mA$		0.65	0.85	V
	$I_F = 50 mA$		0.8	1	
V_{FM} Peak forward voltage	$I_F = 300 mA$		1.41		V
C_t Total capacitance	$V_R = 0 V,$ $f = 1 MHz$		11	20	pF
	$V_R = 2 V,$ $f = 1 MHz$		8	16	

‡ All typical values are at $T_A = 25^\circ C$.

NOTE 2: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_x Internal crosstalk current	Total I_F current = 1.2 A, See Note 3		0.6	2	mA
	Total I_F current = 126 mA, See Note 3		0.01	0.1	

‡ All typical values are at $T_A = 25^\circ C$.

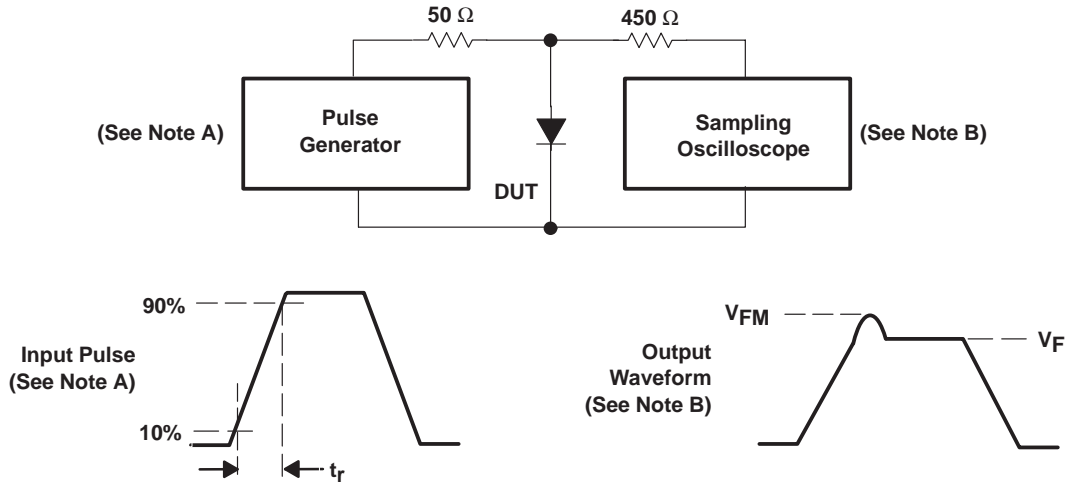
NOTE 3: I_x is measured under the following conditions with one diode static, all others switching:
 Switching diodes: $t_W = 100 \mu s$, duty cycle = 20%
 Static diode: $V_R = 5 V$
 The static diode input current is the internal crosstalk current I_x .

switching characteristics, $T_A = 25^\circ C$ (see Figures 1 and 2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{rr} Reverse recovery time	$I_F = 10 mA,$ $I_{RM(REC)} = 10 mA,$ $I_{R(REC)} = 1 mA,$ $R_L = 100 \Omega$		5	10	ns

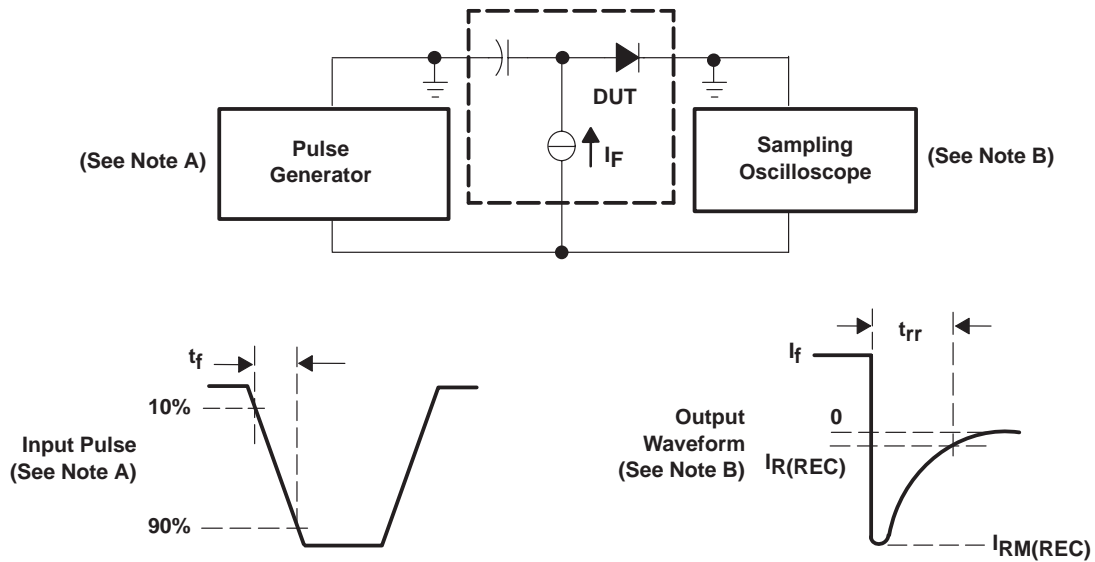


PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: $t_r = 20$ ns, $Z_O = 50$ Ω , freq = 500 Hz, duty cycle = 0.01.
 B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \leq 350$ ps, $R_i = 50$ Ω , $C_i = \leq 5$ pF.

Figure 1. Forward Recovery Voltage



- NOTES: A. The input pulse is supplied by a pulse generator having the following characteristics: $t_f = 0.5$ ns, $Z_O = 50$ Ω , $t_W = \geq 50$ ns, duty cycle = 0.01.
 B. The output waveform is monitored by an oscilloscope having the following characteristics: $t_r \leq 350$ ps, $R_i = 50$ Ω , $C_i = \leq 5$ pF.

Figure 2. Reverse Recovery Time

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APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74S1056 diode termination array helps suppress negative transients caused by transmission-line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver reduce negative transients, but they also can increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in the following figures. The diode conducts current when the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. A typical current versus voltage plot for the SN74S1056 is shown in Figure 3.

To illustrate how the diode arrays act to reduce negative transients at the end of a transmission line, the test setup in Figure 4(a) was evaluated. The resulting waveforms with and without the diode are shown in Figure 4(b).

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when the diode arrays are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes also can be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

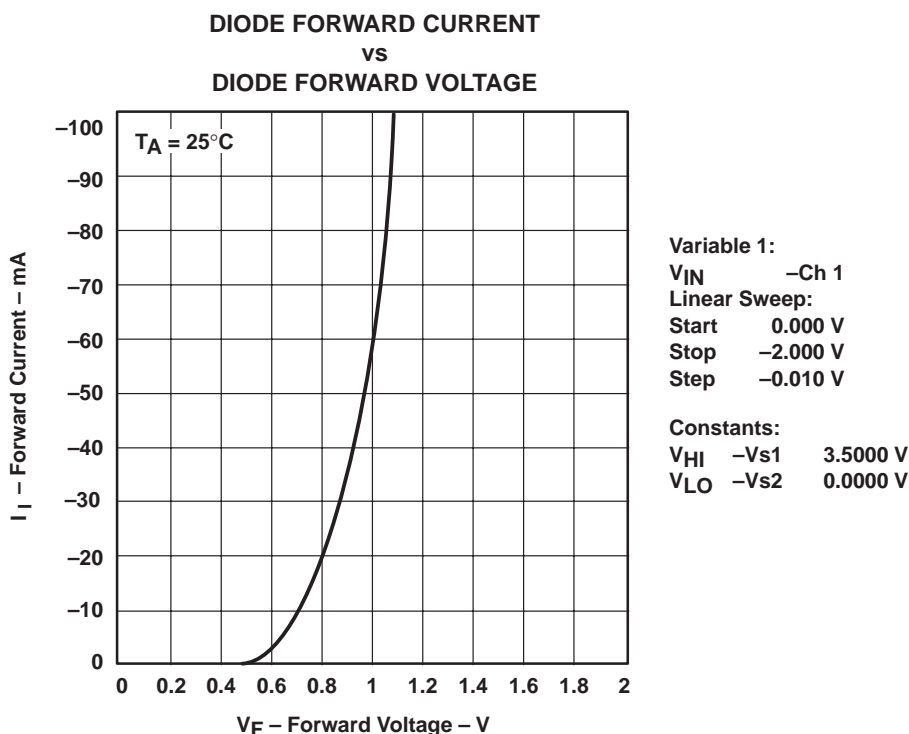


Figure 3. Current Versus Voltage for the SN74S1056

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74S1056D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74S1056DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70		
SN74S1056SC	OBSOLETE	SIP	SC	10		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

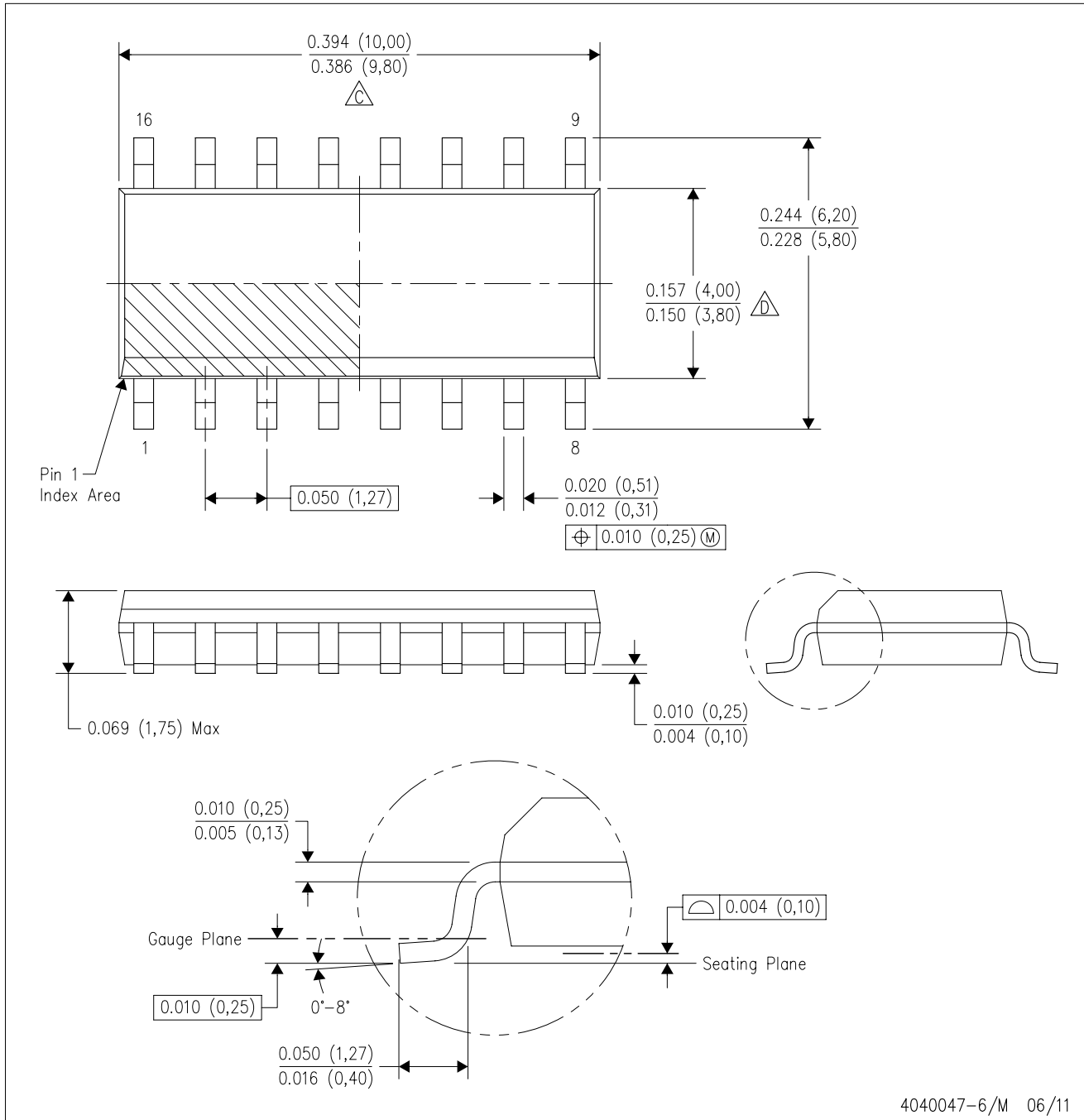
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

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