

IRF9630, IRF9631 IRF9632, IRF9633

Avalanche Energy Rated
P-Channel Power MOSFETs

August 1991

Features

- -5.5A and -6.5A, -150V and -200V
- $r_{DS(ON)} = 0.8\Omega$ and 1.2Ω
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

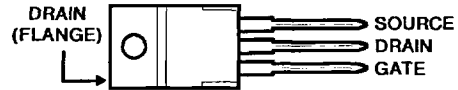
Description

The IRF9630, IRF9631, IRF9632 and IRF9633 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are p-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRF types are supplied in the JEDEC TO-220AB plastic package.

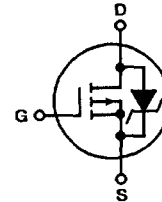
Package

TO-220AB
TOP VIEW



Terminal Diagram

P-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$) Unless Otherwise Specified

	IRF9630	IRF9631	IRF9632	IRF9633	UNITS
Drain-Source Voltage (1)	V_{DS} -200	-150	-200	-150	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$) (1)	V_{DGR} -200	-150	-200	-150	V
Continuous Drain Current					
$T_C = 25^\circ\text{C}$	I_D -6.5	-6.5	-5.5	-5.5	A
$T_C = 100^\circ\text{C}$	I_D -4.0	-4.0	-3.5	-3.5	A
Pulsed Drain Current (3)	I_{DM} -26	-26	-22	-22	A
Gate-Source Voltage	V_{GS} ± 20	± 20	± 20	± 20	V
Maximum Power Dissipation	P_D 75	75	75	75	W
(See Figure 14)					
Linear Derating Factor	0.6	0.6	0.6	0.6	W/ $^\circ\text{C}$
(See Figure 14)					
Single Pulse Avalanche Energy Rating (4)	E_{AS} 500	500	500	500	mJ
Operating and Storage Junction	T_J, T_{STG} -55 to +150	-55 to +150	-55 to +150	-55 to +150	$^\circ\text{C}$
Temperature Range					
Maximum Lead Temperature for Soldering	T_L 300	300	300	300	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)					

NOTES:

1. $T_J = +25^\circ\text{C}$ to $+150^\circ\text{C}$
2. Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$
3. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
4. $V_{DD} = 50\text{V}$, Start $T_J = +25^\circ\text{C}$, $L = 17.55\text{mH}$, $R_G = 25\Omega$, Peak $I_L = 6.5\text{A}$ (See Figures 15 and 16)

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**P-CHANNEL
POWER MOSFETs**

Specifications IRF9630, IRF9631, IRF9632, IRF9633

Electrical Characteristics $T_C = +25^\circ\text{C}$, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Drain-Source Breakdown Voltage IRF9630, IRF9632 IRF9631, IRF9633	BV _{DSS}	V _{GS} = 0V, I _D = -250 μ A	-200	-	-	V
			-150	-	-	V
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = -250 μ A	-2.0	-	-4.0	V
Gate-Source Leakage Forward	I _{GSS}	V _{GS} = -20V	-	-	-500	nA
Gate-Source Leakage Reverse	I _{GSS}	V _{GS} = 20V	-	-	500	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = Max Rating, V _{GS} = 0V	-	-	-250	μ A
		V _{DS} = Max Rating x 0.8, V _{GS} = 0V, T _C = +125 $^\circ$ C	-	-	-1000	μ A
On-State Drain Current (Note 2) IRF9630, IRF9631 IRF9632, IRF9633	I _{D(ON)}	V _{DS} > I _{D(ON)} x r _{DS(ON)} Max, V _{GS} = -10V	-6.5	-	-	A
			-5.5	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRF9630, IRF9631 IRF9632, IRF9633	r _{DS(ON)}	V _{GS} = -10V, I _D = -3.5A	-	0.5	0.8	Ω
			-	0.8	1.2	Ω
Forward Transconductance (Note 2)	g _{fs}	V _{DS} > I _{D(ON)} x r _{DS(ON)} Max, I _D = 3.5A	2.2	3.5	-	S(Ω)
Input Capacitance	C _{ISS}	V _{GS} = 0V, V _{DS} = -25V, f = 1.0MHz See Figure 10	-	550	-	pF
Output Capacitance	C _{OSS}		-	170	-	pF
Reverse Transfer Capacitance	C _{RSS}		-	50	-	pF
Turn-On Delay Time	t _{d(ON)}	V _{DD} = 0.5 BV _{DSS} , I _D = -6.5A, R _G = 50 Ω See Figure 17. (MOSFET switching times are essentially independent of operating temperature.)	-	30	50	ns
Rise Time	t _r		-	50	100	ns
Turn-Off Delay Time	t _{d(OFF)}		-	50	100	ns
Fall Time	t _f		-	40	80	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q _g	V _{GS} = -10V, I _D = -6.5A, V _{DS} = 0.8 Max Rating. See Figure 18 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	31	45	nC
Gate-Source Charge	Q _{gs}		-	18	-	nC
Gate-Drain ("Miller") Charge	Q _{gd}		-	13	-	nC
Internal Drain Inductance	L _D	Measured from the contact screw on tab to center of die.	-	3.5	-	nH
		Measured from the drain lead, 6mm (0.25") from pkg. to center of die.	-	4.5	-	nH
Internal Source Inductance	L _S	Measured from the source lead, 6mm (0.25") from pkg. to source bonding pad.	-	7.5	-	nH
Junction-to-Case	R _{0JC}		-	-	1.67	$^\circ\text{C}/\text{W}$
Case-to-Sink	R _{0CS}	Mounting surface flat, smooth and greased	-	1.0	-	$^\circ\text{C}/\text{W}$
Junction-to-Ambient	R _{0JA}	Typical socket mount	-	-	80	$^\circ\text{C}/\text{W}$

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I _S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier.	-	-	-6.5	A
Pulse Source Current (Body Diode) (Note 3)	I _{SM}		-	-	-26	A
Diode Forward Voltage (Note 2)	V _{SD}	T _C = +25 $^\circ\text{C}$, I _S = -6.5A, V _{GS} = 0V	-	-	-1.5	V
Reverse Recovery Time	t _{rr}	T _J = +150 $^\circ\text{C}$, I _F = -6.5A, dI _F /dt = 100A/ μ s	-	400	-	ns
Reverse Recovered Charge	Q _{RR}	T _J = +150 $^\circ\text{C}$, I _F = -6.5A, dI _F /dt = 100A/ μ s	-	2.6	-	μ C
Forward Turn-on Time	t _{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .	-	-	-	-

NOTES: 1. T_J = +25 $^\circ\text{C}$ to +150 $^\circ\text{C}$
2. Pulse Test: Pulse width \leq 300 μ s,
Duty Cycle \leq 2%

3. Repetitive Rating: Pulse width limited by max.
junction temperature. See Transient Thermal
Impedance Curve (Figure 5)

4. V_{DD} = 50V, Start T_J = +25 $^\circ\text{C}$, L = 17.75mH,
R_G = 25 Ω , Peak I_L = 6.5A (See Figures 15
and 16)

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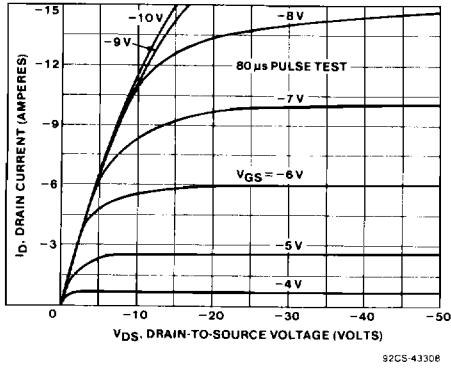


Fig. 1 - Typical output characteristics.

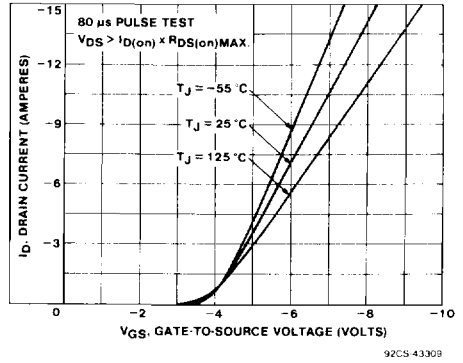


Fig. 2 - Typical transfer characteristics.

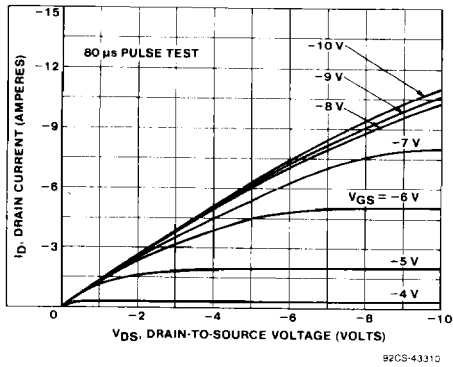


Fig. 3 - Typical saturation characteristics.

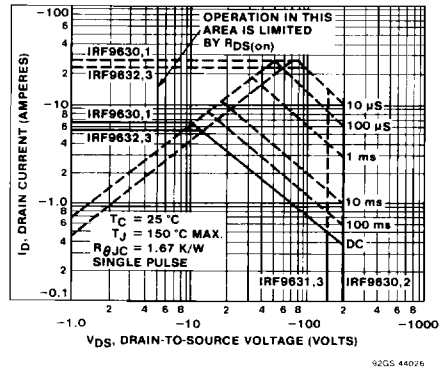


Fig. 4 - Maximum safe operating area.

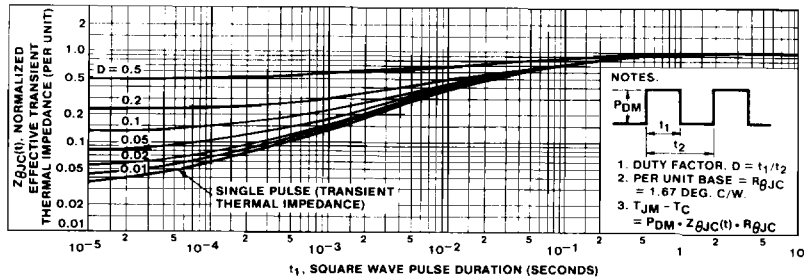


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

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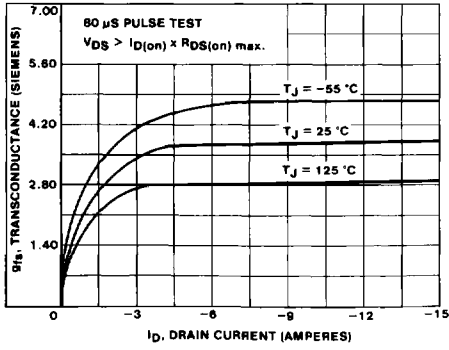


Fig. 6 - Typical transconductance vs. drain current.

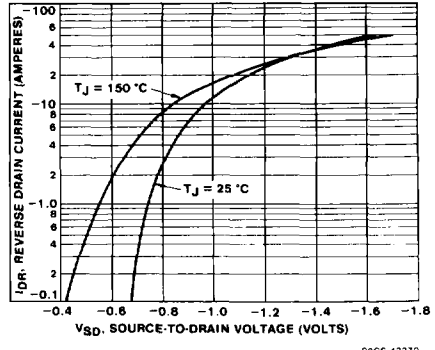


Fig. 7 - Typical source-drain diode forward voltage.

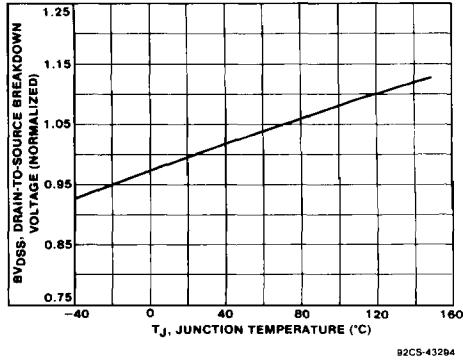


Fig. 8 - Breakdown voltage vs. temperature.

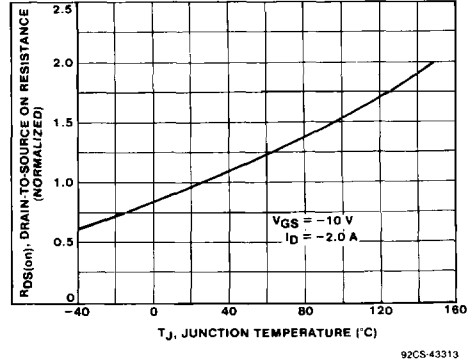


Fig. 9 - Normalized on-resistance vs. temperature.

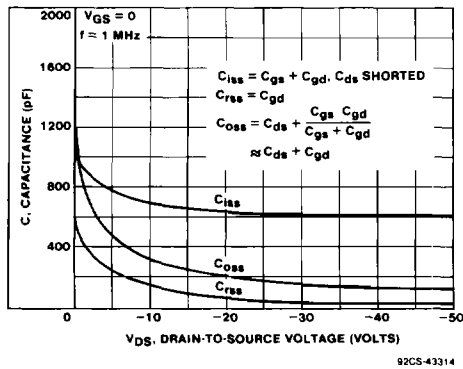


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

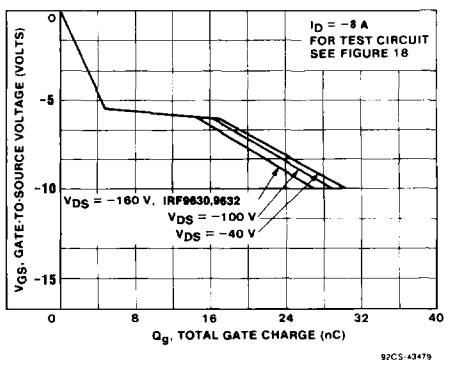


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

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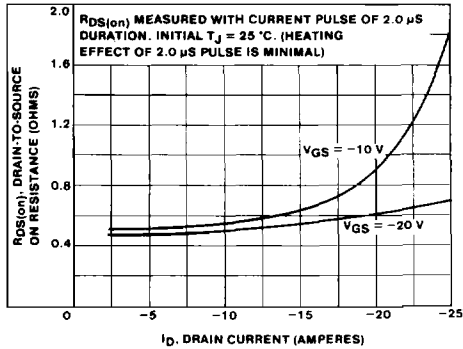


Fig. 12 - Typical on-resistance vs. drain current.

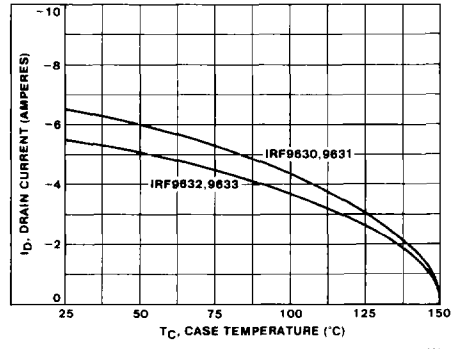


Fig. 13 - Maximum drain current vs. case temperature.

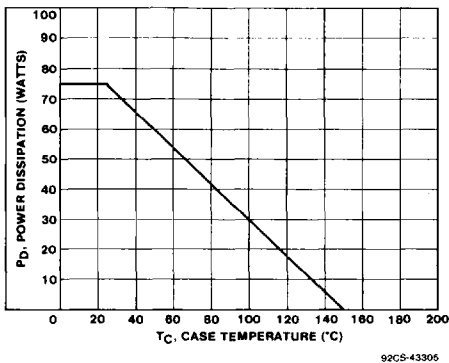


Fig. 14 - Power vs. temperature derating curve.

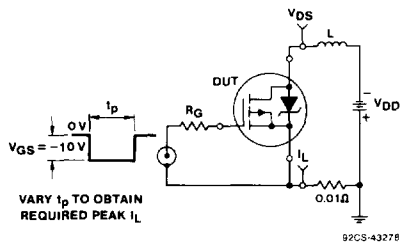


Fig. 15 - Unclamped inductive test circuit.

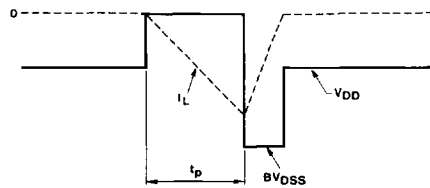


Fig. 16 - Unclamped inductive waveforms.

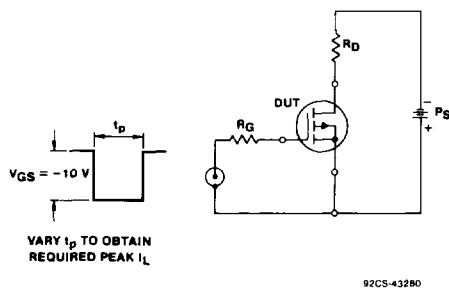


Fig. 17 - Switching time test circuit.

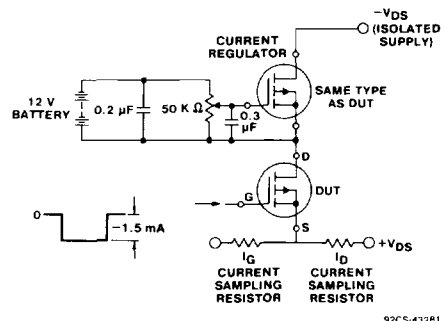


Fig. 18 - Gate charge test circuit.

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