



## SD1731 (TH562)

### RF POWER BIPOLAR TRANSISTORS HF SSB APPLICATIONS

#### FEATURES SUMMARY

- OPTIMIZED FOR SSB
- 30 MHz
- 50 VOLTS
- EFFICIENCY 40%
- COMMON EMITTER
- GOLD METALLIZATION
- $P_{OUT} = 220$  W PEP WITH 13 dB GAIN

#### DESCRIPTION

The SD1731 is a 50 V epitaxial silicon NPN planar transistor designed primarily for SSB communications. This device utilizes emitter ballasting for improved ruggedness and reliability.

Figure 1. Package

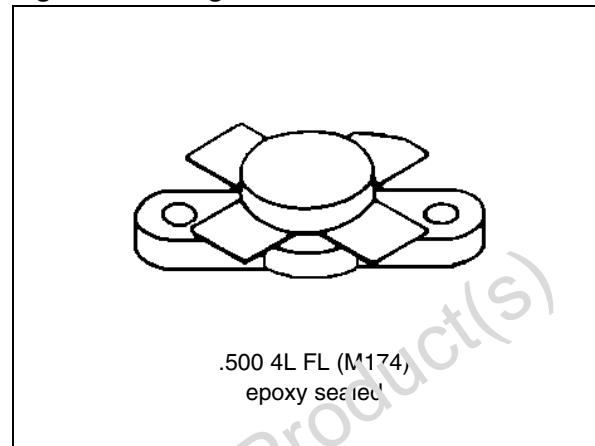


Figure 2. Pin Connection

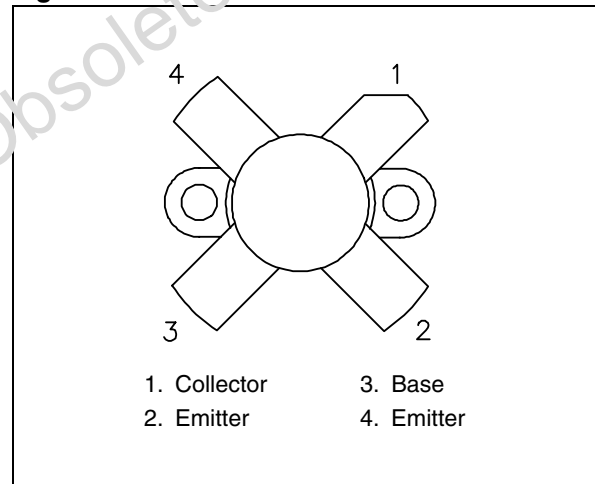


Table 1. Order Codes

Order Codes	Marking	Package	Packaging
SD1731 (TH562)	SD1731	M174	PLASTIC TRAYS

## SD1731 (TH562)

**Table 2. Absolute Maximum Ratings ( $T_{\text{case}} = 25^{\circ}\text{C}$ )**

Symbol	Parameter	Value	Unit
$V_{\text{CBO}}$	Collector-Base Voltage	110	V
$V_{\text{CEO}}$	Collector-Emitter Voltage	55	V
$V_{\text{EBO}}$	Emitter-Base Voltage	4.0	V
$I_{\text{C}}$	Device Current	20	A
$P_{\text{DISS}}$	Power Dissipation ( $T_{\text{heatsink}} \leq 25^{\circ}\text{C}$ )	233	W
$T_{\text{J}}$	Junction Temperature	+200	$^{\circ}\text{C}$
$T_{\text{STG}}$	Storage Temperature	- 65 to +150	$^{\circ}\text{C}$

**Table 3. Thermal Data**

Symbol	Parameter	Value	Unit
$R_{\text{TH(j-c)}}$	Junction-Case Thermal Resistance	0.55	$^{\circ}\text{C/W}$
$R_{\text{TH(c-s)}}$	Case-Heatsink Thermal Resistance	0.2	$^{\circ}\text{C/W}$

## ELECTRICAL SPECIFICATIONS

**Table 4. Static ( $T_{\text{case}} = 25^{\circ}\text{C}$ )**

Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
$BV_{\text{CBO}}$	$I_{\text{C}} = 200 \text{ mA}; I_{\text{E}} = 0 \text{ mA}$	110	—	—	V
$BV_{\text{CEO}}$	$I_{\text{C}} = 200 \text{ mA}; I_{\text{B}} = 0 \text{ mA}$	55	—	—	V
$BV_{\text{EBO}}$	$I_{\text{E}} = 20 \text{ mA}; I_{\text{C}} = 0 \text{ mA}$	4.0	—	—	V
$I_{\text{CEO}}$	$V_{\text{CE}} = 30 \text{ V}; I_{\text{E}} = 0 \text{ mA}$	—	—	5	mA
$I_{\text{CES}}$	$V_{\text{CE}} = 55 \text{ V}; I_{\text{E}} = 0 \text{ mA}$	—	—	10	mA
$h_{\text{FE}}$	$V_{\text{CE}} = 6 \text{ V}; I_{\text{C}} = 10 \text{ A}$	15	—	80	—

**Table 5. Dynamic ( $T_{\text{heatsink}} = 25^{\circ}\text{C}$ )**

Symbol	Test Conditions	Value			Unit
		Min.	Typ.	Max.	
$P_{\text{OUT}}$	$f = 30 \text{ MHz}; V_{\text{CE}} = 50 \text{ V}; I_{\text{CQ}} = 150 \text{ mA}$	220	—	—	W
$G_{\text{P}}^{(1)}$	$P_{\text{OUT}} = 220 \text{ W PEP}; V_{\text{CE}} = 50 \text{ V}; I_{\text{CQ}} = 150 \text{ mA}$	13	—	—	dB
$\text{IMD}^{(1)}$	$P_{\text{OUT}} = 220 \text{ W PEP}; V_{\text{CE}} = 50 \text{ V}; I_{\text{CQ}} = 150 \text{ mA}$	—	—	-30	dBc
$\eta_{\text{c}}^{(1)}$	$P_{\text{OUT}} = 220 \text{ W PEP}; V_{\text{CE}} = 50 \text{ V}; I_{\text{CQ}} = 150 \text{ mA}$	40	—	—	%
$C_{\text{OB}}$	$f = 1 \text{ MHz}; V_{\text{CB}} = 50 \text{ V}$	—	330	—	pF

Note: 1.  $f_1 = 30.00 \text{ MHz}, f_2 = 30.001 \text{ MHz}$

## TYPICAL PERFORMANCE

Figure 3. Power Output PEP vs Power Input

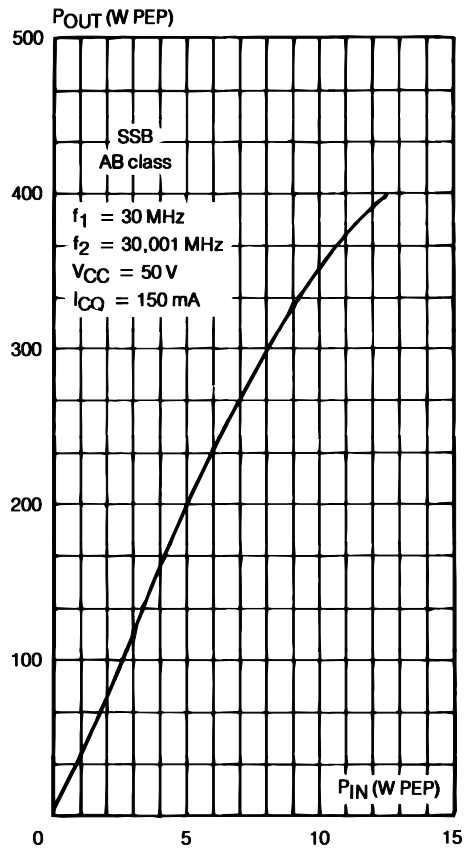


Figure 4. Collector Efficiency vs Power Output PEP

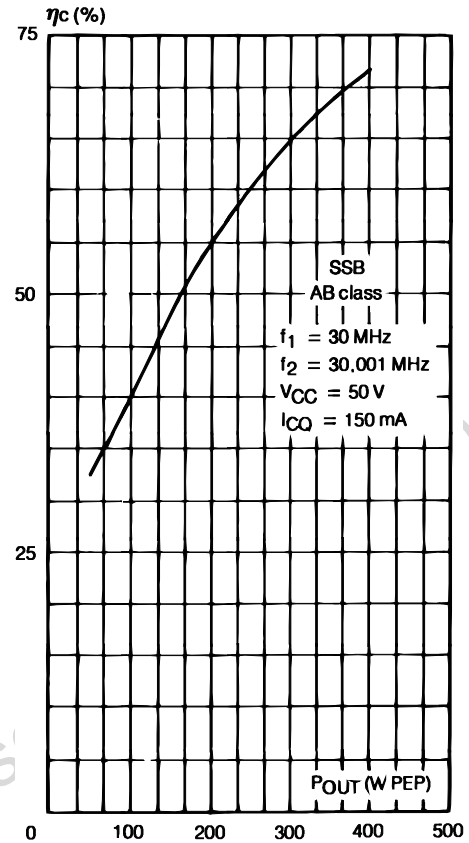


Figure 5. Intermodulation Distortion vs Power Output PEP

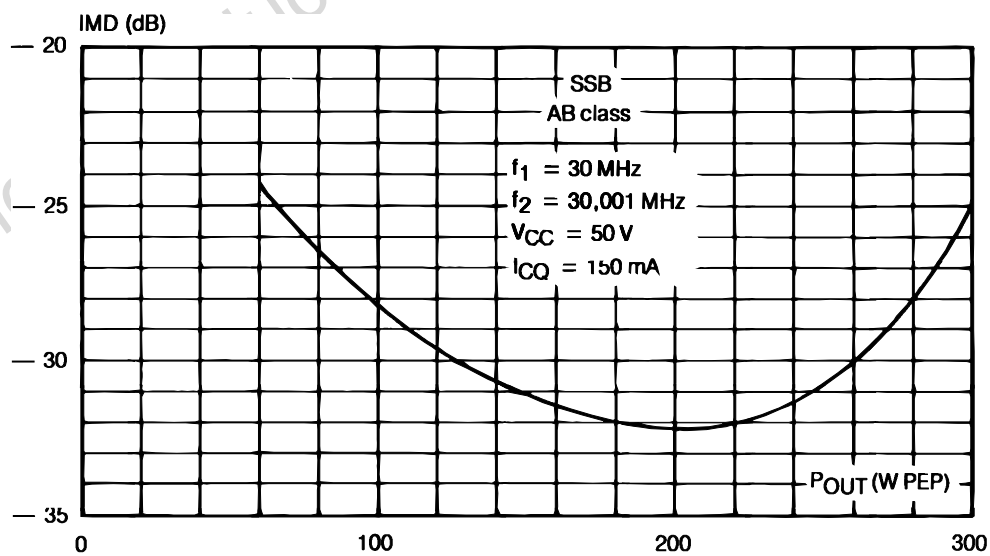


Figure 6. Power Gain vs Power Output PEP

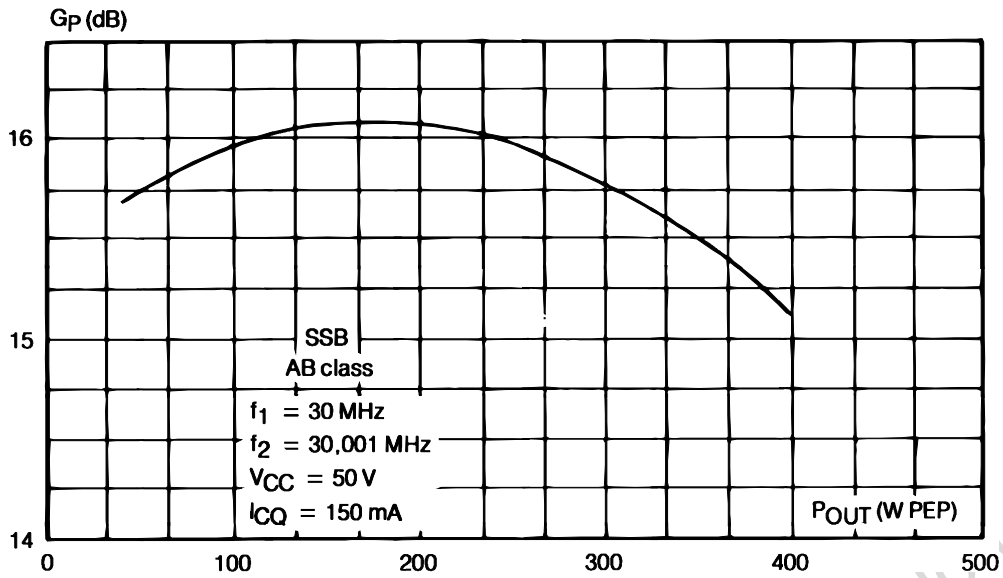
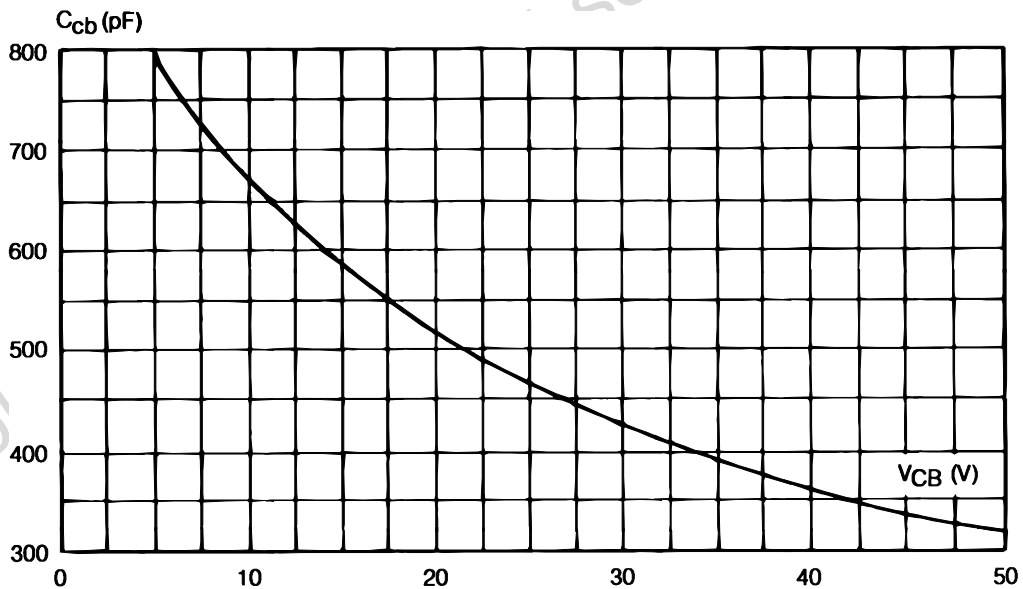


Figure 7. Collector Base Capacitance vs Collector Emitter Voltage



## TEST CIRCUIT

Figure 8. Test Circuit

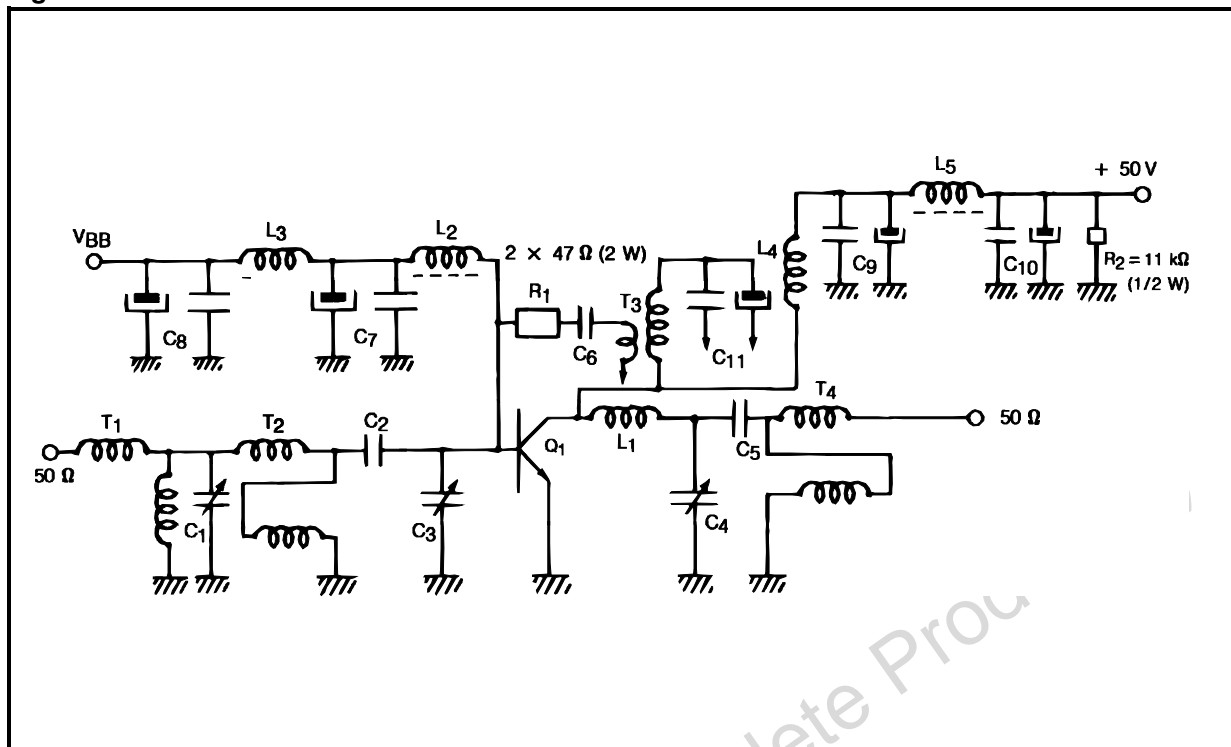
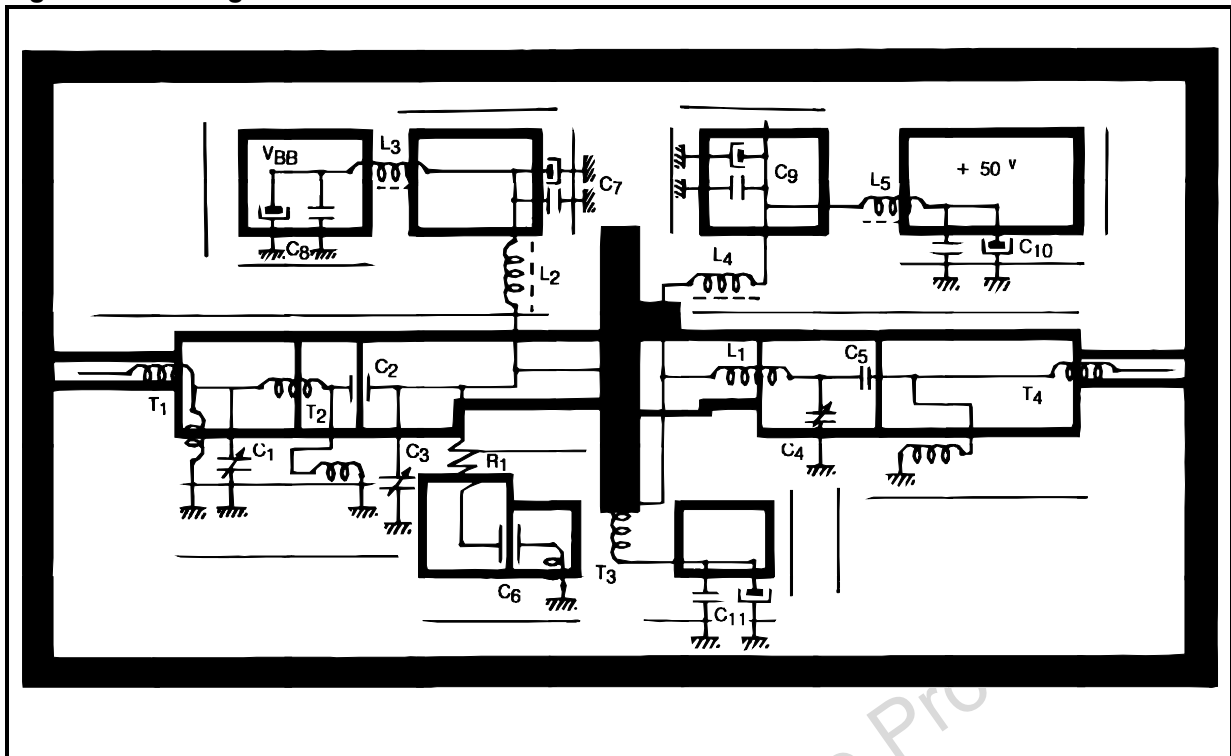


Table 6. Test Circuit

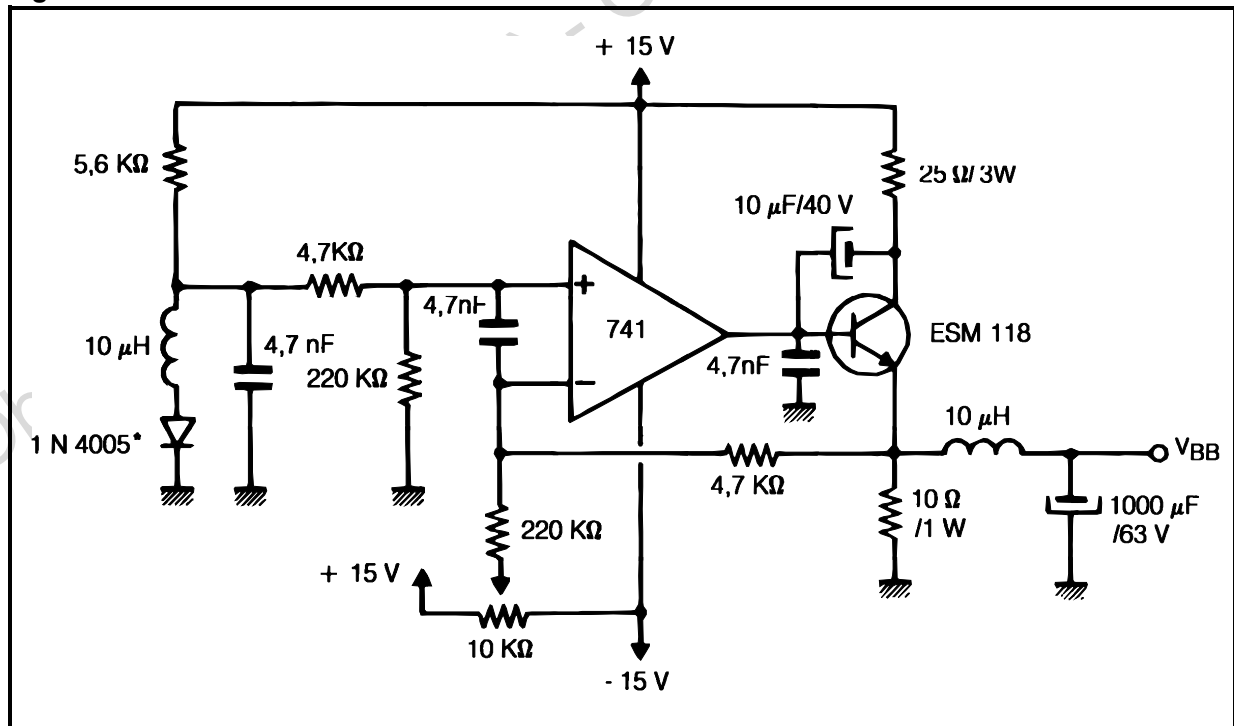
C1	Arco 426 + 220pF + 330pF Chips
C2	2 x 10nF Chips
C3	Arco 4615 + 2.2nF + 2 x 1nF LCC + 4.7nF + 560pf Chps
C4	Arco 4213 + 330pF Chip
C5	10nF Chip
C6	3 x 10nF Chips
C7, C8, C9, C10, C11	1nF + 10nF + 100nF + 4.7μF, 63V + 100μF, 63V
L1	3 Turns of 1.2mm Unenameled Wire Diameter, 7.1mm, Length 13mm
L2, L3	8 Turns of 0.55mm Enameled Wire on Ferrite Core Phillips 4C6 97170 (9 x 6 x 3)
L4	10 Turns of 1.2mm Enameled Wire, Diameter 8.1mm, Length 20mm
L5	7 Turns of 1.2mm Enameled Wire on Ferrite Core Phillips 4C6 97180
T1	6:3.5 Impedance Transformer on toriod Phillips 4C6 97180
T2	Twisted Pair 4:1 Transformer, 4 Turns Made with 1.0mm Enameled on toriod Phillips 4C6 97180
T3	Feedback Transformer Primary: 2 Turns of 1mm Enameled Wire Secondary: 8 Turns of 1mm Enameled Wire
T4	Twisted Pair 4:1 Transformer, 4 Turns of bifilar Twisted 1.2mm Wires on Ferrite Core Phillips 4C6 97200

Figure 9. Mounting Circuit



BIAS CIRCUIT

Figure 10. Bias Circuit

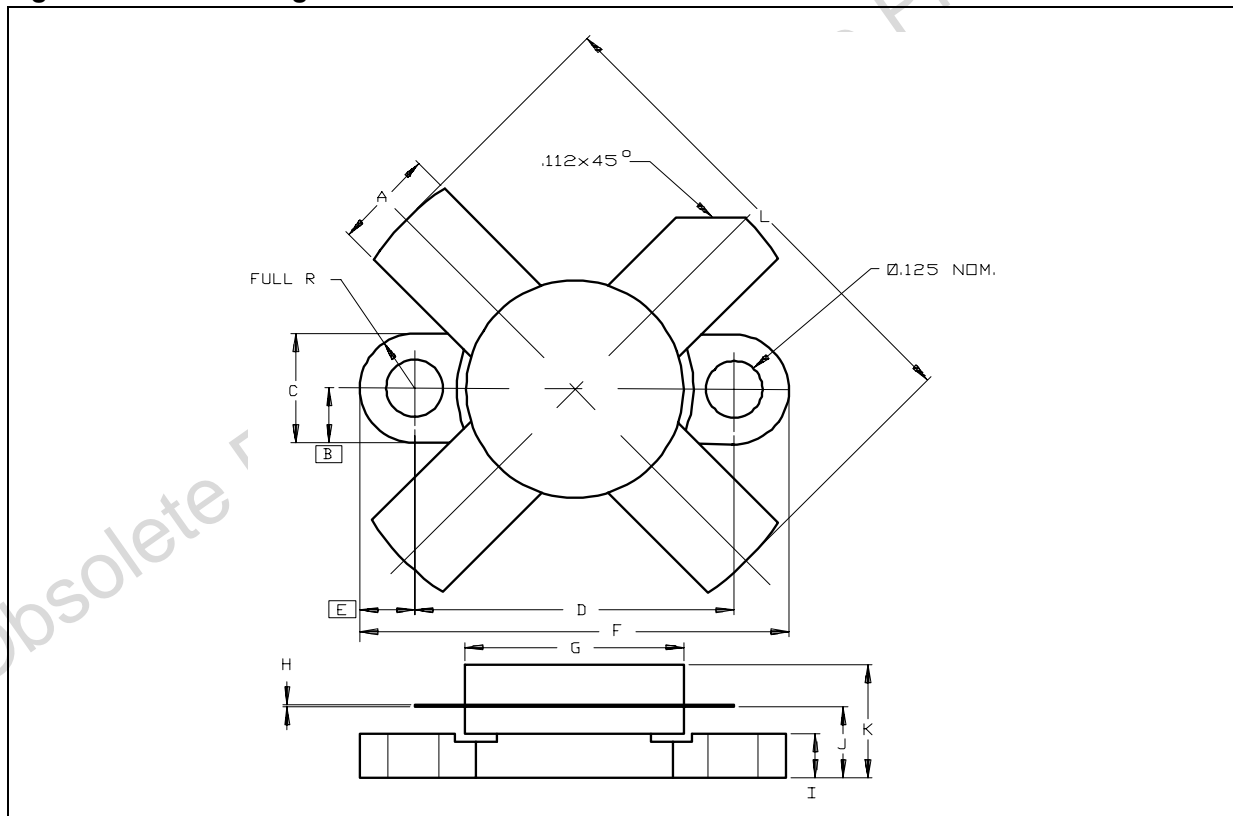


## PACKAGE MECHANICAL

Table 7. M174 Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	5.59		5.84	0.220		0.230
B		3.18			0.125	
C	6.22		6.48	0.245		0.255
D	18.28		18.54	0.720		0.730
E		3.18			0.125	
F	24.64		24.89	0.970		0.980
G	12.57		12.83	0.495		0.505
H	0.08		0.18	0.003		0.007
I	2.29		2.79	0.090		0.110
J	4.06		4.45	0.160		0.175
K			7.11			0.280
L			26.67			1.050

Figure 11. M174 Package Dimensions



Note: Drawing is not to scale.

**REVISION HISTORY**

**Table 8. Revision History**

Date	Revision	Description of Changes
July-1995	1	First Issue
8-June-2004	2	Stylesheet update. No content change.

Obsolete Product(s) - Obsolete Product(s)



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