

## 100351 Low Power Hex D Flip-Flop

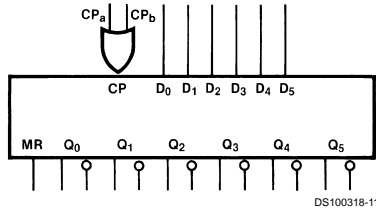
### General Description

The 100351 contains six D-type edge-triggered, master/slave flip-flops with true and complement outputs, a pair of common Clock inputs ( $CP_a$  and  $CP_b$ ) and common Master Reset (MR) input. Data enters a master when both  $CP_a$  and  $CP_b$  are LOW and transfers to the slave when  $CP_a$  and  $CP_b$  (or both) go HIGH. The MR input overrides all other inputs and makes the Q outputs LOW. All inputs have 50 k $\Omega$  pull-down resistors.

### Features

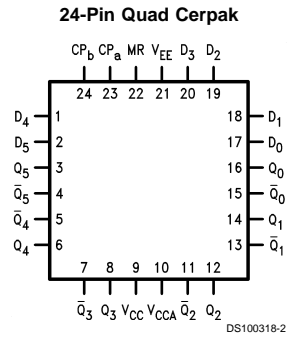
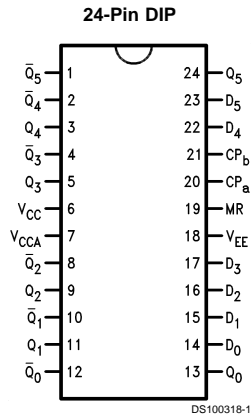
- 40% power reduction of the 100151
- 2000V ESD protection
- Pin/function compatible with 100151
- Voltage compensated operating range: -4.2V to -5.7V
- Standard Microcircuit Drawing (SMD) 5962-9457901

### Logic Symbol

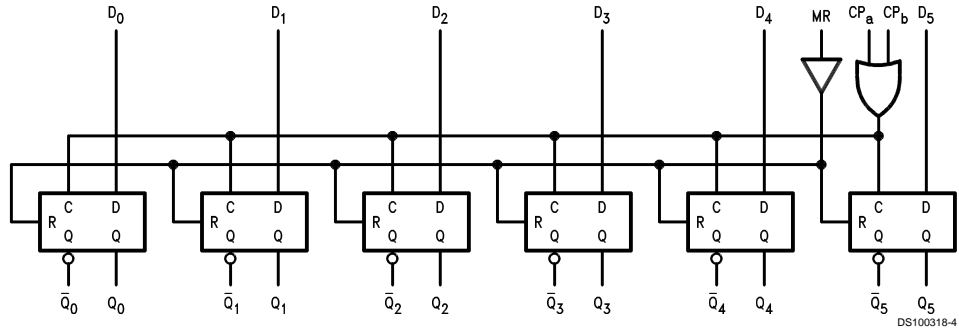


Pin Names	Description
$D_0$ – $D_5$	Data Inputs
$CP_a$ , $CP_b$	Common Clock Inputs
MR	Asynchronous Master Reset Input
$Q_0$ – $Q_5$	Data Outputs
$\bar{Q}_0$ – $\bar{Q}_5$	Complementary Data Outputs

## Connection Diagrams



## Logic Diagram



## Truth Tables (Each Flip-flop)

### Synchronous Operation

Inputs				Outputs
D <sub>n</sub>	CP <sub>a</sub>	CP <sub>b</sub>	MR	Q <sub>n</sub> (t+1)
L	↗	L	L	L
H	↗	L	L	H
L	L	↗	L	L
H	L	↗	L	H
X	H	↗	L	Q <sub>n</sub> (t)
X	↗	H	L	Q <sub>n</sub> (t)
X	L	L	L	Q <sub>n</sub> (t)

### Asynchronous Operation

Inputs				Outputs
D <sub>n</sub>	CP <sub>a</sub>	CP <sub>b</sub>	MR	Q <sub>n</sub> (t+1)
X	X	X	H	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care  
 t = Time before CP positive transition  
 t+1 = Time after CP positive transition  
 ↗ = LOW-to-HIGH transition

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Above which the useful life may be impaired

Storage Temperature (T <sub>STG</sub> )	-65°C to +150°C
Maximum Junction Temperature (T <sub>J</sub> )	
Ceramic	+175°C
V <sub>EE</sub> Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	V <sub>EE</sub> to +0.5V
Output Current (DC Output HIGH)	-50 mA

ESD (Note 2)

≥2000V

## Recommended Operating Conditions

Case Temperature (T <sub>C</sub> )	
Military	-55°C to +125°C
Supply Voltage (V <sub>EE</sub> )	-5.7V to -4.2V

**Note 1:** Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

## Military Version

### DC Electrical Characteristics

V<sub>EE</sub> = -4.2V to -5.7V, V<sub>CC</sub> = V<sub>CCA</sub> = GND, T<sub>C</sub> = -55°C to +125°C

Symbol	Parameter	Min	Max	Units	T <sub>C</sub>	Conditions	Notes	
V <sub>OH</sub>	Output HIGH Voltage	-1025	-870	mV	0°C to +125°C	V <sub>IN</sub> = V <sub>IH</sub> (Max) or V <sub>IL</sub> (Min)	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1085	-870	mV	-55°C			
V <sub>OL</sub>	Output LOW Voltage	-1830	-1620	mV	0°C to +125°C			
		-1830	-1555	mV	-55°C			
V <sub>OHc</sub>	Output HIGH Voltage	-1035		mV	0°C to +125°C	V <sub>IN</sub> = V <sub>IH</sub> (Min) or V <sub>IL</sub> (Max)	Loading with 50Ω to -2.0V	(Notes 3, 4, 5)
		-1085		mV	-55°C			
V <sub>OLc</sub>	Output LOW Voltage		-1610	mV	0°C to +125°C			
			-1555	mV	-55°C			
V <sub>IH</sub>	Input HIGH Voltage	-1165	-870	mV	-55°C to +125°C	Guaranteed HIGH Signal for All Inputs	(Notes 3, 4, 5, 6)	
V <sub>IL</sub>	Input LOW Voltage	-1830	-1475	mV	-55°C to +125°C	Guaranteed LOW Signal for All Inputs	(Notes 3, 4, 5, 6)	
I <sub>IL</sub>	Input LOW Current	0.50		μA	-55°C to +125°C	V <sub>EE</sub> = -4.2V V <sub>IN</sub> = V <sub>IL</sub> (Min)	(Notes 3, 4, 5)	
I <sub>IH</sub>	Input HIGH Current	CP, MR D <sub>0</sub> -D <sub>5</sub>	350	μA	0°C to +125°C	V <sub>EE</sub> = -5.7V V <sub>IN</sub> = V <sub>IH</sub> (Max)	(Notes 3, 4, 5)	
			240					
	CP, MR D <sub>0</sub> -D <sub>5</sub>	500	μA	-55°C				
		340						
I <sub>EE</sub>	Power Supply Current	-135	-50	mA	-55°C to +125°C	Inputs Open	(Notes 3, 4, 5)	

**Note 3:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals -55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 4:** Screen tested 100% on each device at -55°C, +25°C, and +125°C, Subgroups 1, 2, 3, 7, and 8.

**Note 5:** Sample tested (Method 5005, Table I) on each manufactured lot at -55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

**Note 6:** Guaranteed by applying specified input condition and testing V<sub>OH</sub>/V<sub>OL</sub>.

## AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$

Symbol	Parameter	$T_C = -55^\circ C$		$T_C = +25^\circ C$		$T_C = +125^\circ C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
$f_{max}$	Toggle Frequency	375		375		375		MHz	Figures 2, 3	(Note 10)
$t_{PLH}$	Propagation Delay	0.40	2.40	0.50	2.20	0.50	2.60	ns	Figures 1, 3	(Notes 7, 8, 9)
$t_{PHL}$	$CP_a$ , $CP_b$ to Output									
$t_{PLH}$	Propagation Delay	0.60	2.70	0.70	2.60	0.80	2.90	ns	Figures 1, 4	
$t_{PHL}$	MR to Output									
$t_{TLH}$	Transition Time	0.20	1.60	0.20	1.60	0.20	1.60	ns	Figures 1, 3	(Note 10)
$t_{THL}$	20% to 80%, 80% to 20%									
$t_s$	Setup Time									
	$D_0$ - $D_5$	0.90		0.80		0.90		ns	Figure 5	
	MR (Release Time)	1.60		1.80		2.60			Figure 4	
$t_h$	Hold Time	1.50		1.40		1.60		ns	Figure 5	
	$D_0$ - $D_5$									
$t_{pw}(H)$	Pulse Width HIGH	2.00		2.00		2.00		ns	Figures 3, 4	
	$CP_a$ , $CP_b$ , MR									

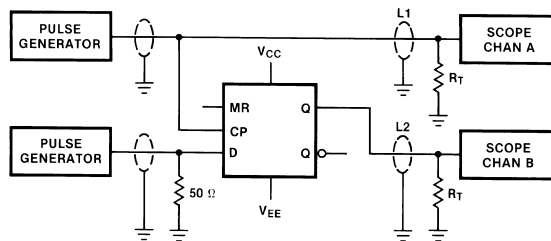
**Note 7:** F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals  $-55^\circ C$ ), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

**Note 8:** Screen tested 100% on each device at  $+25^\circ C$ , Temperature only, Subgroup A9.

**Note 9:** Sample tested (Method 5005, Table I) on each Mfg. lot at  $+25^\circ C$ , Subgroup A9, and at  $+125^\circ C$ , and  $-55^\circ C$  Temperature, Subgroups A10 and A11.

**Note 10:** Not tested at  $+25^\circ C$ ,  $+125^\circ C$  and  $-55^\circ C$  Temperature (design characterization data).

## Test Circuitry



DS100318-5

### Notes:

$V_{CC}$ ,  $V_{CCA} = +2V$ ,  $V_{EE} = -2.5V$

L1 and L2 = equal length  $50\Omega$  impedance lines

$R_T = 50\Omega$  terminator internal to scope

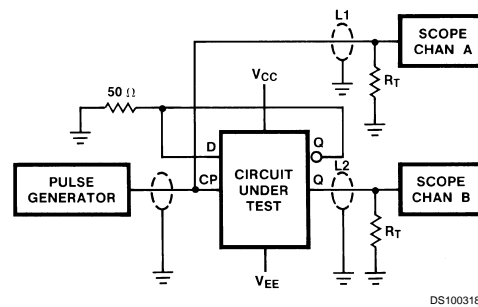
Decoupling  $0.1 \mu F$  from GND to  $V_{CC}$  and  $V_{EE}$

All unused outputs are loaded with  $50\Omega$  to GND

$C_L$  = Fixture and stray capacitance  $\leq 3$  pF

FIGURE 1. AC Test Circuit

## Test Circuitry (Continued)



DS100318-6

### Notes:

$V_{CC}, V_{CCA} = +2V, V_{EE} = -2.5V$

$L1$  and  $L2$  = equal length  $50\Omega$  impedance lines

$R_T = 50\Omega$  terminator internal to scope

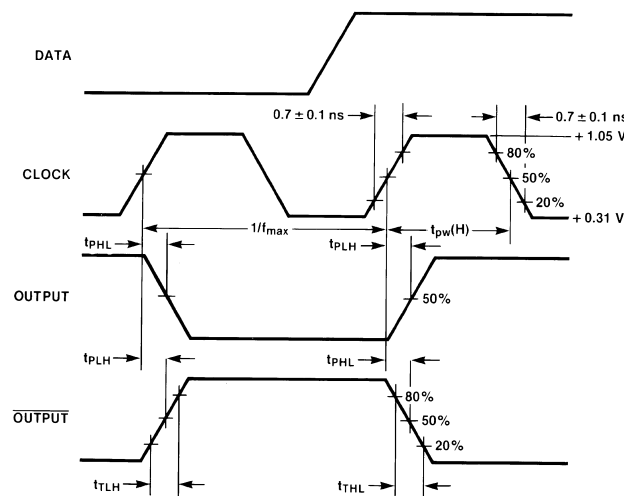
Decoupling  $0.1 \mu F$  from GND to  $V_{CC}$  and  $V_{EE}$

All unused outputs are loaded with  $50\Omega$  to GND

$C_L$  = Jig and stray capacitance  $\leq 3 pF$

FIGURE 2. Toggle Frequency Test Circuit

## Switching Waveforms



DS100318-7

FIGURE 3. Propagation Delay (Clock) and Transition Times

## Switching Waveforms (Continued)

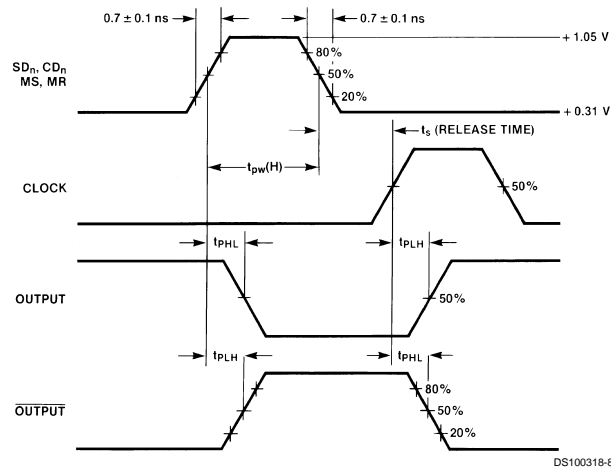
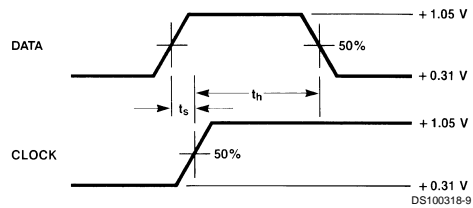


FIGURE 4. Propagation Delay (Reset)

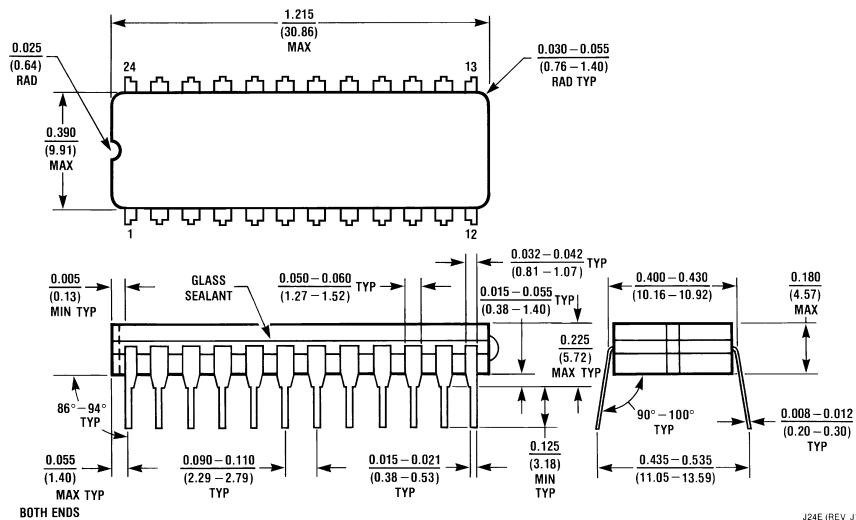


**Notes:**

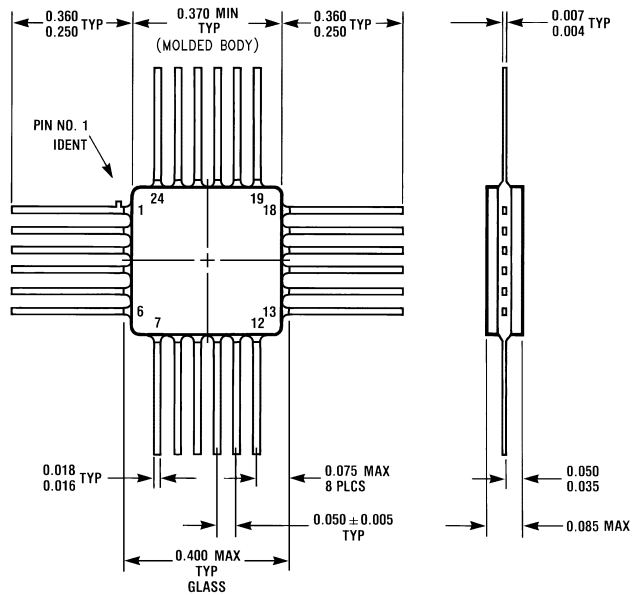
- $t_s$  is the minimum time before the transition of the clock that information must be present at the data input.
- $t_h$  is the minimum time after the transition of the clock that information must remain unchanged at the data input.

FIGURE 5. Setup and Hold Time

**Physical Dimensions** inches (millimeters) unless otherwise noted



**24-Lead Ceramic Dual-In-Line Package (D)**  
NS Package Number J24E



**24-Lead Quad Cerpak (F)**  
NS Package Number W24B

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# 100351 Product Folder

## Low Power Hex D Flip-Flop

<a href="#">General Description</a>	<a href="#">Features</a>	<a href="#">Datasheet</a>	<a href="#">Package &amp; Models</a>	<a href="#">Samples &amp; Pricing</a>
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Title	Size in Kbytes	Date	<a href="#">View Online</a>	<a href="#">Download</a>	<a href="#">Receive via Email</a>
100351 Low Power Hex D Flip-Flop	147 Kbytes	17-Aug-98	<a href="#">View Online</a>	<a href="#">Download</a>	<a href="#">Receive via Email</a>
100351 Mil-Aero Datasheet MN100351-X	106 Kbytes		<a href="#">View Online</a>	<a href="#">Download</a>	<a href="#">Receive via Email</a>

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### Package Availability, Models, Samples & Pricing

Part Number	Package			Status	Models		Samples & Electronic Orders	Budgetary Pricing		Std Pack Size	<a href="#">Package Marking</a>
	Type	Pins	MSL		SPICE	IBIS		Qty	\$US each		
5962-9457901MXA	<a href="#">CERDIP</a>	24	<a href="#">MSL</a>	Full production	N/A	N/A	<a href="#">Buy Now</a>	50+	\$41.6000	rail of 15	[logo]cZcSc4cASE 100351DMQB /Q 5962-9457901MXA
5962-9457901MYA	<a href="#">CERQUAD</a>	24	<a href="#">MSL</a>	Full production	N/A	N/A	<a href="#">Buy Now</a>	50+	\$44.0000	rail of 14	[logo]cZcSc4cA QSE 100351 FMQB 5962 -9457901 MYA
5962-9457901VXA	<a href="#">CERDIP</a>	24	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$265.0000	rail of 15	[logo]cZcSc4cASE 100351J-QMLV 5962-9457901VXA
100351WFQMLV	<a href="#">CERQUAD</a>	24	<a href="#">MSL</a>	Preliminary	N/A	N/A				rail of N/A	[logo]cZcSc4cA 100351WF QMLV 5962 F9457901 VYA SE
RM100351WFQMLV	<a href="#">CERQUAD</a>	24	<a href="#">MSL</a>	Preliminary	N/A	N/A				rail of N/A	[logo]cZcSc4cA RM100351WF QMLV WFR# CR SE

100351W-QMLV	<a href="#">CERQUAD</a>	24	<a href="#">MSL</a>	Full production	N/A	N/A		50+	\$265.0000	rail of 14	[logo]cZcSc4cA 100351W-QMLV 5962-9457901 VYA SE
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