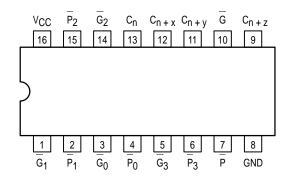


# CARRY LOOKAHEAD GENERATOR

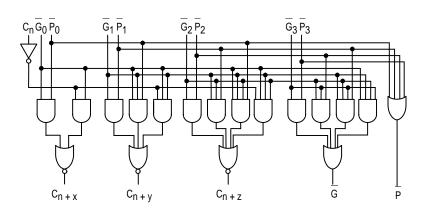
The MC54/74F182 is a high-speed carry lookahead generator. It is generally used with the F181, F381 or 29F01 4-bit arithmetic logic unit to provide high-speed lookahead over word lengths of more than four bits.

- Provides Lookahead Carries Across a Group of Four ALUs
- Multi-level Lookahead High-speed Arithmetic Operation Over Long Word Lengths

#### **CONNECTION DIAGRAM DIP (TOP VIEW)**



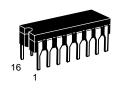
#### **LOGIC DIAGRAM**



# MC54/74F182

# CARRY LOOKAHEAD GENERATOR

**FAST™ SCHOTTKY TTL** 



J SUFFIX CERAMIC CASE 620-09



N SUFFIX PLASTIC CASE 648-08



D SUFFIX SOIC CASE 751B-03

#### ORDERING INFORMATION

MC54FXXXJ Ceramic MC74FXXXN Plastic MC74FXXXD SOIC

#### LOGIC SYMBOL Cn $P_0$ Gn P<sub>1</sub> $C_{n+x}$ 12 -V<sub>CC</sub> = PIN 16 G<sub>1</sub> $c_{n+y}$ GND = PIN 8 - 15 $P_2$ $G_2$ $C_{n+z}$ P<sub>3</sub> $G_3$

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## MC54/74F182

#### **FUNCTION TABLE**

				Inputs					Outputs					
Сn	G <sub>0</sub>	P <sub>0</sub>	G <sub>1</sub>	P <sub>1</sub>	G <sub>2</sub>	P <sub>2</sub>	G <sub>3</sub>	P <sub>3</sub>	C <sub>n+x</sub>	C <sub>n+y</sub>	C <sub>n+z</sub>	G	P	
Х	Н	Н							L					
L	Н	Χ							L					
Х	L	Χ							Н					
Н	Х	L							Н					
Х	Х	Х	Н	Н						L				
Х	Н	Н	Н	X						L				
L	Н	Χ	Н	X						L				
Х	X	Χ	L	X						Н				
Χ	L	Χ	Χ	L						Н				
Н	Χ	L	Χ	L						Н				
Х	Х	Х	Х	Х	Н	Н					L			
Х	X	Χ	Н	Н	Н	X					L			
Χ	Н	Н	Н	X	Н	X					L			
L	Н	Χ	Н	X	Н	X					L			
Х	Х	Χ	Χ	X	L	X					Н			
Х	Х	Χ	L	X	X	L					Н			
Х	L	Χ	Χ	L	X	L					Н			
Н	X	L	X	L	Χ	L					Н			
	Х		Х	Х	Χ	Х	Н	Н				Н		
	Χ		Χ	X	Н	Н	Н	Χ				Н		
	X		Н	Н	Н	X	Н	X				Н		
	Н		Н	X	Н	X	Н	X				Н		
	X		Χ	X	X	X	L	X				L		
	X		Χ	X	L	X	X	L				L		
	X		L	X	X	L	X	L				L		
	L		Х	L	Χ	L	X	L				L		
		Н		Х		Х		Х					Н	
		Χ		Н		Χ		Χ					Н	
		Х		Χ		Н		Χ					Н	
		Χ		X		Χ		Н					Н	
		L		L		L		L					L	

H = HIGH Voltage Level L = LOW Voltage Level X = Don't Care

#### **GUARANTEED OPERATING RANGES**

Symbol	Parameter		Min	Тур	Max	Unit
VCC	Supply Voltage	54,74	4.5	5.0	5.5	V
TA	Operating Ambient Temperature Range	54	<b>-</b> 55	25	125	°C
		74	0	25	70	
loн	Output Current — High	54, 74			-1.0	mA
loL	Output Current — Low	54, 74			20	mA

### MC54/74F182

#### DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

					Limits					0
Symbol	Parameter		Min Typ Max		Unit	Test Conditions				
VIH	Input HIGH Voltage			2.0			V	Guaranteed Input HIGH Voltage		
V <sub>IL</sub>	Input LOW Volta	ige			0.8	V	Guaranteed Input LOW Voltage			
VIK	Input Clamp Dio	de Voltage				-1.2	V	I <sub>IN</sub> = -18 mA	V <sub>CC</sub> = MIN	
Vон	Output HIGH Voltage 54, 74			2.5	3.4		V	I <sub>OH</sub> = -1.0 mA	V <sub>CC</sub> = 4.50 V	
			74	2.7	3.4		V	$I_{OH} = -1.0 \text{ mA}$	V <sub>CC</sub> = 4.75 V	99
VOL	Output LOW Voltage				0.35	0.5	V	I <sub>OL</sub> = 20 mA	V <sub>CC</sub> = MIN	
IH	Input HIGH Curr	ent				20	μΑ	V <sub>IN</sub> = 2.7 V	$V_{CC} = MAX$	Н
						100	μΑ	V <sub>IN</sub> = 7.0 V	VCC = MAX	
		C <sub>n</sub> Input				-1.2				
		P <sub>3</sub> Input				-2.4				U,
I⊫	Input LOW P <sub>2</sub> Input					-3.6	mA	V <sub>IN</sub> = 0.5 V	VCC = MAX	
	Current	urrent G <sub>3</sub> , P <sub>0</sub> , P <sub>1</sub> Inputs				-4.8				
		G <sub>0</sub> , G <sub>2</sub> Inputs				-8.4				U,
		G <sub>1</sub> Input				-9.6	1			
los	Output Short Circuit Current (Note 2)			-60		-150	mA	V <sub>OUT</sub> = 0 V	V <sub>CC</sub> = MAX	
ІССН	Power Supply Current (All Outputs HIGH)				18.4	28	mA	P <sub>3</sub> , G <sub>3</sub> = 4.5 V All Other Inputs = GND	V <sub>CC</sub> = MAX	
ICCL	Power Supply Current (All Outputs LOW)				23.5	36	mA	G <sub>0</sub> , G <sub>1</sub> , G <sub>2</sub> = 4.5 V All Other Inputs = GND	VCC = MAX	6

		54/74F			54	1F	74		
			T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0 V			to +125°C	T <sub>A</sub> = 0°C		
						) V ± 10%	V <sub>CC</sub> = 5.0		
		C <sub>L</sub> = 50 pF			C <sub>L</sub> =	50 pF	C <sub>L</sub> = 9		
Symbol	Parameter	Min	Тур	Max	Min	Max	Min	Max	Unit
<sup>t</sup> PLH	Propagation Delay	3.0	6.6	8.5	3.0	10.5	3.0	9.5	no
<sup>t</sup> PHL	$C_n$ to $C_{n+x}$ , $C_{n+y}$ , $C_{n+z}$	3.0	6.8	9.0	3.0	11	3.0	10	ns
<sup>t</sup> PLH	Propagation Delay	2.5	6.2	8.0	2.5	10.7	2.5	9.0	
<sup>t</sup> PHL	$ \begin{array}{c}  - & - \\  - &$	1.5	3.7	5.0	1.5	6.5	1.5	6.0	ns
<sup>t</sup> PLH	Propagation Delay	2.5	6.5	8.5	2.5	10.5	2.5	9.5	
<sup>t</sup> PHL	$G_0$ , $G_1$ , or $G_2$ to $C_{n+x}$ , $C_{n+y}$ , $C_{n+z}$	1.5	3.9	5.2	1.5	6.5	1.5	6.0	ns

 For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
 No more than one output should be shorted at a time, nor for more than 1 second. **AC CHARACTERISTICS** 

#### **AC CHARACTERISTICS** (Continued)

			54/74F		54	1F	74	ŀF	
			A = +25°(	С	T <sub>A</sub> = -55°C	to +125°C	T <sub>A</sub> = 0°C		
			V <sub>CC</sub> = +5.0 V C <sub>L</sub> = 50 pF			) V ± 10%	V <sub>CC</sub> = 5.0		
						50 pF	C <sub>L</sub> = 50 pF		
Symbol	Parameter	Min	Тур	Max	Min	Max	Min	Max	Unit
tPLH	Propagation Delay	2.0	7.9	10	2.0	12.5	2.0	11	20
<sup>t</sup> PHL	$P_1, P_2, \text{ or } P_3 \text{ to } G$	2.0	6.0	8.0	2.0	9.5	2.0	9.0	ns
<sup>t</sup> PLH	Propagation Delay	2.0	8.3	10.5	2.0	12.5	2.0	11.5	ns
tPHL	G <sub>n</sub> to G	1.5	5.7	7.5	1.5	9.5	1.5	8.5	115
tPLH	Propagation Delay	2.5	5.7	7.5	2.5	11	2.5	8.5	ns
<sup>t</sup> PHL	P <sub>n</sub> to P	2.5	4.1	5.5	2.5	7.5	2.5	6.5	115

#### **FUNCTIONAL DESCRIPTION**

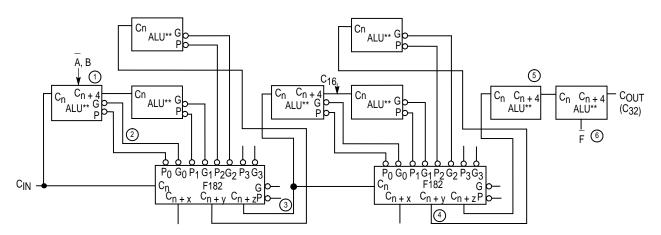
The F182 carry lookahead generator accepts up to four pairs of active-LOW Carry Propagate ( $P_0$ - $P_3$ ) and carry Generate ( $G_0$ - $G_3$ ) signals and an active-HIGH Carry input ( $C_n$ ) and provides anticipated active-HIGH carries ( $C_{n+x}$ ,  $C_{n+y}$ ,  $C_n$ +Z) across four groups of binary adders. The F182 also has active-LOW Carry Propagate (P) and Carry Generate (P) outputs which may be used for further levels of lookahead. The logic equations provided at the output are:

$$C_{n+x} = G_0 + P_0C_n$$
  
 $C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$   
 $C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$ 

$$G = \frac{G_3 + P_3G_2}{P_3P_2P_1P_0} + P_3P_2P_1G_0$$

$$P = P_3P_2P_1P_0$$

Also, the F182 can be used with binary ALUs in an active-LOW or active-HIGH input operand mode. The connections (Figure 1) to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last F181 or F381.



<sup>\*\*</sup> ALUs may be either F181, F381, or 2901A.

Figure 1. 32-Bit ALU with Ripple Carry Between 16-Bit Lookahead ALUs

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