Evaluating the ADGM1001 0 Hz/DC to 34 GHz, SPDT, MEMS Switch

FEATURES

- Single-supply voltage: 3.3 V
- Wide frequency range: DC to 34 GHz
- SMA connectors for RF signals
- Parallel interface and SPI
- On-board CALIBRATION THRU transmission line for analyzer calibration

EVALUATION KIT CONTENTS

EVAL-ADGM1001SDZ evaluation board

ADDITIONAL EQUIPMENT NEEDED

- 3.3 V dc power supply
- Vector network analyzer (VNA)
- EVAL-SDP-CB1Z (SDP-B) controller board
- Analysis | Control | Evaluation (ACE) Software with EVAL-ADGM1001SDZ plug-in

GENERAL DESCRIPTION

This user guide describes the EVAL-ADGM1001SDZ evaluation board for the ADGM1001, a dual-chip, RF switching solution containing a single-pole, two-throw (SPDT), microelectromechanical systems (MEMS) switch, and a control chip copackaged in a compact, 5.00 mm × 4.00 mm × 0.90 mm, LGA package.

The SPDT switch uses Analog Devices, Inc., MEMS switch technology, providing optimum performance in terms of bandwidth, power handling capability, and linearity for RF applications. The control chip generates the high voltage signals needed for the MEMS switch and allows the user to control its operation through a simple and flexible complementary metal-oxide semiconductor (CMOS)-/low voltage transistor-transistor logic (LVTTL)-compliant parallel interface as well as via a serial peripheral interface (SPI). It is possible to daisy-chain multiple ADGM1001 devices together to enable the configuration of multiple devices with a minimal number of digital lines.

For SPI, the EVAL-ADGM1001SDZ connects to the USB port of a PC via the SDP board. The EVAL-SDP-CB1Z board (SDP-B controller board) is available to order at via the Analog Devices website at www.analog.com/SDP-B.

The EVAL-ADGM1001SDZ comes fitted with connectors for RF and control signals as well as links to control the operation of the switch and evaluate its performance.

For full details on the ADGM1001, see the ADGM1001 data sheet, which should be consulted in conjunction with this user guide when using the EVAL-ADGM1001SDZ evaluation board.

EVAL-ADGM1001SDZ EVALUATION BOARD PHOTOGRAPH

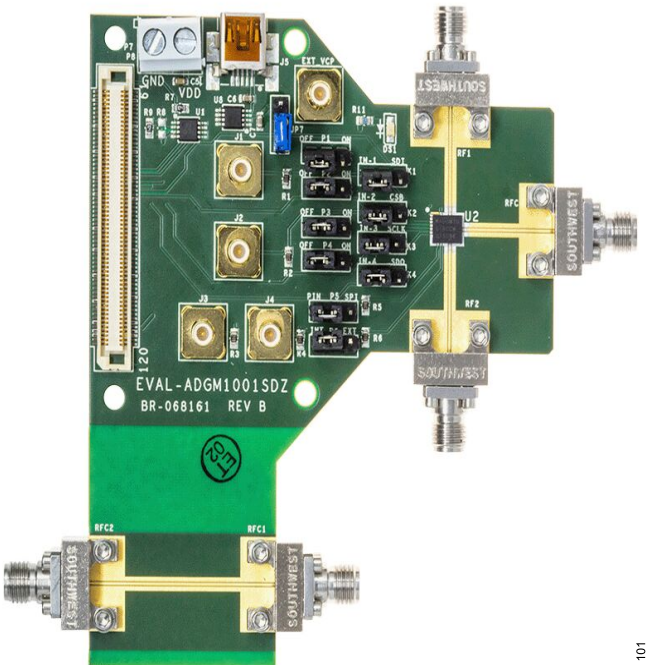

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Figure 1.

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REVISION HISTORY

3/2022—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The EVAL-ADGM1001SDZ evaluation kit contains a fully fitted, printed circuit board (PCB).

The EVAL-ADGM1001SDZ allows the user to connect RF signals to the MEMS switch. The user controls the switch operation using the on-board links or by applying the correct control signals to the appropriate connectors.

The EVAL-ADGM1001SDZ provides an additional transmission line to facilitate the calibration of the network analyzer to minimize the effects of the PCB tracks that connect the RF signals to the MEMS switch. This user guide describes the calibration process in detail (see the Network Analyzer Calibration Procedure section).

POWER SUPPLY

To operate the EVAL-ADGM1001SDZ, the user must provide an external power supply either through a Mini-USB connector (J5) or through the power block (P7). When JP7 is in the A position, the EVAL-ADGM1001SDZ is powered by the Mini-USB connector, and when JP7 is in the B position, the EVAL-ADGM1001SDZ is powered by the external 3.3 V power supply through the power block (see Table 1). The power supply voltage required for the EVAL-ADGM1001SDZ is 3.3 V, and it must be positive with respect to the ground of the EVAL-ADGM1001SDZ. The ground of the EVAL-ADGM1001SDZ is marked with GND on the silkscreen (see Figure 25).

Table 1. JP7 Link Position

Position	Power Supply Selection
A	EVAL-ADGM1001SDZ powered by the Mini-USB
B	EVAL-ADGM1001SDZ powered by the external 3.3 V power supply

RF CONNECTORS

The 2.92 mm end launch connectors on the EVAL-ADGM1001SDZ (RF1, RF2, and RFC) connect to each switch in the ADGM1001 for performance evaluation purposes. The RFC1 and RFC2 connectors connect to a transmission line to estimate the loss associated with the PCB (see the Measuring Switch Performance section).Table 2 describes the RF connectors to the ADGM1001.

Table 2. Connecting the RF Connectors to the ADGM1001

Connector	Description
RF1	Port RF1 of the ADGM1001
RF2	Port RF2 of the ADGM1001
RFC	Common RF port of the ADGM1001
RFC1, RFC2	CALIBRATION THRU transmission lines used for calibration

SWITCH CONTROL CONNECTORS

The ADGM1001 comes with a standard LVTTL parallel interface consisting of two input pins (IN1 and IN2) controlled by the P1 and P2 links. See Table 5 for more details on the logic control when using the parallel interface.

The ADGM1001 also has a SPI that can be controlled by the K1 to K4 links. When P5 link is set to the PIN position, the SPI is enabled. When the P5 link is set to the SPI position, the parallel interface is enabled (see Table 3).

Table 3. P5 Link Position

Position	Reference Clock Setting
SPI (Default)	Parallel interface enabled
PIN	SPI enabled, parallel interface disabled

The control IC packaged with the MEMS switch internally generates the voltage required to drive the switch. The internal control IC contains a reference clock signal at a nominal 10 MHz. In normal operation, set the P6 link to INT, enabling the built-in 10 MHz oscillator to enable the internal driver IC voltage boost circuitry (see Table 4). Set the P6 link to EXT to disable the internal 10 MHz oscillator and drive the V_{CP} pin with 80 V dc from the external voltage supply. The V_{CP} pin is connected to the EXT_VCP SMB connector on the EVAL-ADGM1001SDZ, which can be used for applying 80 V dc to the external voltage supply. Disabling the internal oscillator eliminates the associated 10 MHz noise feedthrough into the switch. With the oscillator disabled, the logic interface pins (P1 to P2) still control the switch.

Table 4. P6 Link Position

Position	Reference Clock Setting
INT (Default)	Built-in 10 MHz oscillator enable
EXT	Disables the internal oscillator

Table 5. Link Settings (Per PCB Label) for Parallel Interface Use (See Figure 7)

P1	P2	P3	P4	K1	K2	K3	K4	RF1 to RFC	RF2 to RFC
OFF	OFF	OFF	OFF	IN-1	IN-2	IN-3	IN-4	OFF	OFF
ON	OFF	OFF	OFF	IN-1	IN-2	IN-3	IN-4	ON	OFF
OFF	ON	OFF	OFF	IN-1	IN-2	IN-3	IN-4	OFF	ON
ON	ON	OFF	OFF	IN-1	IN-2	IN-3	IN-4	ON	ON

EVALUATION BOARD SOFTWARE FOR THE SPI

INSTALLING THE SOFTWARE

The EVAL-ADGM1001SDZ uses the Analog Devices ACE software. ACE is a desktop software application that allows the evaluation and control of multiple evaluation systems.

The ACE software installer installs the necessary SDP drivers and .NET Framework 4 by default. Install the ACE software before connecting the SDP driver. The ACE software and access to full instructions on how to install and use the ACE software can be found on the Analog Devices website at www.analog.com/ace.

After the installation completes, the EVAL-ADGM1001SDZ plugins appear when opening the ACE software.

INITIAL SETUP

To set up the EVAL-ADGM1001SDZ, complete the following steps:

1. Change the position of the K1 through the K4 links to SDI, CSB, SCLK, and SDO, respectively.
2. Change the position of the P1 through the P4 links to the off position.
3. Change the P5 link position from PIN to SPI and keep the P6 link position at INT.
4. Connect the EVAL-ADGM1001SDZ to the SDP board and connect the SDP board to the computer via a USB cable.
5. Power the EVAL-ADGM1001SDZ as described in the Power Supply section.
6. Run the ACE software. The EVAL-ADGM1001SDZ board plugins appear in the attached hardware section of the **Start** tab (see Figure 2).
7. Double-click on the EVAL-ADGM1001SDZ board plug-ins to open the evaluation board view in Figure 3.
8. The chip block diagram can be accessed by double-clicking on the ADGM1001 chip (see Figure 2). This view provides a basic representation of functionality of the board. The main functions are labeled in Figure 4.

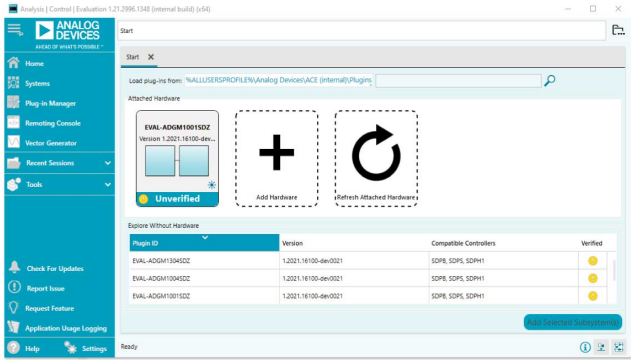

Figure 2. EVAL-ADGM1001SDZ Plugin Start-Up Window

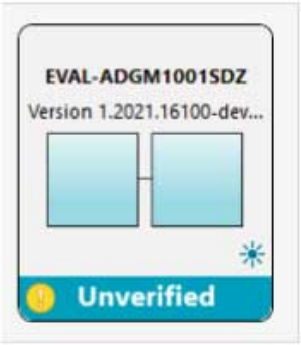

Figure 3. Evaluation Board View of the EVAL-ADGM1001SDZ

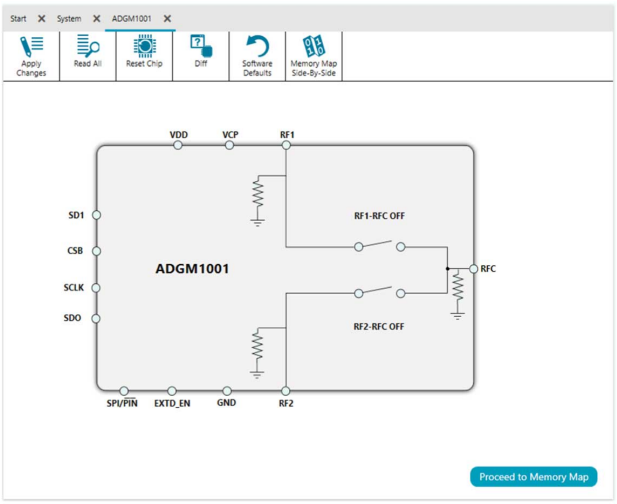

Figure 4. Chip Block Diagram View for the ADGM1001

Table 6. SPI Interface Links Description

Links	Position	Description
K1	SDI	Serial data Input pin
K2	CSB	Chip select pin
K3	SCLK	Clock input pin
K4	SDO	Serial data output pin

EVAL-ADGM1001SDZ BLOCK DIAGRAM AND DESCRIPTIONS

The EVAL-ADGM1001SDZ software is organized so that it appears similar to the functional block diagram shown in the ADGM1001 data sheet. In this way, it is easy to correlate the functions on the EVAL-ADGM1001SDZ with the description in the data sheet. A full description of each block and register, as well as their respective settings, is given in the ADGM1001 data sheet.

Some of the blocks and their functions are described in Table 7 as these blocks pertain to the EVAL-ADGM1001SDZ. The full screen block diagram, shown in Figure 5, describes the functionality of each block.

All changes to the blocks correspond to the block diagram in the software. For example, if the internal register bit is enabled, it displays as enabled on the block diagram. Any bits or registers that are bold are modified values that have not been transferred to the EVAL-ADGM1001SDZ. After clicking **Apply Changes**, the data is transferred to the EVAL-ADGM1001SDZ.

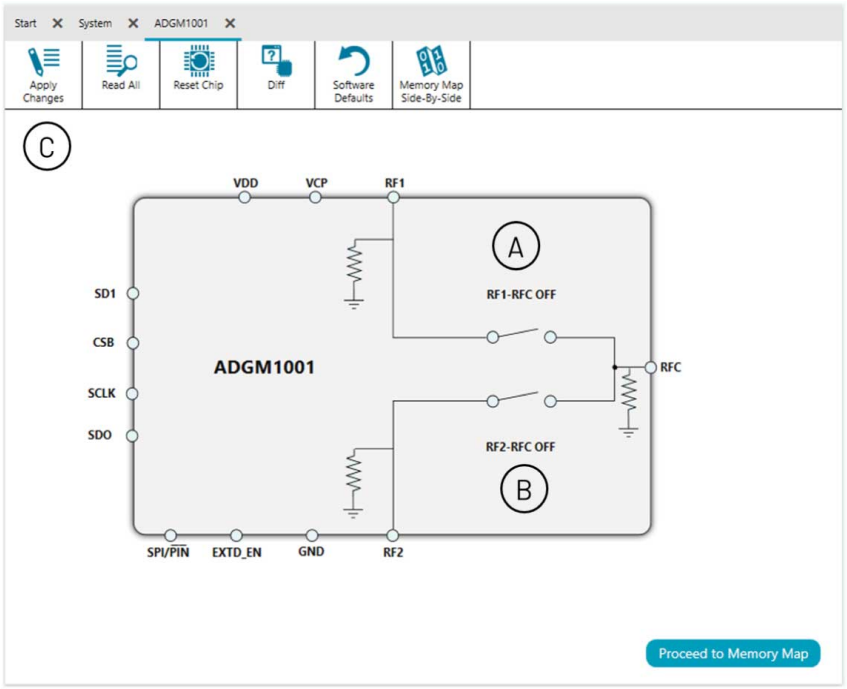

Figure 5. EVAL-ADGM1001SDZ Block Diagram with Labels

Table 7. EVAL-ADGM1001SDZ Block Diagram Function Descriptions (See Figure 5)

Label	Function Description
A	Click the switch symbol to open and close the RF1 to RFC switch
B	Click the switch symbol to open and close the RF2 to RFC switch
C	Click **Apply Changes** to apply all the modified values to the devices

EVAL-ADGM1001SDZ BLOCK DIAGRAM AND DESCRIPTIONS

MEMORY MAP

Click **Proceed to Memory Map** for full accessibility to all of the registers (see Figure 5). This access allows registers to be edited at a bit level (see Figure 6). The bits shaded in dark gray are read only bits and cannot be accessed from ACE, and all other bits are toggled. The **Apply Changes** button transfers data to the ADGM1001.

All changes made in the memory map correspond to the block diagram. For example, if the internal register bit is enabled, the bit displays as enabled in the block diagram. Any bits or registers that are bold are modified values that have not been transferred to the EVAL-ADGM1001SDZ. Click **Apply Changes** to transfer data to the EVAL-ADGM1001SDZ.

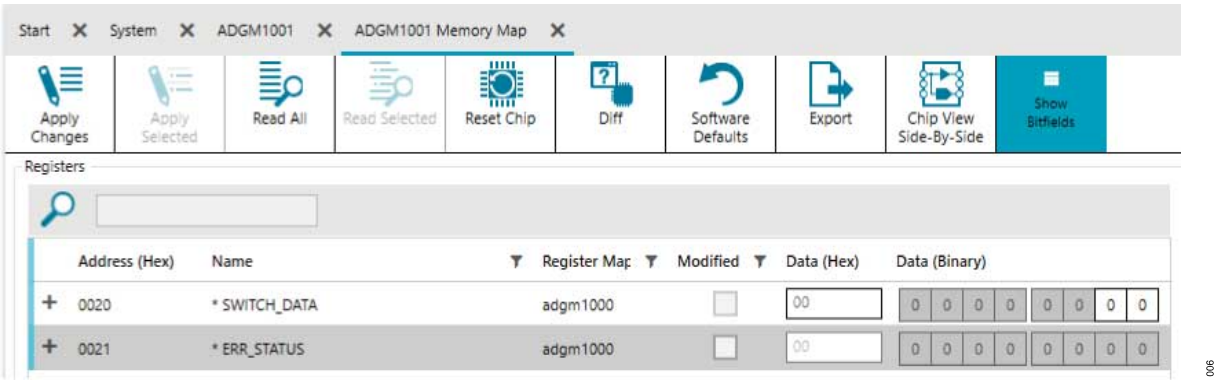

Figure 6. ADGM1001 Memory Map

MEASURING SWITCH PERFORMANCE

Figure 7 shows the EVAL-ADGM1001SDZ of the ADGM1001. Apply a V_{DD} supply to the EVAL-ADGM1001SDZ to measure the performance of the switch. The links are set according to the switch under test (see Table 6). After selecting the desired channel and its state, the switch performance data can be collected using a network analyzer. Terminate the RFx edge connectors of the unused switch channels into 50 Ω loads to achieve the full performance of the channel under test.

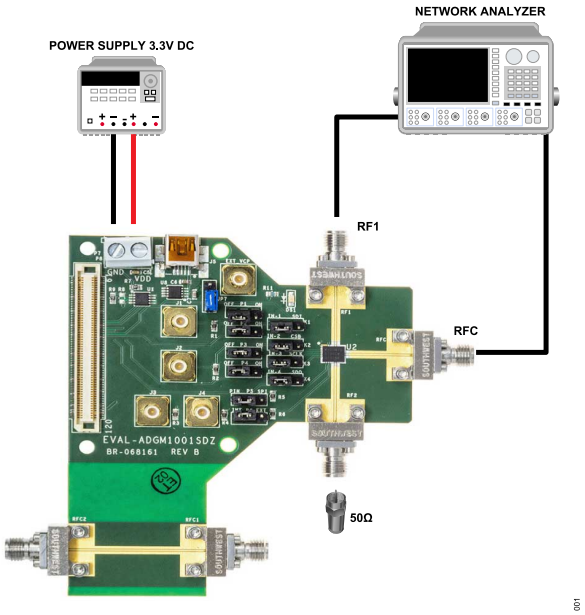

Figure 7. EVAL-ADGM1001SDZ Connection Diagram for Parallel Interface

The EVAL-ADGM1001SDZ, shown in Figure 7, comes with a calibration transmission line, CALIBRATION THRU, on the PCB. This calibration line removes the insertion loss and phase offset of the PCB transmission lines connecting to the switch from the measurement. Figure 8 shows the calibration transmission line and Figure 9 shows its insertion loss and return loss up to 35 GHz. The calibration line is exactly the same length as the distance from any one RFx connector to the RFx pin of the ADGM1001, plus the distance from the RFC connector to the RFC pin of the ADGM1001.

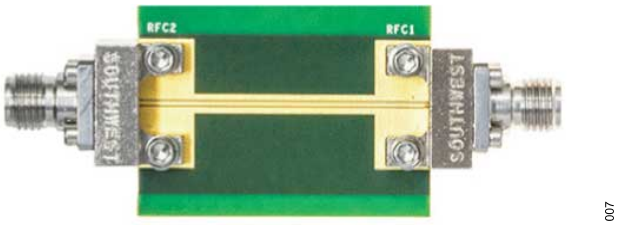

Figure 8. EVAL-ADGM1001SDZ Calibration Transmission Line Used for PCB Insertion Loss and Phase Offset Correction

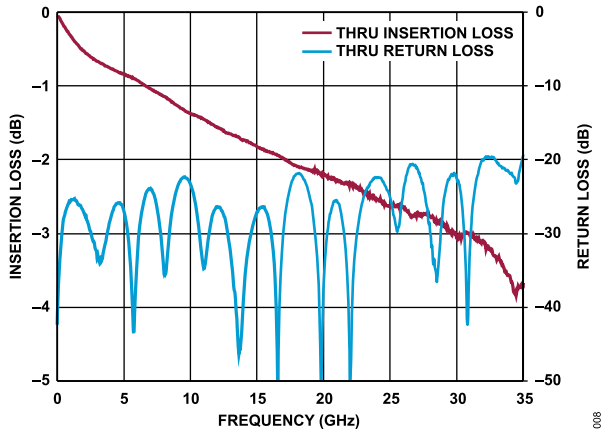

Figure 9. Calibration Transmission Line Insertion Loss and Return Loss

Figure 10 illustrates the calibration line length. All RF traces connecting to the ADGM1001 are of equal length.

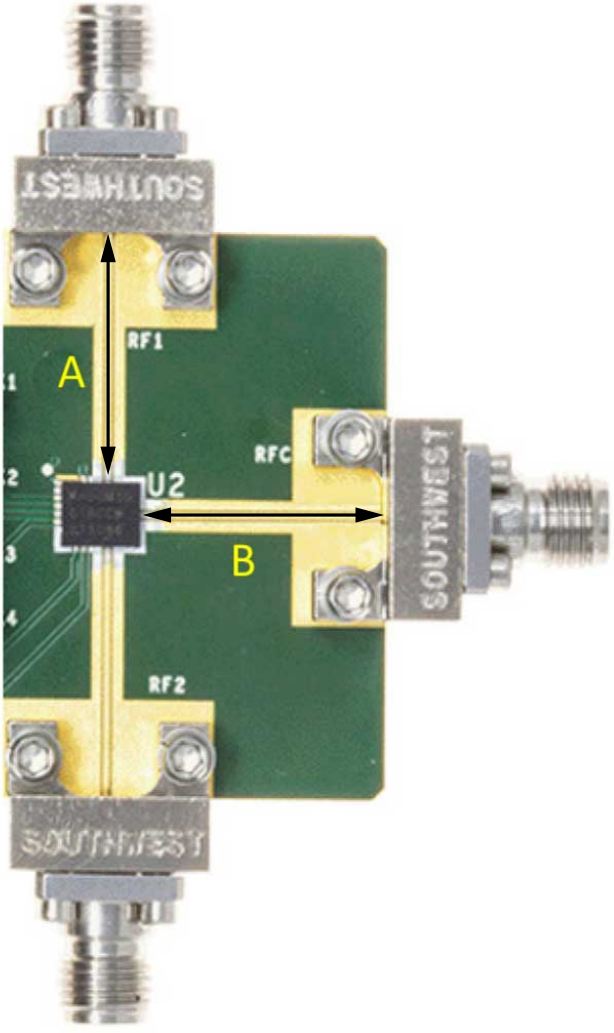

Figure 10. Calibration Transmission Line Length Equal to the A + B Length

MEASURING SWITCH PERFORMANCE

To de-embed the PCB transmission line insertion loss from the entire switch insertion loss board measurement (the RF1 to RFC path), divide the S(2,1) insertion loss of the measured data by the |S(2,1)| of the CALIBRATION THRU line. Perform this de-embedding by using the network analyzer at the time of the measurement or after the measurement using individual measurement data files. Refer to the Network Analyzer Calibration Procedure section for more information.

Use the network analyzer port extension function to de-embed any phase offset introduced by the PCB transmission lines. The port extension method uses time delay offset values to correct for phase. Enter the time delays into the port extension menu on the network analyzer corresponding to any phase offset introduced from an RF edge connector to the switch pin. Figure 10 shows an example of these phase offsets on a typical switch measurement, labeled as A and B. Both A and B are identical in length and can be calculated by measuring the time delay of the calibration line and dividing it by two.

Figure 11 shows the ADGM1001 switch insertion loss measurement results that are de-embedded with respect to the PCB transmission line losses. The red trace shows the return loss of RF1 to RFC switch channel, and the blue trace shows the insertion loss of RF1 to RFC switch channel.

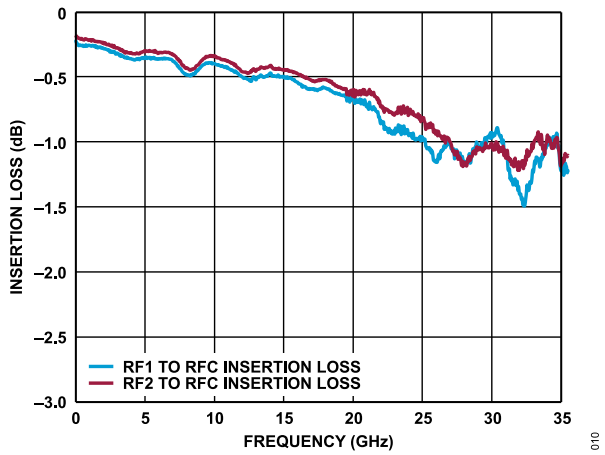

Figure 11. PCB De-Embedded ADGM1001 Insertion Loss Performance

Figure 12 shows the ADGM1001 switch return loss performance measurement results for two channels. The red trace is the RF1 to RFC switch channel, and the blue trace is the RF2 to RFC switch channel.

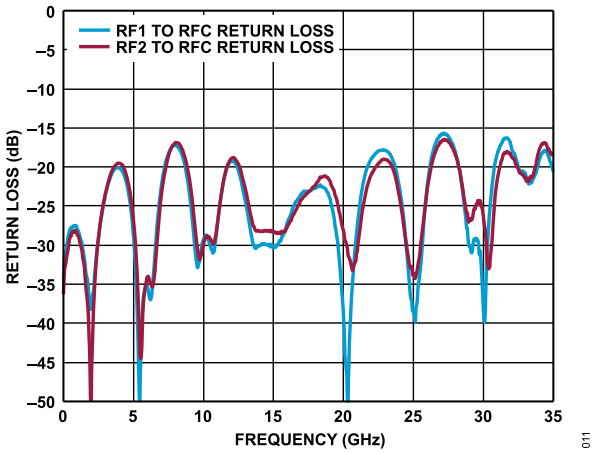

Figure 12. ADGM1001 Return Loss Performance

Figure 13 shows the ADGM1001 switch off isolation performance measurement results for two channels. The red trace is the RF1 to RFC switch channel, and the blue trace is the RF2 to RFC switch channel.

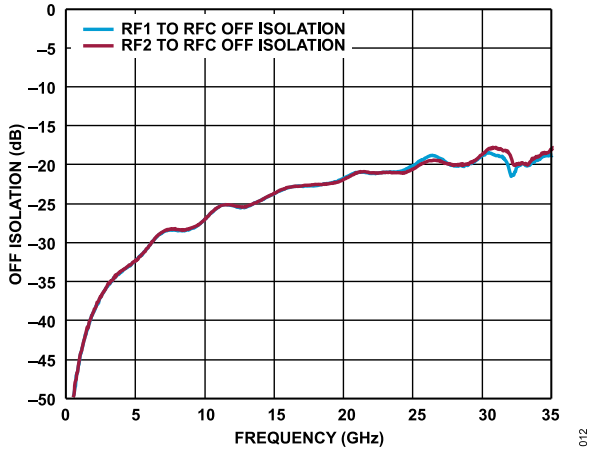

Figure 13. ADGM1001 Off Isolation Performance

NETWORK ANALYZER CALIBRATION PROCEDURE

Use the following procedure in conjunction with the EVAL-ADGM1001SDZ for two-port measurements, assuming the user has a set of manual calibration standards or an electric calibration type unit to perform a short load open through (SLOT) calibration of the network analyzer. The maximum value for the network analyzer frequency sweep for the EVAL-ADGM1001SDZ PCB can be up to 40 GHz.

1. Perform a full, two-port standard SLOT calibration of the network analyzer.
2. Connect the CALIBRATION THRU calibration line (Connector RFC1 and Connector RFC2) to the analyzer and measure its insertion loss, S(2,1).
3. Save the measured data to the network analyzer memory for later use.
4. Configure the EVAL-ADGM1001SDZ links and power up the EVAL-ADGM1001SDZ with a 3.3 V dc power supply.
5. Connect the network analyzer to the desired MEMS switch RF connectors and apply the external control signals, if needed.
6. Measure the complete insertion loss of the EVAL-ADGM1001SDZ. Include the insertion loss of the MEMS switch and test fixture (PCB transmission lines and RF connectors).
7. De-embed the PCB losses from the complete evaluation board measurement using the data saved at Step 3 and the measured data at Step 6. Because the extraction method is dependent on the network analyzer, consult the network analyzer user manual before performing the extraction. Typically, the divide function divides the complete S(2,1) insertion loss measurement data by the CALIBRATION THRU line S(2,1) insertion loss data stored in memory.
8. Use the network analyzer port extension function to de-embed the phase offset introduced by the PCB transmission lines. The port extension method uses time delay offset values to correct for phase. Enter the time delay values into the port extension menu on the network analyzer for each RF edged connector to switch the pin path equal to the electrical length of the calibration line divided by two.

HANDLING GUIDELINES

Adhere to the following handling guidelines for the EVAL-ADGM1001SDZ:

- Always treat the ADGM1001 as a static sensitive device and observe normal handling precautions, including working only on static dissipative surfaces, wearing wrist straps, or other electrostatic discharge (ESD) control devices.
- Take care when connecting signals. Hold the EVAL-ADGM1001SDZ from the edges to avoid any damage to the device under test (DUT).
- Avoid connecting live signal sources. Ensure that outputs are switched off (preferably grounded) before connecting to the DUT. In addition, ensure all instrumentation shares a common chassis ground.
- Avoid running measurement instruments (for example, digital multimeters (DMMs) in autorange modes). Some instruments can generate large transient compliance voltages when switching ranges.
- Use the highest practical range (that is, lowest resolution) setting for resistance measurements to minimize compliance voltages.

LAYOUT RECOMMENDATIONS

The EVAL-ADGM1001SDZ is a 4-layer board. EVAL-ADGM1001SDZ uses 8 mil Roger RO4003C dielectric. The outer copper layers have 2.2 mil finish thickness with electroless nickel immersion gold (ENIG) finish. The RF transmission lines were designed using a coplanar waveguide (CPWG) model with a width of 14 mil and ground spacing of 7 mil to have a characteristic impedance of 50 Ω (see Figure 14 and Figure 15). It is recommended to use plenty of vias under the ADGM1001 and along the RF traces to provide good grounding and to avoid any resonance at high frequencies (see Figure 16). Impedance matching is performed when transitioning from the ADGM1001 to the RF trace on the PCB to avoid any mismatch. Impedance matching details are detailed in Figure 16. To achieve optimum RF performance, south west end launch connectors (1092-04A-12) are used.

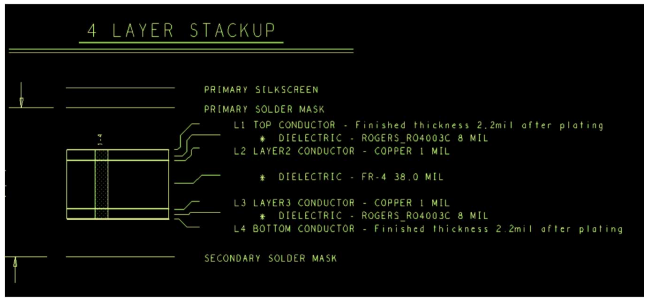

Figure 14. EVAL-ADGM1001SDZ Board Stackup

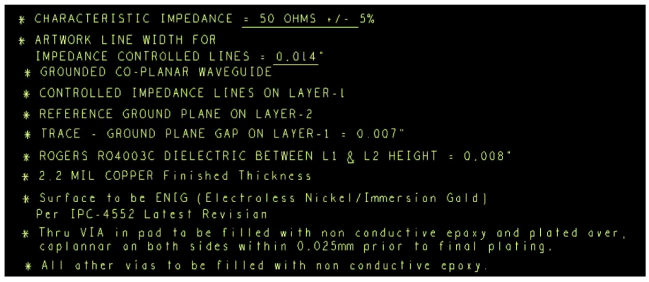

Figure 15. EVAL-ADGM1001SDZ Additional Board Manufacturing Information

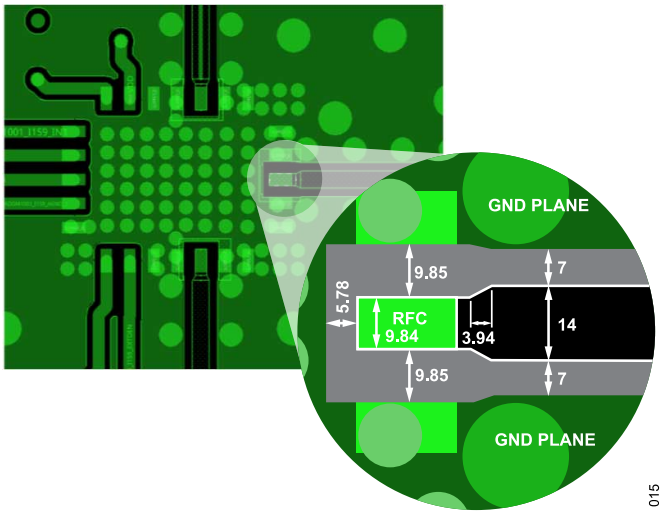

Figure 16. Layout Recommendation in Mils (1 mil = 0.001 inches)

SOLDERING RECOMMENDATIONS

To avoid solder voids under the ADGM1001, it is recommended to use a 0.0767 mm (3 mil) thick solder stencil with nano coating. The aperture size for the solder stencil must be 1:1, and divide the paste mask with multiple pads as shown in Figure 17. Poor soldering may impact the RF performance of the ADGM1001.

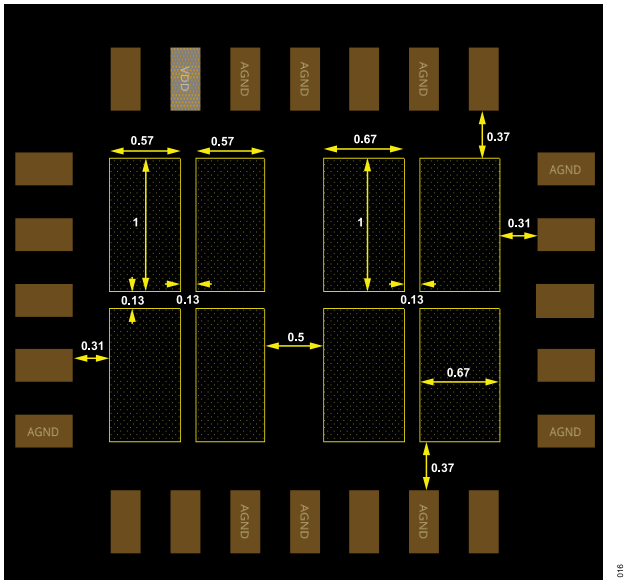

Figure 17. Solder Stencil Recommendations in Millimeters

EVALUATION BOARD SCHEMATICS AND ARTWORK

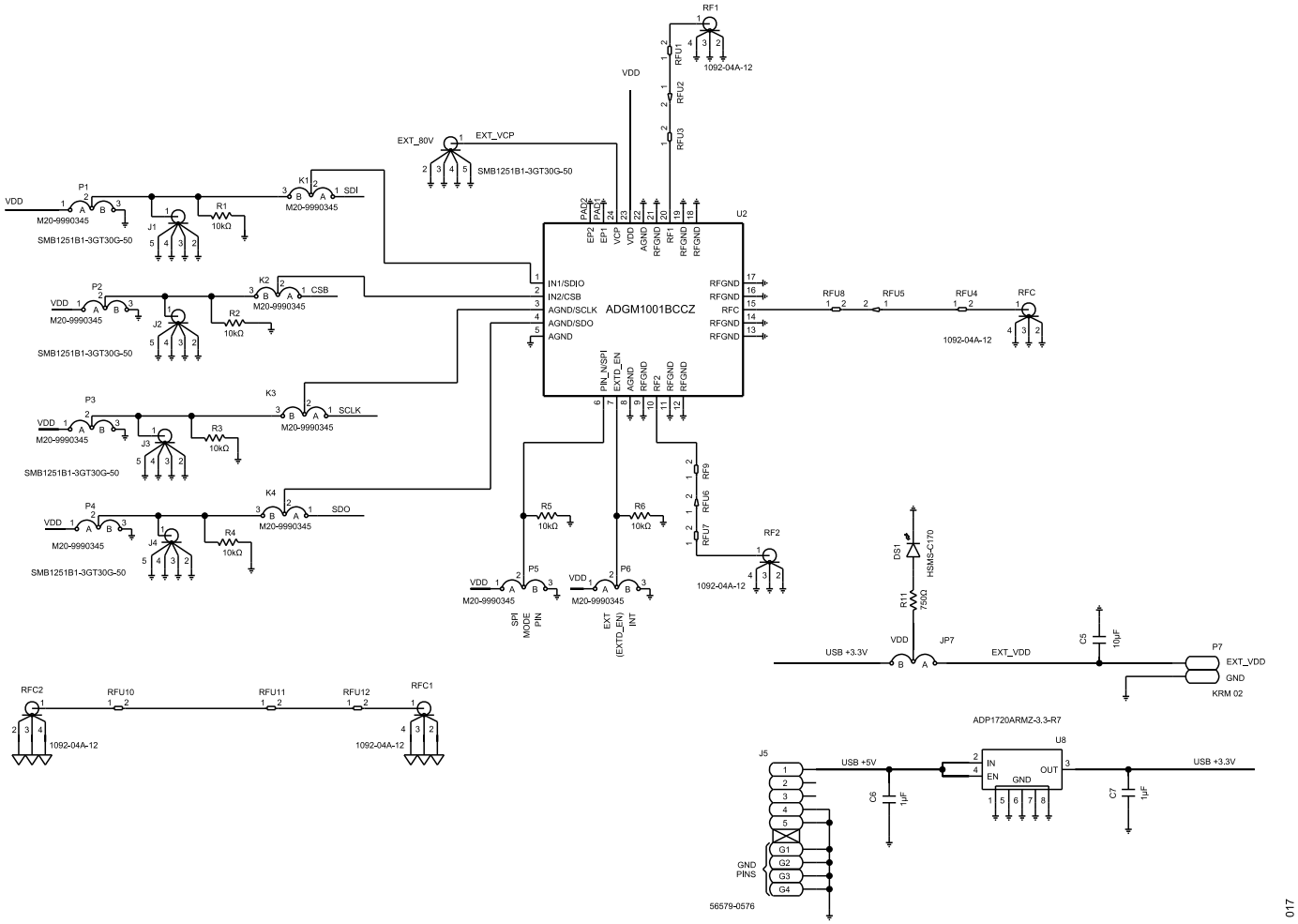

Figure 18. Schematic of the EVAL-ADGM1001SDZ

EVALUATION BOARD SCHEMATICS AND ARTWORK

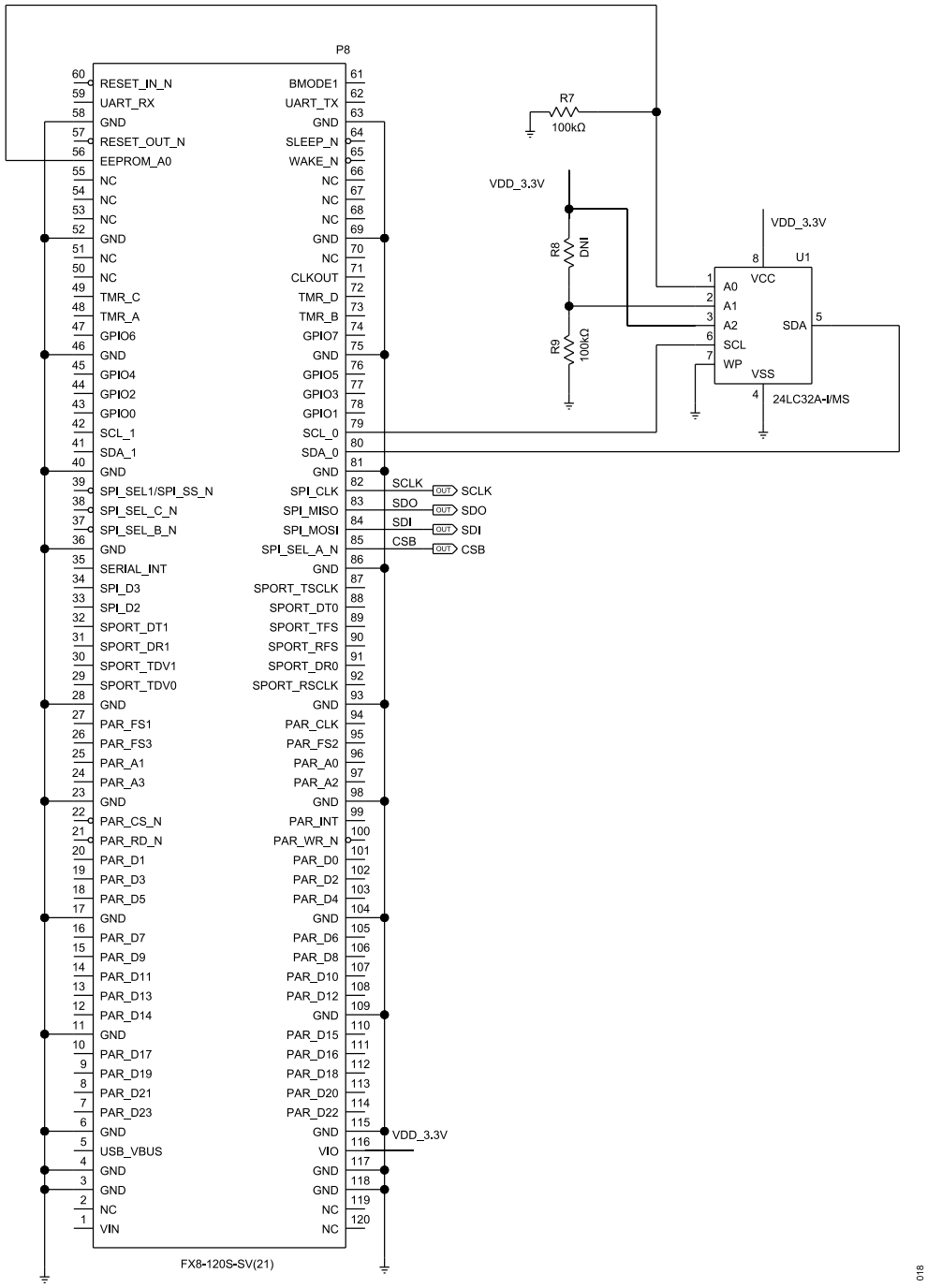

Figure 19. Schematic of the EVAL-ADGM1001SDZ with an SDP Connector

EVALUATION BOARD SCHEMATICS AND ARTWORK

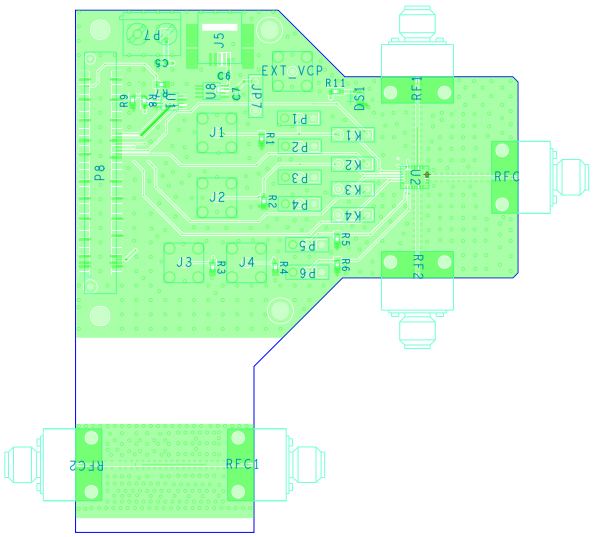

Figure 20. EVAL-ADGM1001SDZ Component Side PCB Drawing (Layer 1)

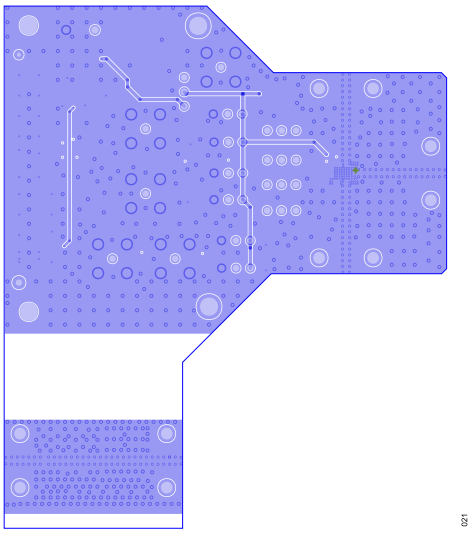

Figure 22. EVAL- ADGM1001SDZ Component Side Ground Plane PCB Drawing (Layer 3)

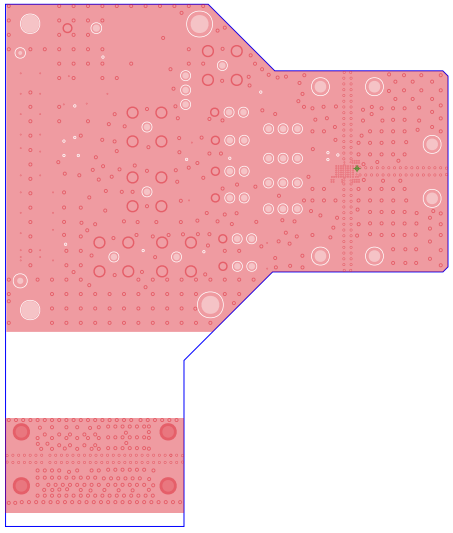

Figure 21. EVAL- ADGM1001SDZ Component Side Ground Plane PCB Drawing (Layer 2)

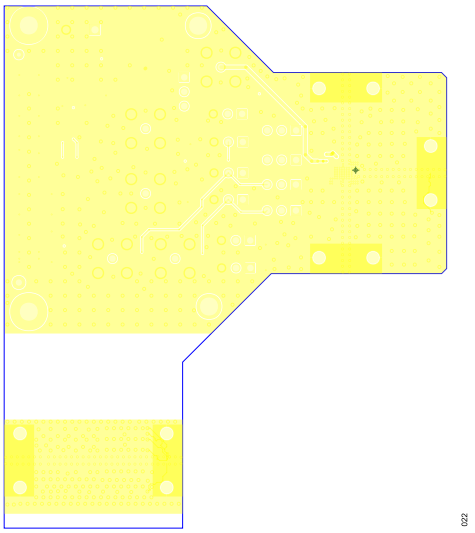

Figure 23. EVAL- ADGM1001SDZ Component Side, Bottom Side PCB Drawing (Layer 4)

EVALUATION BOARD SCHEMATICS AND ARTWORK

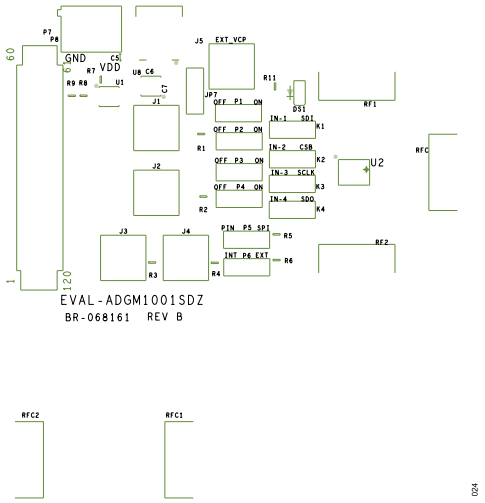

Figure 24. EVAL-ADGM1001SDZ Component Side Silkscreen PCB Drawing (Top)

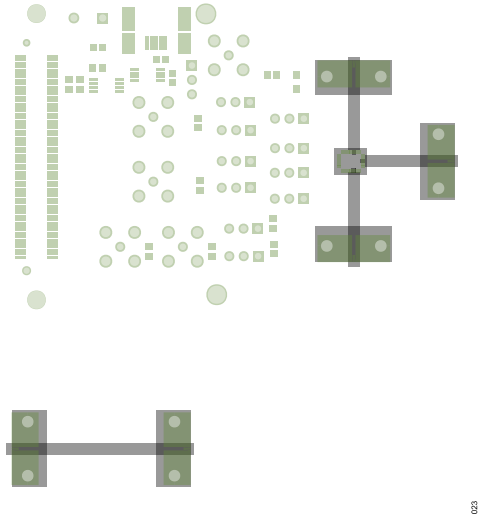

Figure 25. EVAL-ADGM1001SDZ Solder Mask Top

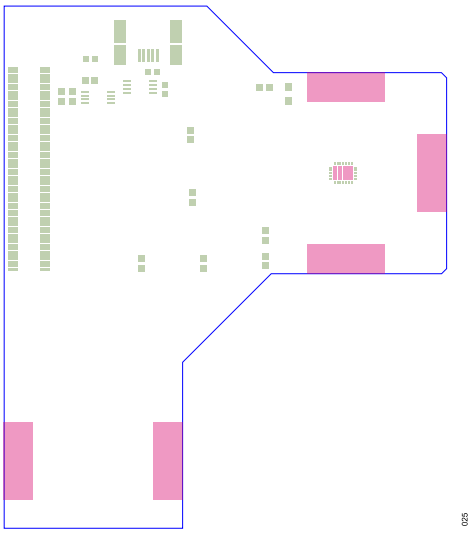

Figure 26. EVAL-ADGM1001SDZ Paste Top

ORDERING INFORMATION

BILL OF MATERIALS

Table 8.

Reference Designator	Description	Manufacturer	Manufacturer Number
C5	10 µF ceramic capacitor, 10 V, 20%, X5R, 0603, low effective series resistance (ESR)	TDK	C1608X5R1A106M080AC
C6, C7	1 µF ceramic capacitors, 16 V, 10%, X7R, 0603	AVX	0603YC105KAT2A
DS1	630 nm light emitting diode (LED), surface-mount device (SMD), red	Broadcom Limited	HSMS-C170
EXT_VCP, J1 to J4	PCB connectors, Subminiature Version B (SMB), coaxial straight jack	Amphenol	SMB1251B1-3GT30G-50
J5	PCB connector, USB MINI-AB series	Molex	56579-0576
JP7, K1 to K4, P1 to P6	PCB connectors, 3 position, male header, unshrouded single row, 2.54 mm pitch, 3 mm solder tail	Harwin	M20-9990345
P7	2-pin terminal block (5 mm pitch)	Lumberg	KRM 02
P8	120-way, 0.6 mm pitch, 2 row straight PCB connector	HRS	FX8-120S-SV(21)
R1 to R6	10 kΩ resistors, SMD, 0.01%, 1/16 W, 0603	Multicomp (SPC)	MCTF0603TTX1002
R11	750 Ω resistors, SMD, 1%, 1/10 W, 0603, AEC-Q200	Vishay	CRCW0603750RFKEA
R7, R9	100 kΩ resistors, 1%, 1/10 W, 0603	Yageo	RC0603JR-07100KL
RF1, RF2, RFC, RFC1, RFC2	PCB connectors, jack female end, launch edge mount, low profile, 2.92 mm, 40 GHz	Southwest Microwave	1092-04A-12
U1	IC, 32 KBIT serial EEPROM	Microchip Technology	24LC32A-I/MS
U2	0 Hz to 34 GHz, SPDT MEMS switch	Analog Devices	ADGM1001BCCZ
Not applicable[1]	Wideband 50 Ω termination SMA loads	Pasternack	PE6081

[1] Screwed on at measurement time (see Figure 7).

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.