HARRIS SEMICONDUCTOR

HSP50214A

February 1998

Programmable Downconverter

Features

- Up to 65 MSPS Front-End Processing Rates (CLKIN) and 55 MSPS (41 MSPS Using the Discriminator) Back-End Processing Rates (PROCCLK) Clocks May Be Asynchronous
- Processing Capable of >100dB SFDR
- Up to 255-Tap Programmable FIR
- Overall Decimation Factor Ranging from 4 to 16384
- Output Samples Rates to ≅12.94 MSPS with Output Bandwidths to ≅ 982kHz Lowpass
- 32-Bit Programmable NCO for Channel Selection and Carrier Tracking
- Digital Resampling Filter for Symbol Tracking Loops and Incommensurate Sample-to-Output Clock Ratios
- Digital AGC with Programmable Limits and Slew Rate to Optimize Output Signal Resolution; Fixed or Auto Gain Adjust
- Serial, Parallel, and FIFO 16-Bit Output Modes
- Cartesian to Polar Converter and Frequency Discriminator for AFC Loops and Demodulation of AM, FM, FSK, and DPSK
- Input Level Detector for External I.F. AGC Support

Applications

- Single Channel Digital Software Radio Receivers
- Base Station Rx's: AMPS, NA TDMA, GSM, and CDMA
- Compatible with HSP50210 Digital Costas Loop for PSK Reception
- Evaluation Platform Available

Description

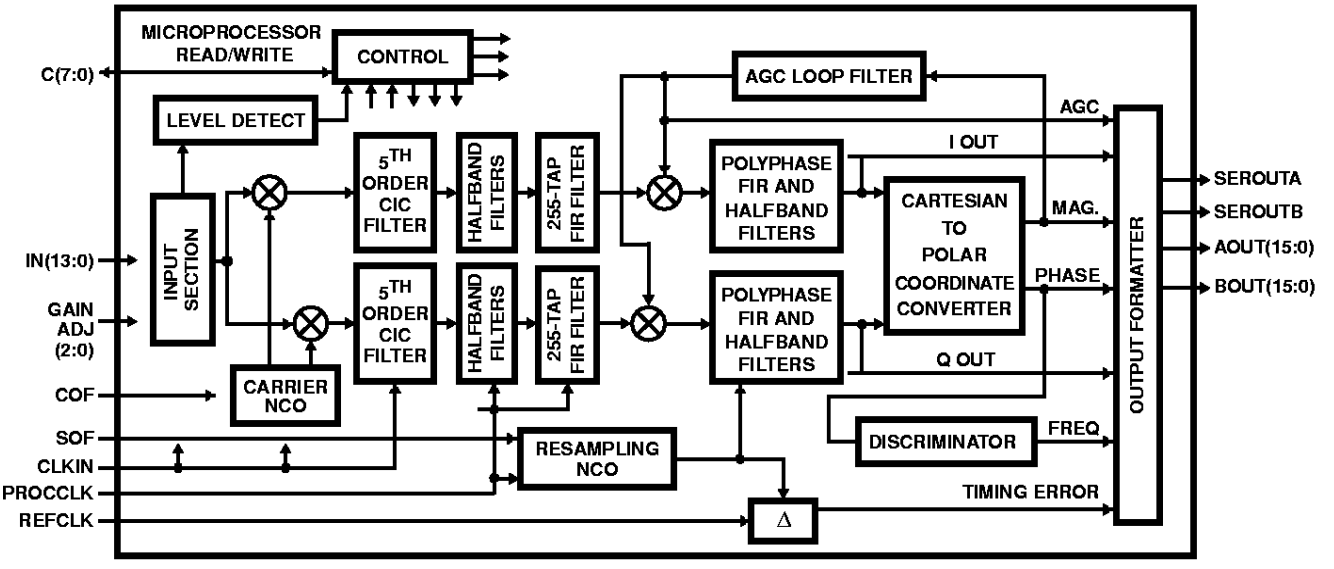
The HSP50214A Programmable Downconverter converts digitized IF data into filtered baseband data which can be processed by a standard DSP microprocessor. The Programmable Downconverter (PDC) performs down conversion, decimation, narrowband low pass filtering, gain scaling, resampling, and Cartesian to Polar coordinate conversion.

The 14-bit sampled IF input is down converted to baseband by digital mixers and a quadrature NCO, as shown in the Block Diagram. A decimating (4 to 32) fifth order Cascaded Integrator-Comb (CIC) filter can be applied to the data before it is processed by up to 5 decimate-by-2 halfband filters. The halfband filters are followed by a 255-tap programmable FIR filter. The output data from the programmable FIR filter is scaled by a digital AGC before being re-sampled in a polyphase FIR filter. The output section can provide seven types of data: Cartesian (I, Q), polar (R, θ), filtered frequency ($d\theta/dt$), Timing Error (TE), and AGC level in either parallel or serial format.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HSP50214AVC	0 to 70	120 Ld MQFP	Q120.28x28
HSP50214AVI	-40 to 85	120 Ld MQFP	Q120.28x28

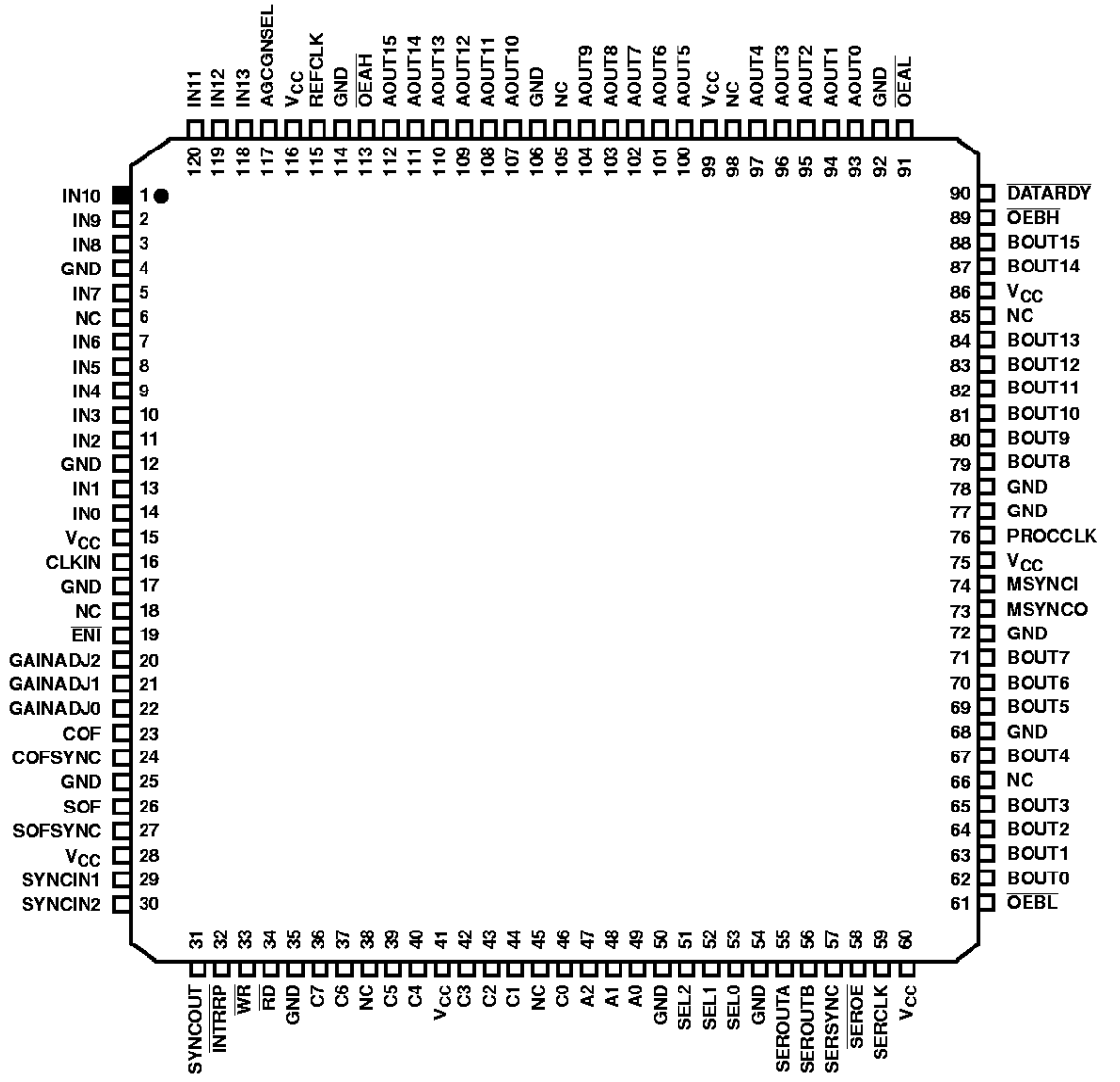
Block Diagram



File Number **4449**

Pinout

120 LEAD MQFP
TOP VIEW



Pin Descriptions

NAME	TYPE	DESCRIPTION
V_{CC}	-	Positive Power Supply Voltage.
GND	-	Ground.
CLKIN	I	Input Clock. This clock should be a multiple of the input sample rate. All input section processing occurs on the rising edge of CLKIN. The frequency of CLKIN is designated f_{CLKIN}.
IN(13:0)	I	Input Data. The format of the input data may be set to offset binary or 2's complement. IN13 is the MSB (see Control Word 0).
$\overline{ENI}$	I	Input Enable. Active Low. This pin enables the input to the part in one of two modes, gated or interpolated (see Control Word 0). In gated mode, one sample is taken per CLKIN when $\overline{ENI}$ is asserted. The input sample rate is designated f_S, which can be different from f_{CLKIN} When $\overline{ENI}$ is used.
GAINADJ(2:0)	I	GAINADJ Input. Adds an offset to the gain via the shifter following the mixer. GAINADJ value is added to the shift code from the microprocessor (µP) interface. The shift code is saturated to a maximum code of F. The gain is offset by (6dB)(GAINADJ); (000 = 0dB gain adjust; 111 = 42dB gain adjust) GAINADJ2 is the MSB. See "Using the Input Gain Adjust Control Signals" Section.
PROCCLK	I	Processing Clock. PROCCLK is the clock for all processing functions following the CIC Section. Processing is performed on PROCCLK's rising edge. All output timing is derived from this clock. ***NOTE: This clock may be asynchronous to CLKIN.***
AGCGNSEL	I	AGC Gain Select. This pin selects between two AGC loop gains. This input is setup and held relative to PROCCLK. Gain setting 1 is selected when AGCGNSEL = 1.
COF	I	Carrier Offset Frequency Input. This serial input pin is used to load the carrier offset frequency into the Carrier NCO (see Serial Interface Section). The offset may be 8, 16, 24, or 32 bits. The setup and hold times are relative to CLKIN. This input is compatible with the output of the HSP50210 Costas loop [1].
COFSYNC	I	Carrier Offset Frequency Sync. This signal is asserted one CLK before the most significant bit (MSB) of the offset frequency word (see Serial Interface Section). The setup and hold times are relative to CLKIN. This input is compatible with the output of the HSP50210 Costas loop [1].
SOF	I	Re-Sampler Offset Frequency Input. This serial input pin is used to load the offset frequency into the Re-Sampler NCO (see Serial Interface Section). The offset may be 8, 16, 24, or 32 bits. The setup and hold times are relative to PROCCLK. This input is compatible with the output of the HSP50210 Costas loop [1].
SOFSYNC	I	Re-Sampler Offset Frequency Sync. This signal is asserted one CLK before the MSB of the offset frequency word (see Serial Interface Section). The setup and hold times are relative to PROCCLK. This input is compatible with the output of the HSP50210 Costas loop [1].
AOUT(15:0)	O	Parallel Output Bus A. Two parallel output modes are available on the HSP50214A. The first is called the Direct Output Port, where the source is selected through Control Word 20 (see the Microprocessor Write Section) and comes directly from the Output MUX Section (see Output Control Section). The most significant byte of AOUT always outputs the most significant byte of the Parallel Direct Output Port whose data type is selected via µP interface. AOUT15 is the MSB. In this mode, the AOUT(15:0) bus is updated as soon as data is available. $\overline{DATARDY}$ is asserted to indicate new data. The second mode for parallel data is called the Buffer RAM Output Port. The Buffer RAM Output Port acts like a FIFO for blocks of information called data sets. Within a data set is I, Q, magnitude, phase, and frequency information; a data type is selected using SEL(2:0). Up to 7 data sets are stored in the Buffer RAM Output Port. The LSBytes of the AOUT and BOUT busses form the 16 bits for the buffered output mode and can be used for buffered mode while the MSBytes are outputting data in the direct output mode.
BOUT(15:0)	O	Parallel Output Bus B. Two parallel output modes are available on the HSP50214A. The first is called the Direct Output Port, where the source is selected through Control Word 20 (see the Microprocessor Write Section) and comes directly from the Output MUX Section (see Output Control Section). The most significant byte of BOUT always outputs the most significant byte of the Parallel Direct Output Port whose data type is selected via µP interface. BOUT15 is the MSB. In this mode, the BOUT(15:0) bus is updated as soon as data is available. $\overline{DATARDY}$ is asserted to indicate new data. The second mode for parallel data is called the Buffer RAM Output Port. The Buffer RAM Output Port acts like a FIFO for blocks of information called data sets. Within a data set is I, Q, magnitude, phase, and frequency information; a particular information is selected using SEL(2:0). Up to 7 data sets is stored in the Buffer RAM Output Port. The least significant byte of BOUT can be used to either output the least significant byte of the B Parallel Direct Output Port or the least significant byte of the Buffer RAM Output Port. See Output Section.

Pin Descriptions (Continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{DATARDY}}$	O	Output Strobe Signal. Active Low. Indicates when new data from the Direct Output Port Section is available. DATARDY is asserted for one PROCCLK cycle during the first clock cycle that data is available on the parallel out busses. See Output Section.
$\overline{\text{OEAH}}$	I	Output enable for the MSByte of the AOUT bus. Active Low.
$\overline{\text{OEAL}}$	I	Output enable for the LSByte of the AOUT bus. Active Low.
$\overline{\text{OEBH}}$	I	Output enable for the MSByte of the BOUT bus. Active Low.
$\overline{\text{OEBL}}$	I	Output enable for the LSByte of the BOUT bus. Active Low.
SEL(2:0)	I	Select Address is used to choose which information in a data set from the Buffer RAM Output Port is sent to the least significant bytes of AOUT and BOUT. SEL2 is the MSB.
$\overline{\text{INTRRP}}$	O	Interrupt Output. Active Low. This output is asserted for 8 PROCCLK cycles when the Buffer RAM Output Port is ready for reading.
SEROUTA	O	Serial Output Bus A Data. I, Q, magnitude, phase, frequency, timing error and AGC information can be sequenced in programmable order. See Output Section and Microprocessor Write Section.
SEROUTB	O	Serial Output Bus B Data. Contents may be related to SEROUTA. I, Q, magnitude, phase, frequency, timing error and AGC information can be sequenced in programmable order. See Output Section and Microprocessor Write Section.
SERCLK	O	Output Clock for Serial Data Out. Derived from PROCCLK as given by Control Word 20 in the Microprocessor Write Section.
SERSYNC	O	Serial Output Sync Signal. Serves as serial data strobes. See Output Section and Microprocessor Write Section.
$\overline{\text{SEROE}}$	I	Serial Output Enable. When high, the SEROUTA, SEROUTB, SERCLK, and SERSYNC signals are set to a high impedance.
C(7:0)	I/O	Processor Interface Data Bus. See Microprocessor Write Section. C7 is the MSB.
A(2:0)	I	Processor Interface Address Bus. See Microprocessor Write Section. A2 is the MSB.
$\overline{\text{WR}}$	I	Processor Interface Write Strobe. C(7:0) is written to Control Words selected by A(2:0) in the Programmable Down Converter on the rising edge of this signal. See Microprocessor Write Section.
$\overline{\text{RD}}$	I	Processor Interface Read Strobe. C(7:0) is read from output or status locations selected by A(2:0) in the Programmable Down Converter on the falling edge of this signal. See Microprocessor Read Section.
REFCLK	I	Reference Clock. Used as an input clock for the timing error detector. The timing error is computed relative to REFCLK. REFCLK frequency must be less than or equal to PROCCLK/2.
MSYNCO	O	Multiple Chip Sync Output. Provided for synchronizing multiple parts when CLKIN and PROCCLK are asynchronous. MSYNCO is the synchronization signal between the input section operating under CLKIN and the back end processing operating under PROCCLK. This output sync signal from one part is connected to the MSYNCI signal of all the HSP50214As.
MSYNCI	I	Multiple Chip Sync Input. The MSYNCI pin of all the parts should be tied to the MSYNCO of one part. ***NOTE: MSYNCI must be connected to an MSYNCO signal for operation.***
SYNCIN1	I	CIC Decimation/Carrier NCO Update Sync. Can be used to synchronize the CIC Section, carrier NCO update, or both. See the Multiple Chip Synchronization Section and Control Word 0 in the Microprocessor Write Section. Active High.
SYNCIN2	I	FIR/Timing NCO Update/AGC Gain Update Sync. Can be used to synchronize the FIR, Timing NCO update, AGC gain update, or any combination of the above. See the Multiple Chip Synchronization Section and Control Words 7, 8, and 10 in the Microprocessor Write Section. Active High.
SYNCOUT	O	Strobe Output. This synchronization signal is generated by the µP interface for synchronizing multiple parts. Can be generated by PROCLK or CLKIN (see Control Word 0 and Control Word 24 in the Microprocessor Write Section). Active High.

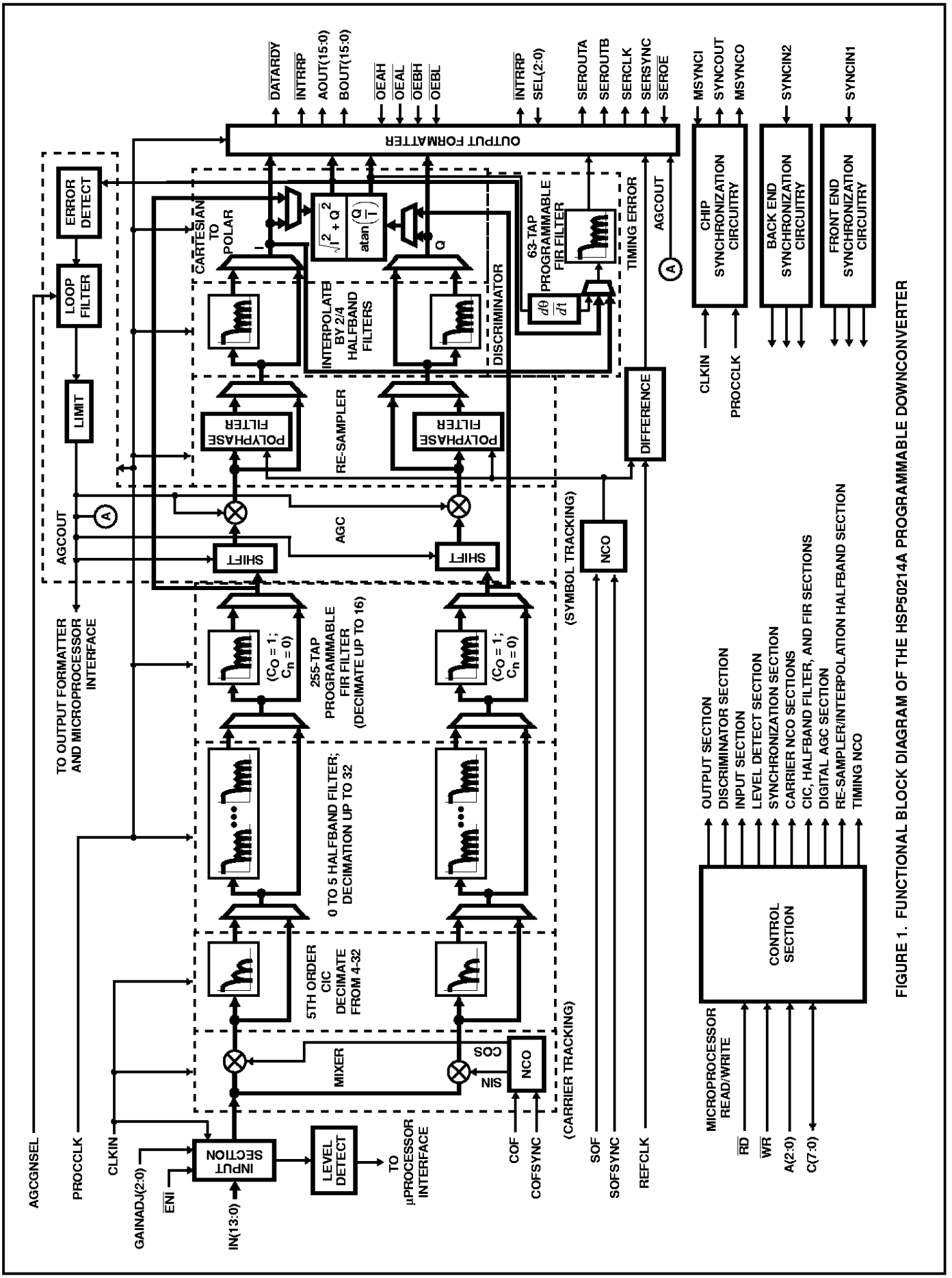


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF THE HSP50214A PROGRAMMABLE DOWNCONVERTER

Functional Description

The HSP50214A Programmable Downconverter (PDC) is an agile digital tuner designed to meet the requirements of a wide variety of communications industry standards. The PDC contains the processing functions needed to convert sampled IF signals to baseband digital samples. These functions include LO generation/mixing, decimation filtering, programmable FIR shaping/bandlimiting filtering, resampling, Automatic Gain Control (AGC), frequency discrimination and detection as well as multi-chip synchronization. The HSP50214A interfaces directly with a DSP microprocessor to pass baseband and status data.

A top level functional block diagram of the HSP50214A is shown in Figure 1. The diagram shows the major blocks and multiplexers used to reconfigure the data path for various architectures. The HSP50214A can be broken into 13 sections: Synchronization, Input, Input Level Detector, Carrier Mixer/Numerically Control Oscillator (NCO), CIC Decimating Filter, Halfband Decimating Filter, 255-Tap Programmable FIR Filter, Automatic Gain Control (AGC), Re-sampler/Halfband Filter, Timing NCO, Cartesian to Polar Converter, Discriminator, and Output Sections. All of these sections are configured through a microprocessor interface.

The HSP50214A has three clock inputs; two are required and one is optional. The input level detector, carrier NCO, and CIC decimating filter sections operate on the rising edge of the input clock, CLKIN. The halfband filter, programmable FIR filter, AGC, Re-Sampler/Halfband filters, timing NCO, discriminator, and output sections operate on the rising edge of PROCCLK. The third clock, REFCLK, is used to generate timing error information.

NOTE: All of the clocks may be asynchronous.

PDC Applications Overview

This section highlights the motivation behind the key programmable features from a communications system level perspective. These motivations will be defined in terms of ability to provide DSP processing capability for specific modulation formats and communication applications. The versatility of the Programmable Downconverter can be intimidating because of the many Control Words required for chip configuration. This section provides system level insight to help allay reservations about this versatile DSP product. It should help the designer capitalize on the greatest feature of the PDC - ***VERSATILITY THROUGH PROGRAMMABILITY***. It is this feature, when fully understood, that brings the greatest return on design investment by offering a single receiver design that can process the many waveforms required in the communications marketplace.

FDM Based Standards and Applications

Table 1 provides an overview of some common frequency division multiplex (FDM) base station applications to which the PDC can be applied. The PDC provides excellent selectivity for frequency division multiple access (FDMA) signals. This high selectivity is achieved with 0.012Hz resolution frequency control of the NCO and the sharp filter responses capable with a 255-tap, 22-bit coefficient FIR filter. The 16-bit resolution out of the Cartesian to Polar Coordinate Converter are routed to the frequency detector, which is followed by a 63-tap, 22-bit coefficient FIR filter structure for facilitating FM and FSK detection. The 14-bit input resolution is the smallest bit resolution found throughout the conversion and filtering sections, providing excellent dynamic range in the DSP processing. A unique input gain scaler adds an additional 42dB of range to the input level variation, to compensate for changes in the analog RF front end receive equipment. Synchronization circuitry allows precise timing control of the base station reconfiguration for all receive channels simultaneously. Portions of this table were corroborated with reference [2].

TABLE 1. CELLULAR PHONE BASE STATION APPLICATIONS USING FDMA

STANDARD	AMPS (IS-91)	MCS-L1 MCS-L2	NMT-400 NMT-900	C450	ETACS NTACS
RX BAND (MHz)	824-849	925-940	453-458 890-915	451-456	871-904 915-925
CHANNEL BW (kHz)	30	25.0 12.5	25 12.5	20.0 10.0	25.0 12.5
# TRAFFIC CHANNELS	832	600 1200	200 1999	222 444	1240 800
VOICE MODULATION	FM	FM	FM	FM	FM
PEAK DEVIATION (kHz)	12	5	5	4	9.5
CONTROL MODULATION	FSK	FSK	FSK	FSK	FSK
PEAK DEVIATION (kHz)	8	4.5	3.5	2.5	6.4
CONTROL CHANNEL RATE (Kbps)	10	0.3	1.2	5.3	8

TDM Based Standards and Applications

Table 2 provides an overview of some common Time Division Multiplexed (TDM) base station applications to which the PDC can be applied. For time division multiple access (TDMA) applications, such as North American TDMA (IS136), where 30kHz is the received band of interest for the PCS basestation, the PDC offers 0.012Hz frequency resolution in downconversion in addition to $\alpha = 0.35$ matched (programmable) filtering capability. The $\pi/4$ DPSK modulation can be processed using the PDC Cartesian to Polar coordinate converter and $d\phi/dt$ detector circuitry or by processing the I/Q samples in the DSP μP. The PDC provides the ability to change the received signal gain and frequency, synchronous with burst timing. The synchronous gain adjustment allows the user to measure the power of the signal at the A/D at the end of a burst, and synchronously reload that same gain value at the arrival of the next user burst.

For applications other than cellular phones (where the preambles are not changed), the PDC frequency discriminator output can be used to obtain correlation on the preamble pattern to aid in burst acquisition.

TABLE 2. CELLULAR BASESTATION APPLICATIONS USING TDMA

STANDARD	GSM	PCN	IS-54
TYPE	Cellular	Cellular	Cellular
BASESTATION RX BAND (MHz)	935-960	1805-1880	824-849
CHANNEL BW (kHz)	200	200	30
# TRAFFIC CHANNELS	8	16	3
VOICE MODULATION	GMSK	GMSK	$\pi/4$ DQPSK
CHANNEL RATE (Kbps)	270.8	270.8	48.6
CONTROL MODULATION	GMSK	GMSK	$\pi/4$ DQPSK
CHANNEL RATE (Kbps)	270.8	270.8	48.6

Several applications are combinations of frequency and time domain multiple access schemes. For example, GSM is a TDMA signal that is frequency hopped. The individual channels contain Gaussian MSK modulated signals. The PDC again offers the 0.012Hz tuning resolution for de-hopping the received signal. The combination of halfband and 256-tap programmable, 22-bit coefficient FIR filters readily performs the necessary matched filtering for demodulation and optimum detection of the GMSK signals.

CDMA Based Standards and Applications

For Code Division Multiple Access (CDMA) type signals, the PDC offers the ability to have a single wideband RF front end, from which it can select a single spread channel of interest. The synchronization circuitry provides for easy control of multiple PDC for applications where multiple received signals are required, such as base-stations.

In IS-95 CDMA, the receive signal bandwidth is approximately 1.2288MHz wide with many spread spectrum channel in the band. The PDC supplies the downconversion and filtering required to receive a single RF channel in the presence of strong adjacent interference. Multiple PDC's would be sourced from a single receive RF chain, each processing a different receive frequency channel. The despreader would usually follow the PDC. In some very specific applications, with short, fixed codes, the filtering and despreading may be possible with innovative use of the programmable, 22-bit coefficient FIR filter. The PDC offers 0.012Hz resolution on tuning to the desired receive channel and excellent rejection of the portions of the band not being processed, via the halfband and 255-tap programmable, 22-bit coefficient FIR filter.

Traditional Modulation Formats

AM, ASK, FM and FSK

The PDC has the capability to fully demodulate AM and FM modulated waveforms. The PDC outputs 15 bits of amplitude or 16 bits of frequency for these modulation formats. The FM discriminator has a 63-tap programmable, 22-bit coefficient FIR filter for additional signal conditioning of the FM signal. Digital versions of these formats, ASK and FSK are also readily processed using the PDC. Just as in the AM modulated case, ASK signals will use 15-bit magnitude output of the Cartesian to Polar Coordinate converter. Multi-tone FSK can be processed several ways. The frequency information out of the discriminator can be used to identify the received tone, or the filter can be used to identify and power detect a specific tone of the received signal. AMPS is an example of an FM application.

PM and PSK

The PDC provides the downconversion, demodulation, matched filtering and coordinate conversion required for demodulation of PM and PSK modulated waveforms. These modulation formats will require external carrier and symbol timing recovery loop filters to complete the receiver design. The PDC was designed to interface with the HSP50210 Digital Costas Loop to implement the carrier phase and symbol timing recovery loop filters (for continuous PSK signals - not burst).

Digital modulation formats that combine amplitude and phase for symbol mapping, such as m-ary QAM, can also be downconverted, demodulated, and matched filtered. The received symbol information is provided with 16 bits of resolution in either Cartesian or Polar coordinates to facilitate remapping into bits and to recover the carrier phase. External Symbol mapping and Carrier Recovery Loop Filtering is required for this waveform.

Resampling and Interpolation Filters

Two key features of the resampling FIR filter are that the resampler filter allows the output sample rate to be programmed with millihertz resolution and that the output sample rate can be phase locked to an independent separate clock. The resampler frees the front end sampling clocks from having to be synchronous or integrally related in rate to the baseband output. The asynchronous relationship between front end and back end clocks is critical in applications where ISDN interfaces drive the baseband interfaces, but the channel sample rates are not related in any way. The interpolation halfband filters can increase the rate of the output when narrow frequency bands are being processed. The increase in output rate allows maximum use of the programmable FIR while preserving time resolution in the baseband data.

14-Bit Input and Processing Resolution

The PDC maintains a minimum of 14 bits of processing resolution through to the output, providing over 84dB of dynamic range. The 18 bits of resolution on the internal references provide a spurious floor that is better than 98dBc. Furthermore, the PDC provides up to 42dB of gain scaling to compensate for any change in gain in the RF front end as well as up to 96dB of gain in the internal PDC AGC. This gain maximizes the output resolution for small signals and compensates for changes in the RF front end gain, to handle changes in the incoming signal.

Summary

The greatest feature of the PDC is its ability to be reconfigured to process many common standards in the communications industry. Thus, a single hardware element can receive and process a wide variety of signals from PCS to traditional cellular, from wireless local loop to SATCOM. The high resolution frequency tuning and narrowband filtering are instrumental in almost all of the applications.

Multiple Chip Synchronization

Multiple PDCs are synchronized using a MASTER/SLAVE configuration. One part is responsible for synchronizing the front end internal circuitry using CLKIN while another part is responsible for synchronizing the backend internal circuitry using PROCCLK.

The PDC is synchronized with other PDCs using five control lines: SYNCOUT, SYNCIN1, SYNCIN2, MSYNCO, and MSYNCI. Figure 2 shows the interconnection of these five signals for multiple chip synchronization where different sources are used for CLKIN and PPOCCLK.

PDC A is the Master sync through MSO.

PDC B configures the CLKIN sync through SYNCIN1.

PDC A configures the PROCCLK sync through SYNCIN2.

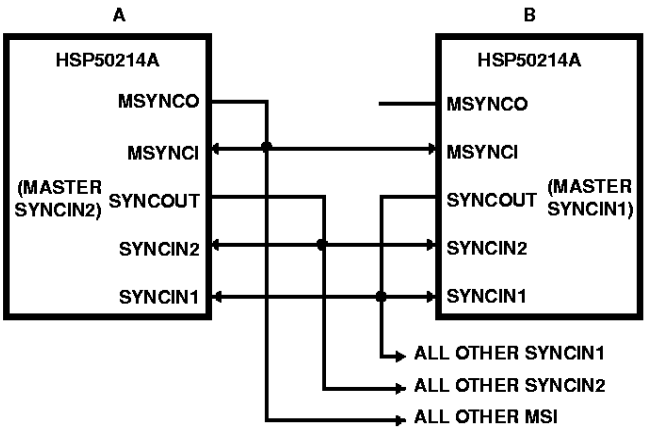


FIGURE 2. SYNCHRONIZATION CIRCUIT

SYNCOUT for PDC B should be set to be synchronous with CLKIN (Control Word 0, Bit 3 = 0. See the Microprocessor Write Section). SYNCOUT for PDC B is tied to the SYNCIN1 of all the PDCs. The SYNCIN1 can be programmed so that the carrier NCO and/or the 5th order CIC filter of all PDCs can be synchronously loaded/updated using SYNCIN1. See Control Word 0, Bits 19 and 20 in the Microprocessor Write Section for details.

SYNCOUT for one of the PDC's other than PDC B, should be set for PROCCLK (bit 3 = 1 in Control Word 0). This output signal is tied to the SYNCIN2 of all PDCs. The SYNCIN2 can be programmed so that the AGC updates its accumulator with the contents in the master registers (Control Word 8, Bit 29 in the Microprocessor Write Section). SYNCIN2 is also used to load or reset the timing NCO using bit 5, Control Word 11. The halfband and FIR filters can be reset on SYNCIN2 using Control Word 7, Bit 21. The MSYNCO of one of the PDCs is then used to drive the MSYNCI of all the PDCs (including its own).

For application configurations where CLKIN and PROCCLK have the same source, SYNCIN1 and SYNCIN2 can be tied together. However, if different enabling is desired for the front end and backend processing of the PDC's, these signals can still be controlled independently.

In the HSP50214A, the Control Word 25 reset signal has been extended so that the front end reset is 10 CLKIN periods wide and the back end reset is 10 PROCCLK periods wide. This guarantees that no enables will be caught in the pipelines. In addition, the SYNCIN1 internal reset signal, which is enabled by setting Control Word 7, Bit 21 = 1, has been extended to 10 cycles.

In summary, SYNCIN1 is used to update carrier phase offset, update carrier center frequency, reset CIC decimation counters and reset the carrier NCO (clear the feedback in the NCO). SYNCIN2 is used to reset the HB filter, FIR filter, re-sampler/HB state machines and the output FIFO, load a new gain into the AGC and load a new re-sampler NCO center frequency and phase offset.

Input Section

The block diagram of the input controller is provided in Figure 3. The input can support offset binary or two's complement data and can be operated in gated or interpolated mode (see Control Word 0 from the Microprocessor Write Section). The gated mode takes one sample per clock when the input enable (ENI) is asserted. The gated mode allows the user to synchronize a low speed sampling clock to a high speed CLKIN.

The interpolated mode allows the user to input data at a low sample rate and to zero-stuff the data prior to filtering. This zero stuffing effectively interpolates the input signal up to the rate of the input clock (CLKIN). This interpolated mode allows the part to be used at rates where the sampling frequency is above the maximum input rate range of the halfband filter section, and where the desired output bandwidth is too wide to use a Cascaded Integrator Comb (CIC) filter without significantly reducing the dynamic range. See Figures 4-7 for an interpolated input example, detailing the associated spectral results.

Interpolation Example:

The specifications for the interpolated input example are:

Input Sample Rate = 5 MSPS
PROCCLK = 28MHz
Interpolate by 8, Decimate by 10
Desired 85dB dynamic range output bandwidth = 500kHz

Input Level Detector

The Input Level Detector Section measures the average magnitude error at the PDC input for the microprocessor by comparing the input level against a programmable threshold and then integrating the result. It is intended to provide

a gain error for use in an AGC loop with either the RF/IF or A/D converter stages (see Figure 8). The AGC loop includes Input Level Detector, the microprocessor and an external gain control amplifier (or attenuator). The input samples are rectified and added to a threshold programmed via the microprocessor interface, as shown in Figure 9. The bit weighting of the data path through the input threshold detector is shown in Figure 10. The threshold is a signed number, so it should be set to the inverse of the desired input level. The threshold can be set to zero if the average input level is desired instead of the error. The sum of the threshold and the absolute value of the input is accumulated in a 32-bit accumulator. The accumulator can handle up to 2^{18} samples without overflow. The integration time is controlled by an 18-bit counter. The integration counter preload (ICPrel) is programmed via the microprocessor interface through Control Word 1. Only the upper 16 bits are programmable. The 2 LSBs are always zero. Control Word 1, Bits 29-14 are programmed to:

$$ICPrel = (N)/4 + 1 \quad \text{(EQ. 1)}$$

where N is the desired integration period, defined as the number of input samples to be integrated. N must be a multiple of 4: [0, 4, 8, 12, 16 .... , 2^{18}].

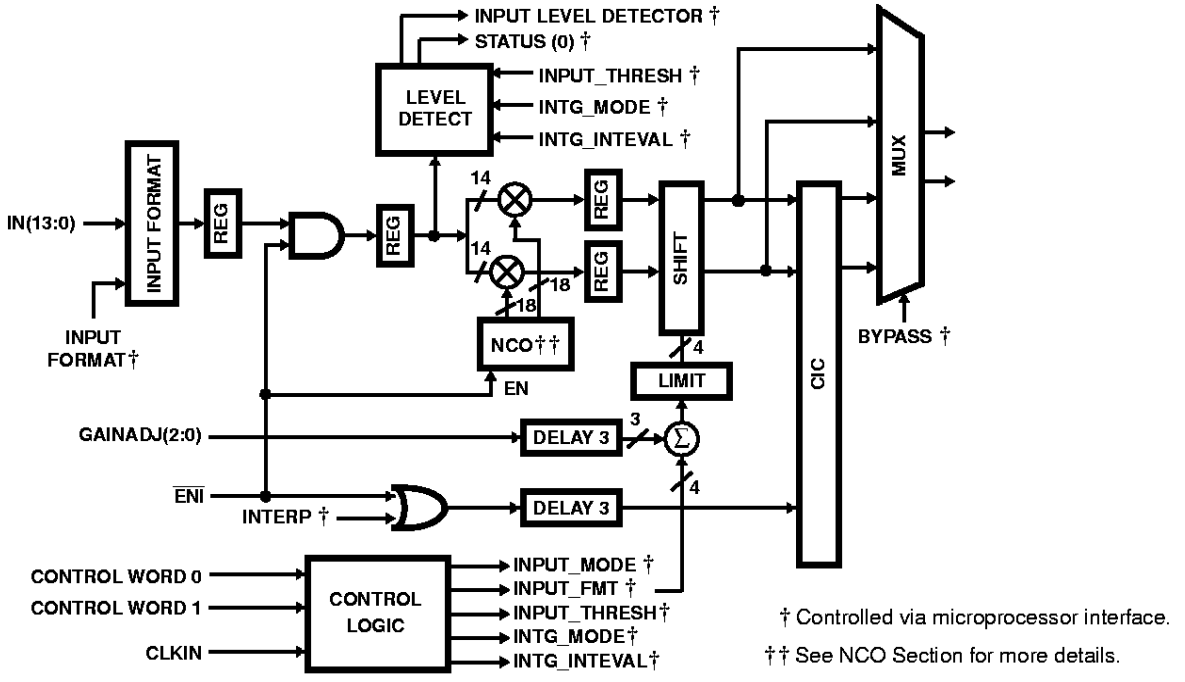
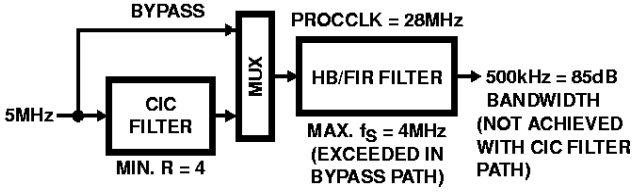


FIGURE 3. BLOCK DIAGRAM OF THE INPUT SECTION



Without Interpolation, the CIC bypass path exceeds the HB/FIR filter input sample rate and the CIC filter path will not yield the desired 85dB dynamic range band width of 500kHz.

FIGURE 4. STATEMENT OF THE PROBLEM

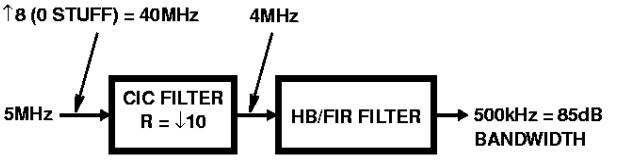


FIGURE 5. BLOCK DIAGRAM OF THE INTERPOLATION APPROACH