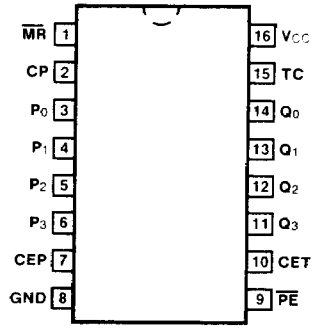
9310 • 9316
93L10 • 93L16
93S10 • 93S16

BCD DECADE COUNTER/ 4-BIT BINARY COUNTER

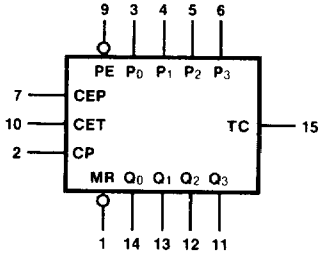
DESCRIPTION — The '10 is a high speed synchronous BCD decade counter and the '16 is a high speed synchronous 4-bit binary counter. They are synchronously presetable, multifunctional MSI building blocks useful in a large number of counting, digital integration and conversion applications. Several states of synchronous operation are obtainable with no external gating packages required through an internal carry lookahead counting technique.

- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY CIRCUITRY**
- **EASY INTERFACING WITH DTL, LPDTL, AND TTL FAMILIES**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

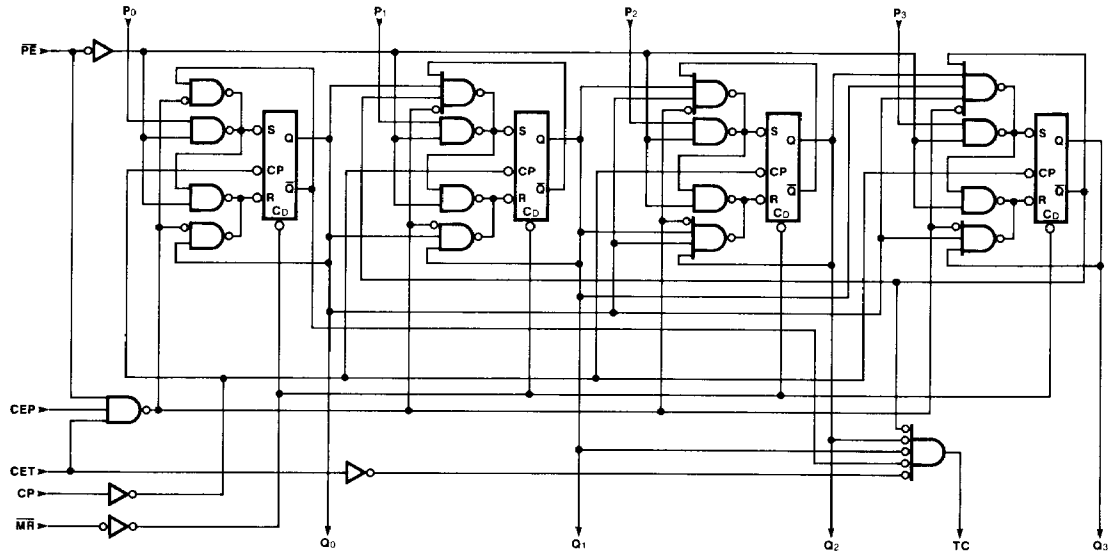
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	9310PC, 9316PC 93L10PC, 93L16PC 93S10PC, 93S16PC		9B
Ceramic DIP (D)	A	9310DC, 9316DC 93L10DC, 93L16DC 93S10DC, 93S16DC	9310DM, 9316DM 93L10DM, 93L16DM 93S10DM, 93S16DM	6B
Flatpak (F)	A	9310FC, 9316FC 93L10FC, 93L16FC 93S10FC, 93S16FC	9310FM, 9316FM 93L10FM, 93L16FM 93S10FM, 93S16FM	4L

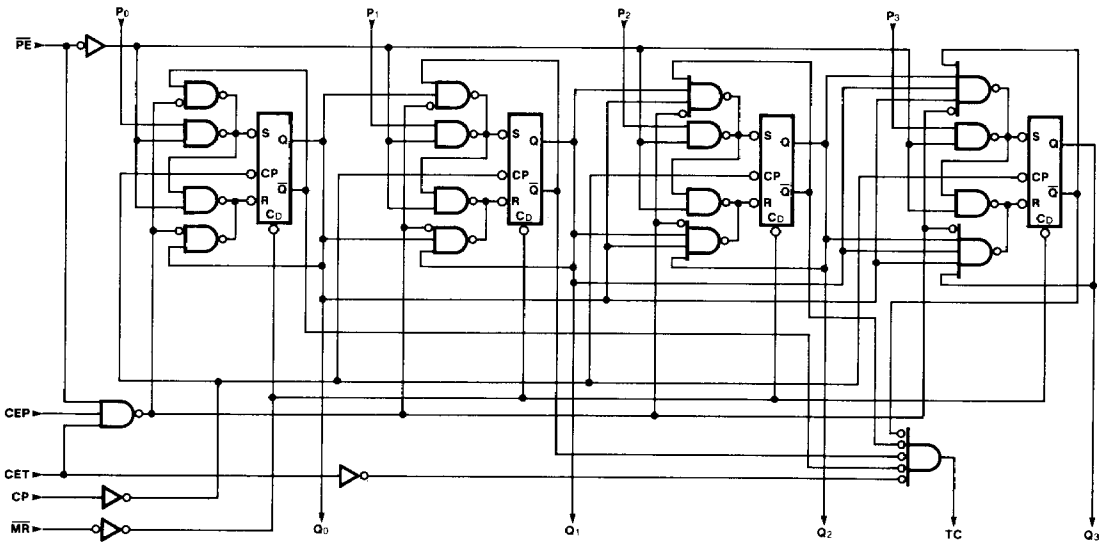
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	93XX (U.L.) HIGH/LOW	93L (U.L.) HIGH/LOW	93S (U.L.) HIGH/LOW
CEP	Count Enable Parallel Input	1.0/1.0	0.5/0.25	2.5/2.5
CET	Count Enable Trickle Input	2.0/2.0	1.0/0.5	3.1/3.1
CP	Clock Pulse Input (Active Rising Edge)	2.0/2.0	1.0/0.5	3.1/3.1
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	0.5/0.25	1.25/1.25
P0 — P3	Parallel Data Inputs	0.67/0.67	0.33/0.17	1.25/1.25
$\overline{PE}$	Parallel Enable Input (Active LOW)	2.0/2.0	1.0/0.5	2.5/2.5
Q0 — Q3	Flip-flop Outputs	16/8.0	10/5.0 (3.0)	20/10
TC	Terminal Count Output	20/10	10/5.0 (3.0)	25/12.5

LOGIC DIAGRAMS
'10, 'L10

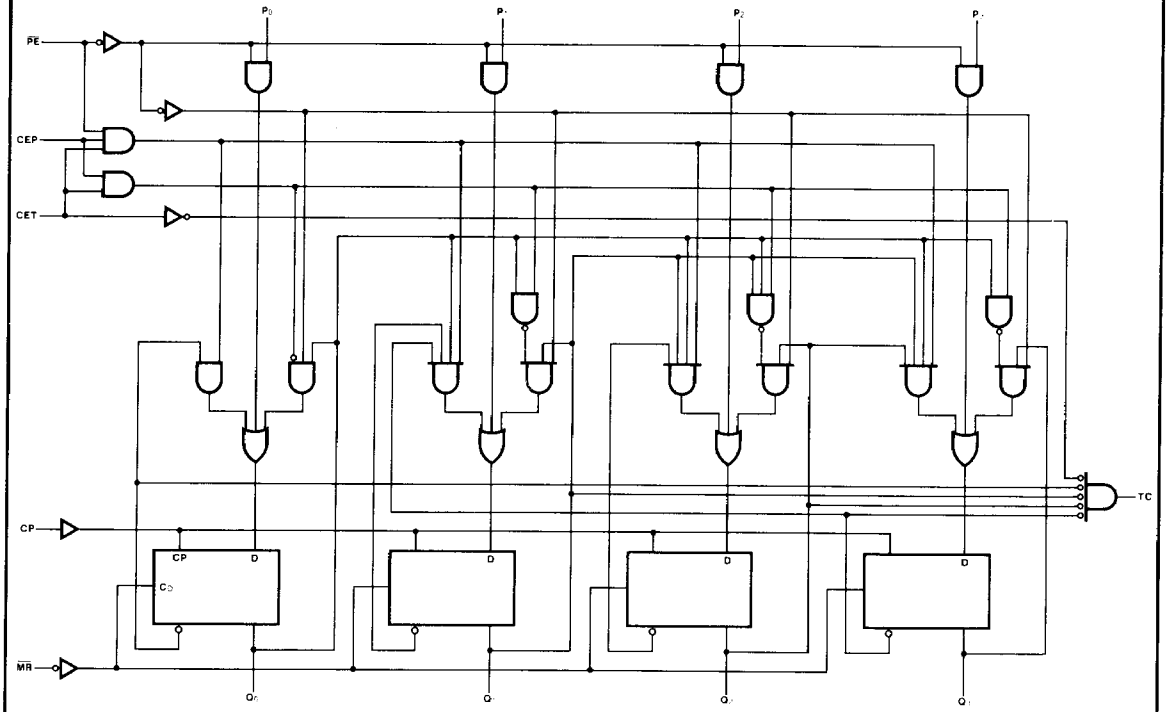


'16, 'L16

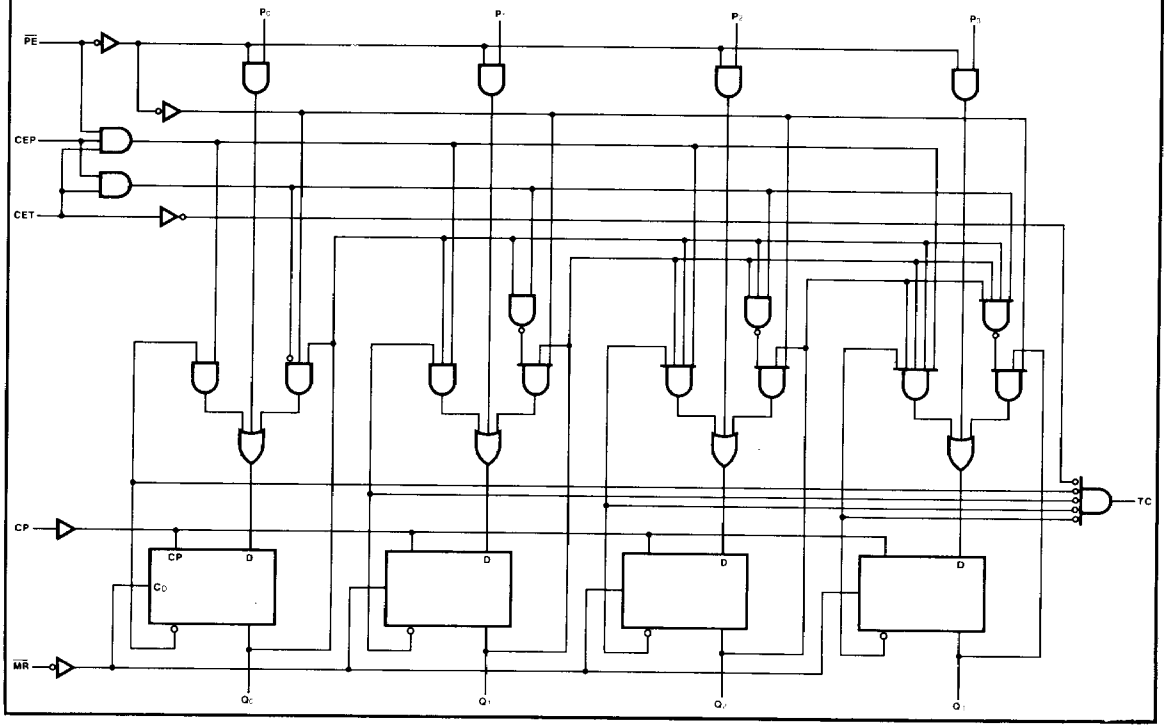


LOGIC DIAGRAMS

'S16



'S10



FUNCTIONAL DESCRIPTION — The '10 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it increments to state 0 (LLLL). The '16 counts modulo-16 in binary sequence. From state 15 (HHHH) it increments to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset, parallel load, count-up and hold. Four control inputs — Master Reset ($\overline{MR}$) Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The TTL and LP-TTL versions ('10, '16, 'L10 and 'L16 as opposed to the 'S10 and 'S16) contain masterslave flip-flops which are "next-state catching" because of the JK feedback. This means that when CP is LOW, information that would change the state of a flip-flop, whether from the counting logic or the parallel entry logic if either mode is momentarily enabled, enters the master and is locked in. Thus to avoid inadvertently changing the state of a master latch, and the subsequent transfer of the erroneous information to the slave when the clock rises, it is necessary to insure that neither the counting mode, nor the parallel entry mode is momentarily enabled while CP is LOW. The S-TTL versions ('S10 and 'S16) use D-type edge-triggered flip-flops and changing the $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in its maximum count state (9 for the decade counters, 15 for the binary counters — fully decoded in both types). To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. These two schemes are shown in *Figures a and b*. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the state diagrams.

Multistage Counting — The '10/'16 counters may be cascaded to provide multistage synchronous counting. Two methods commonly used to cascade these counters are shown in *Figures a and b*.

In multistage counting, all less significant stages must be at their terminal count before the next more significant counter is enabled. The '10/'16 internally decodes the terminal count condition and "ANDs" it with the CET input to generate the terminal count (TC) output. This arrangement allows one to perform series enabling by connecting the TC output (enable signal) to the CET input of the following stage, *Figure a*. The setup requires very few interconnections, but has the following drawback: since it takes time for the enable to ripple through the counter stages, there is a reduction in maximum counting speed. To increase the counting rate, it is necessary to decrease the propagation delay of the TC signal, which is done in the second method.

The scheme illustrated in *Figure b* permits multistage counting, limited by the fan-out of the terminal count. The CEP input of the '10/'16 is internally "ANDed" with the CET input and as a result, both must be HIGH for the counter to be enabled. The CET inputs are connected as before except for the second stage. There the CET input is left floating and is therefore HIGH. Also, all CEP inputs are connected to the terminal output of the first stage. The advantage of this method is best seen by assuming all stages except the second and last are in their terminal condition. As the second stage advances to its terminal count, an enable is allowed to trickle down to the last counter stage, but has the full cycle time of the first counter to reach it. Then as the TC of the first stage goes active (HIGH), all CEP inputs are activated, allowing all stages to count on the next clock.

MODE SELECT TABLE

INPUTS					RESPONSE
$\overline{MR}$	$\overline{PE}$	CEP	CET	CP	
L	X	X	X	X	Clear; All Outputs LOW
H	L	X	X	↑	Parallel Load; $P_n \rightarrow Q_n$
H	H	L	X	X	Hold
H	H	X	L	X	Hold; TC = LOW
H	H	H	H	↑	Count Up

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC EQUATIONS

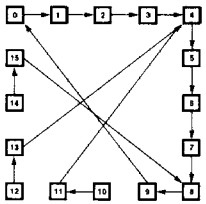
Count Enable = MR • PE • CEP • CET

Terminal Count = CET • Q_0 • Q_1 • Q_2 • Q_3 ('16)

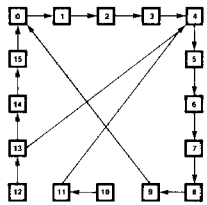
Terminal Count = CET • Q_0 • $\overline{Q}_1$ • $\overline{Q}_2$ • Q_3 ('10)

STATE DIAGRAMS

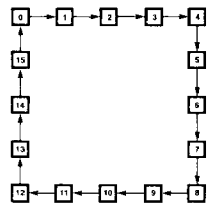
'S10



'10, 'L10



'16, 'S16, 'L16



NOTE: The '20 can be preset to any state, but will not count beyond 9. If preset to state 10,11,12,13,14 or 15, it will return to its normal sequence within two clock pulses.

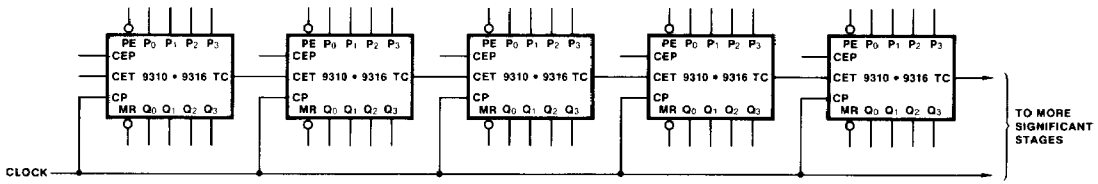


Fig. a Synchronous Multistage Counting Scheme (Slow)

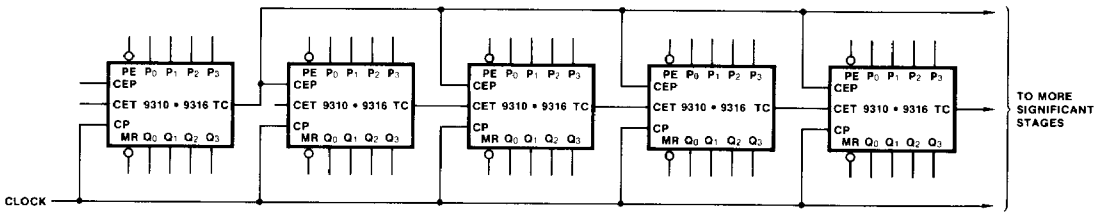


Fig. b Synchronous Multistage Counting Scheme (Fast)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	93XX		93L		93S		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
I_{OS}	Output Short Circuit Current	-20	-80	-2.5	-25	-40	-100	mA	V_{CC} = Max
I_{CC}	Power Supply Current		92		27.5		127	mA	V_{CC} = Max, $\overline{MR}$ = Gnd

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	93XX		93L		93S		UNITS	CONDITIONS
		C_L = 15 pF		C_L = 15 pF		C_L = 15 pF			
		Min	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	30		13		70		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q		20 23		32 39		9.0 13	ns	
t_{PLH} t_{PHL}	Propagation Delay CP to TC		35 22		66 30		18 12	ns	
t_{PLH} t_{PHL}	Propagation Delay CET to TC		19 19		35 30		10 10	ns	Figs. 3-1, 3-5
t_{PHL}	Propagation Delay $\overline{MR}$ to Q		45		62		20	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	93XX		93L		93S		UNITS	CONDITIONS
		Min	Max	Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW P_n to CP	30 30		75 75		8.0 5.0		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW P_n to CP	0 0		10 10		0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{PE}$ to CP	Note 2 30		Note 2 53		10 5.0		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{PE}$ to CP	-7.0 Note 2		7.0 Note 2		0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW CEP or CET to CP	22 Note 1		26 Note 1		9.0 7.5		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW CEP or CET to CP	Note 1 0		Note 1 10		0 0		ns	
t_w (H) t_w (L)	CP Pulse Width	17 17		25 25		6.5 7.0		ns	Fig. 3-8
t_w (L)	$\overline{MR}$ Pulse Width LOW	30		65		14		ns	Fig. 3-16
t_{rec}	Recovery Time $\overline{MR}$ to CP	15		55		5.5		ns	Fig. 3-16

NOTES:
(1) The Setup Time "t_s (L)" and Hold Time "t_h (H)" between the Count Enable (CEP and CET) and the Clock (CP) indicate that the HIGH-to-LOW transition of the CEP and CET must occur only while the Clock is HIGH for conventional operation.
(2) The Setup Time "t_s (H)" and Hold Time "t_h (L)" between the Parallel Enable ($\overline{PE}$) and Clock (CP) indicate that the LOW-to-HIGH transition of the $\overline{PE}$ must occur only while the Clock is HIGH for conventional operation.

6