1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 14-bit digital-to-analog converter. The device is configured to accept right-justified data in two bytes from an 8-bit data bus. A novel low-leakage configuration enables the AD7534 to exhibit excellent output leakage current characteristics over the specified temperature range.

1.2 Part Number.

The complete part numbers per Table 1 of this specification are as follows:

Device	Part Number
−1	AD7534SQ/883B
−2	AD7534TQ/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: Q-20

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{DD} (Pin 19) to DGND	−0.3V, +17V
V_{SS} (Pin 20) to AGND	−15V, +0.3V
V_{REF} (Pin 1) to AGND	±25V
V_{RFB} (Pin 2) to AGND	±25V
Digital Input Voltage (Pins 7-18) to DGND	−0.3V, V_{DD}
V_{PIN3} to DGND	−0.3V, V_{DD}
AGND to DGND	−0.3V, V_{DD}
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W
θ_{JA} = 120°C/W

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Table 1.

Test	Symbol	Device[2]	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2,3	Sub Group 4	Test Condition[1]	Units
Resolution	RES	–1,2	14					Bits
Relative Accuracy	RA	–1 –2	±2 ±1	±2 ±2	±2 ±1	 ±1		 LSB max
Differential Nonlinearity	DNL	–1,2	±1	±1	±1	±1	Guaranteed Monotonic to 14-Bits	LSB max
Gain Error[2]	A_E	–1 –2	±8 ±4	±8 ±8	±8 ±4	 ±4		LSB max
Gain Tempco	TC_{AE}	–1 –2	±5 ±2.5					ppm/°C max
Supply Rejection ($\Delta Gain/\Delta V_{DD}$)		–1,2	±0.02	±0.01	±0.02		ΔV_{DD} = ±5%	% per % max
Output Leakage Current (Pin 3)	I_{OUT}	–1,2	±20	±5	±20		V_{SS} = –300mV (DAC Register Loaded with All 0's)	nA max
		–1,2	±150	±5	±150		V_{SS} = 0V	nA max
Output Current Settling Time @ 25°C	t_{SL}	–1,2	1.5				To 0.003% of FSR. I_{OUT} Load = 100Ω, C_{EXT} = 13pF. DAC Register Alternately Loaded with All 1's and All 0's.	µs max
Feedthrough Error[3]	FT	–1,2	10				V_{REF} = ±10V, 10kHz Sine Wave DAC Register Loaded with All 0's	mV p-p max
Input Resistance, Pin 1	R_{IN}	–1,2	3.5	3.5	3.5		Typical Input Resistance = 6kΩ	kΩ min
			10	10	10			kΩ max
Input High Voltage	V_{IH}	–1,2	2.4	2.4	2.4			V min
Input Low Voltage	V_{IL}	–1,2	0.8	0.8	0.8			V max
Input Leakage Current	I_{IN}	–1,2	±10	±1	±10		V_{IN} = 0V or V_{DD}	µA max
Input Capacitance	C_{IN}	–1,2	7					pF max
Analog Output Capacitance: (Pin 3)	C_{OUT}	–1,2	260 130				DAC Register Loaded with All 1's DAC Register Loaded with All 0's	pF max
Address Valid to Write Setup Time	t_{AWS}	–1,2	0					ns min
Address Valid to Write Hold Time	t_{AWH}	–1,2	0					ns min
Data Setup Time	t_{DS}	–1,2	180					ns min
Data Hold Time	t_{DH}	–1,2	30					ns min
Chip Select to Write Setup Time	t_{CWS}	–1,2	0					ns min
Chip Select to Write Hold Time	t_{CWH}	–1,2	0					ns min
Write Pulse Width	t_{WR}	–1,2	240					ns min
Power Supply Voltage Range	V_{DD}	–1,2	11.4				Specs Guaranteed Over This Range	V min
			15.75					V max
	V_{SS}	–1,2	–200				Specs Guaranteed Over This Range	mV min
			–500					mV max
Power Supply Current	I_{DD}	–1,2	3	3	3		All Digital Inputs V_{IL} or V_{IH}	mA max
			500	500	500		All Digital Inputs 0 or V_{DD}	µA max

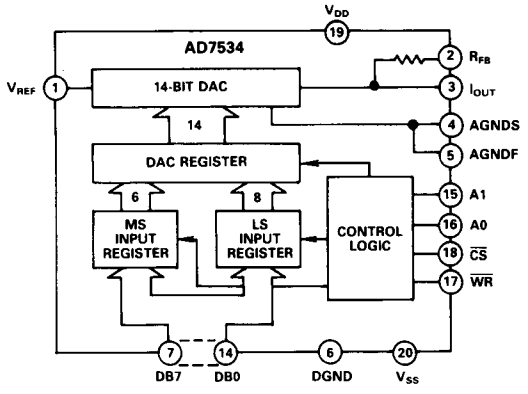
NOTES

[1] V_{DD} = +12V to 15V; V_{REF} = +10V, $V_{PIN3} = V_{PIN4}$ = 0V, V_{SS} = –300mV unless otherwise stated. Specifications are guaranteed for a V_{DD} of +12V to +15V with a tolerance of ±5%; testing is performed at 12V and 15V only. At V_{DD} = 5V, the device is fully functional with a slight degradation in performance.

[2] Measured using internal feedback resistor and includes effects of leakage current and gain T.C.

[3] Feedthrough can be further reduced by connecting the metal lid to ground.

3.2.1 Functional Block Diagram and Terminal Assignments.



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (81).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883, Method 1005. Burn-in is per MIL-STD-883 Method 1015, Test Condition (B).