CS4354

5-V Stereo DAC with 2-V_{RMS} Ground-Centered Output

Features

- Advanced multibit delta–sigma modulator
- 101 dB A-weighted dynamic range
- –86 dB THD+N
- Single-ended ground-centered analog architecture
  - No DC-blocking capacitors required
  - Integrated inverting charge pump
  - Filtered line-level outputs
  - 2 V_{RMS} full-scale output
- Low-latency digital filtering
- Supports sample rates up to 192 kHz
- 24-bit I²S input
- +5-V analog supply with integrated inverting charge pump and regulator for core logic, and +1.8-V to +5-V interface power supplies
- 50-mW power consumption
- 14-pin SOIC, lead-free assembly

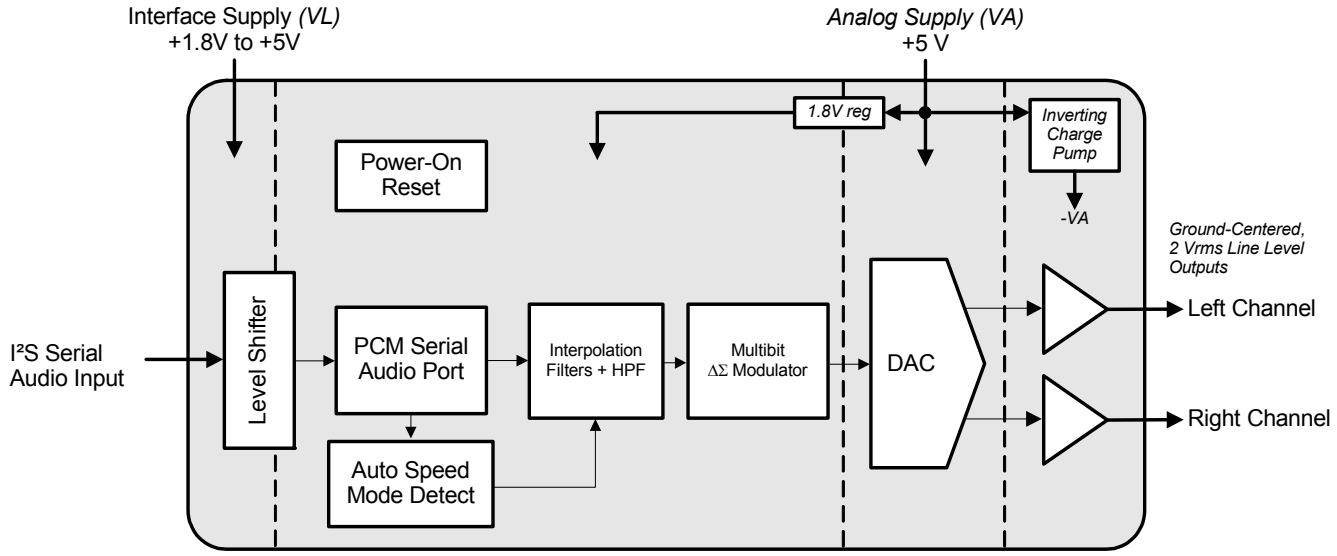
Description

The CS4354 is a complete stereo digital-to-analog system including digital interpolation, third-order multi-bit delta–sigma digital-to-analog conversion, digital de-emphasis, analog filtering, and on-chip 2 V_{RMS} line-level driver from a 5 V supply.

The advantages of this architecture include ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature, high tolerance to clock jitter, and a minimal set of external components.

These features are ideal for cost-sensitive, two-channel audio systems including video game consoles, Blu-Ray Disc® and DVD players, set-top boxes, digital TVs, and DAB/DMB devices.

The CS4354 is available in a 14-pin SOIC package in Commercial (–40°C to +85°C) grade. The CDB4354 Customer Demonstration Board is also available for device evaluation and implementation suggestions. Please see "Ordering Information" on page 23 for complete details.



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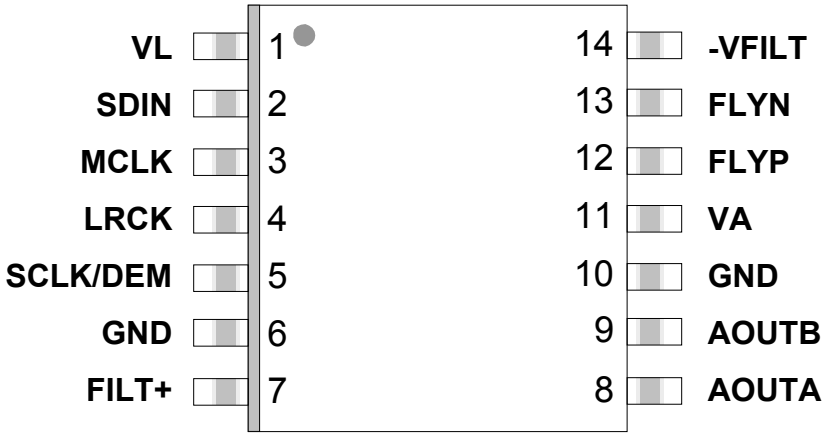


Pin Name	Pin #	Pin Description
VL	1	**Serial Audio Interface Power** (*Input*) **-** Positive power for the serial audio interface.
SDIN	2	**Serial Audio Data Input** (*Input*) - Input for two's complement serial audio data.
MCLK	3	**Master Clock** (*Input*) - Clock source for the delta-sigma modulator and digital filters.
LRCK	4	**Left / Right Clock** (*Input*) - Determines which channel, Left or Right, is currently active on the serial audio data line.
SCLK/DEM	5	**Serial Clock** (*Input*) - Serial clock for the serial audio interface.
FILT+	7	**Positive Voltage Reference** (*Output*) **-** Positive reference voltage for the internal sampling circuits.
AOUTA AOUTB	8 9	**Analog Outputs** (*Output*) - The full-scale analog line output level is specified in the Analog Characteristics table.
GND	6, 10	**Ground** (*Input*) - Ground reference. See Section 4.10 on page 18 for layout considerations.
VA	11	**Analog, Charge Pump, and Regulator Power** (*Input*) **-** Positive power supply for the analog, inverting charge pump, and regulator for the digital core logic sections.
FLYP FLYN	12 13	**Inverting Charge Pump Cap Positive/Negative Nodes** *(Output)* - Positive and Negative nodes for the inverting charge pump's flying capacitor.
-VFILT	14	**Inverting Charge Pump Filter Connection** *(Output)* - Power supply from the inverting charge pump that provides the negative rail for the output amplifiers.

2. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

GND = 0 V; all voltages with respect to ground.(Note 1)

Parameters		Symbol	Min	Typ	Max	Units
DC power supply	Analog power	VA	4.75	5.0	5.25	V
	Interface power	VL	1.4	1.8, 3.3, 5.0	5.25	V
Ambient operating temperature (power applied)	-CSZ	T_A	-40	-	+85	°C

Notes: 1. Device functional operation is guaranteed within these limits. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

ABSOLUTE MAXIMUM RATINGS

GND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Max	Units
DC power supply	Low voltage analog power	VA	-0.3	6.0	V
	Interface power	VL	-0.3	6.0	V
Input current, any pin except supplies		I_{in}	-	±10	mA
Digital input voltage (Note 2)	Digital interface	V_{IN-L}	-0.3	VL+ 0.4	V
Ambient operating temperature (power applied)		T_A	-55	+125	°C
Storage temperature		T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes: 2. The maximum over/under voltage is limited by the input current except on the power supply pin.

DAC ANALOG CHARACTERISTICS

Test conditions (unless otherwise specified): T_A = 25 °C; VA = 5 V, VL = 3.3 V; GND = 0 V; FILT+, -VFILT, and FLYP/N capacitors as shown in Figure 5 on page 12; input test signal is a 997 Hz sine wave at 0 dBFS; measurement bandwidth 20 Hz to 20 kHz.

Parameter			Symbol	Min	Typ	Max	Unit
Dynamic Performance, Fs = 48, 96, and 192 kHz (Notes 3, 5)							
Dynamic range	24-bit	A-weighted		95	101	-	dB
		unweighted		92	98	-	dB
	16-bit	A-weighted		-	96	-	dB
		unweighted		-	93	-	dB
Total harmonic distortion + noise	24-bit	0 dB	THD+N	-	-86	-80	dB
		-20 dB		-	-78	-72	dB
		-60 dB		-	-38	-32	dB
	16-bit	0 dB		-	-86	-	dB
		-20 dB		-	-73	-	dB
		-60 dB		-	-33	-	dB
Idle channel noise/signal-to-noise ratio		(A-weighted)		-	101	-	dB
Interchannel Isolation		(1 kHz)		-	100	-	dB
Analog Output (Note 4)							
Full scale AOUTx output voltage		(Notes 6, 7)		0.38•VA	0.40•VA	0.42•VA	V_{RMS}
				1.07•VA	1.13•VA	1.19•VA	V_{pp}
Interchannel gain mismatch				-	0.1	-	dB
Output offset				-	±1	±8	mV
Gain drift				-	100	-	ppm/°C
Output impedance			Z_{OUT}	-	100	-	Ω
Load resistance			R_L	3	-	-	kΩ
Load capacitance			C_L	-	-	100	pF

Notes: 3. Measured at the output of the external low-pass filter on AOUTx as shown in Figure 5 on page 12.

4. Measured between the AOUTx and GND pins.

5. One LSB of triangular PDF dither is added to data.

6. Does not include attenuation due to Z_{OUT}. Additional impedance between the AOUTx pin and the load will lower the voltage delivered to the load.

7. V_{PP} is the controlling specification. V_{RMS} specification valid for sine wave signals only.

   Note that for sine wave signals: $V_{RMS} = \frac{V_{pp}}{2\sqrt{2}}$

COMBINED DIGITAL AND ON-CHIP ANALOG FILTER CHARACTERISTICS

The filter characteristics have been normalized to the sample rate (Fs) and can be referenced to the desired sample rate by multiplying the given characteristic by Fs. Reference level (0 dB) is set at 997 Hz. (Note 11)

Parameter		Min	Typ	Max	Unit
Single-Speed Mode - 48 kHz					
Passband (Note 8)	to -0.05 dB corner	$1.796 \cdot 10^{-4}$	-	0.470	Fs
	to -3 dB corner	$1.947 \cdot 10^{-5}$	-	0.500	Fs
Frequency response 20 Hz to 20 kHz		-0.05	-	+0.05	dB
Stopband		0.550	-	-	Fs
Stopband attenuation	(Note 9)	80 dB	-	-	dB
High-pass filter settling time (input signal goes to 95% of its final value)		-	$2.452 \cdot 10^{4}$/Fs	-	s
Total group delay		-	9.4/Fs	-	s
De-emphasis error (Note 10)(Relative to 1 kHz)	Fs = 44.1 kHz	-	-	±0.14	dB
Double-Speed Mode - 96 kHz					
Passband (Note 8)	to -0.05 dB corner	$8.980 \cdot 10^{-5}$	-	0.290	Fs
	to -3 dB corner	$9.736 \cdot 10^{-6}$	-	0.500	Fs
Frequency response 20 Hz to 20 kHz		-0.05	-	+0.05	dB
Stopband		0.583	-	-	Fs
Stopband attenuation	(Note 9)	82 dB	-	-	dB
High-pass filter settling time (input signal goes to 95% of its final value)		-	$4.903 \cdot 10^{4}$/Fs	-	s
Total group delay		-	7.0/Fs	-	s
Quad-Speed Mode - 192 kHz					
Passband (Note 8)	to -0.05 dB corner	$4.490 \cdot 10^{-5}$	-	0.253	Fs
	to -3 dB corner	$4.868 \cdot 10^{-6}$	-	0.486	Fs
Frequency response 20 Hz to 20 kHz		-0.05	-	+0.05	dB
Stopband		0.630	-	-	Fs
Stopband attenuation	(Note 9)	85 dB	-	-	dB
High-pass filter settling time (input signal goes to 95% of its final value)		-	$9.807 \cdot 10^{4}$/Fs	-	s
Total group delay		-	4.9/Fs	-	s

Notes: 8. Response is clock-dependent and will scale with Fs.

9. For Single- and Double-Speed Mode, the Measurement Bandwidth is from stopband to 3 Fs. For Quad-Speed Mode, the Measurement Bandwidth is from stopband to 1.34 Fs.

10. De-emphasis is available only in Single-Speed Mode.

11. Amplitude vs. frequency plots of this data are available in “Combined Digital and On-chip Analog Filter Response Plots” on page 20.

SWITCHING SPECIFICATIONS - SERIAL AUDIO INTERFACE

Parameters	Symbol	Min	Typ	Max	Units
MCLK frequency		7.6	-	55.3	MHz
MCLK duty cycle		35	-	65	%
Input sample rate All MCLK/LRCK ratios combined (Note 12)	Fs	30	-	216	kHz
(SSM) 256x, 384x, 512x, 768x, 1024x		30	-	54	kHz
(DSM) 128x, 192x, 256x, 384x, 512x		84	-	108	kHz
(QSM) 128x, 192x, 256x		170	-	216	kHz
External SCLK Mode					
LRCK duty cycle		45	-	55	%
SCLK pulse width low	t_{sclkl}	20	-	-	ns
SCLK pulse width high	t_{sclkh}	20	-	-	ns
SCLK duty cycle		45	-	55	%
SCLK rising to LRCK edge delay	t_{slrd}	20	-	-	ns
LRCK edge to SCLK rising delay	t_{slrs}	20	-	-	ns
SDIN valid to SCLK rising setup time	t_{sdlrs}	20	-	-	ns
SCLK rising to SDIN hold time	t_{sdh}	20	-	-	ns
Internal SCLK Mode					
LRCK duty cycle		$50\% - \frac{1}{2 \times MCLK}$	-	$50\% + \frac{1}{2 \times MCLK}$	-
SCLK period (Note 13)	t_{sclkw}	$\frac{10^9}{SCLK}$	-	-	ns
MCLK falling to LRCK edge	t_{mclkf}	$\frac{-10^9}{4 \times MCLK}$	-	$\frac{10^9}{4 \times MCLK}$	ns
LRCK edge to SCLK rising	t_{sclkr}	-	(Note 14)	-	ns
SDIN valid to SCLK rising setup time	t_{sdlrs}	$\frac{10^9}{512 \times Fs} + 10$	-	-	ns
SCLK rising to SDIN hold time MCLK / LRCK = 1024, 512, 256, 128	t_{sdh}	$\frac{10^9}{512 \times Fs} + 15$	-	-	ns
MCLK / LRCK = 768, 384, 192		$\frac{10^9}{384 \times Fs} + 15$	-	-	

12. Not all sample rates are supported for all clock ratios. See Section 4.2 “Sample Rate Range/Operational Mode Detect” on page 13 for supported ratios and frequencies. SSM = Single-Speed Mode, DSM = Double-Speed Mode, QSM = Quad-Speed Mode.
13. SCLK period is defined by the SCLK / LRCK ratio. The SCLK/LRCK ratio may be either 32, 48, or 64. See Table 5 on page 14.
14. $t_{sclkr} = \frac{t_{sclkw}}{2} + \frac{10^9}{2 \times MCLK} + t_{mclkf}$

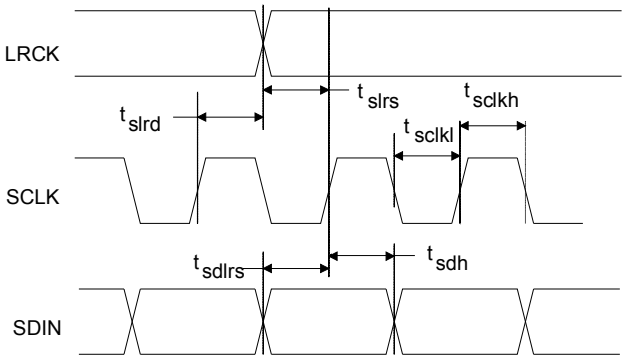
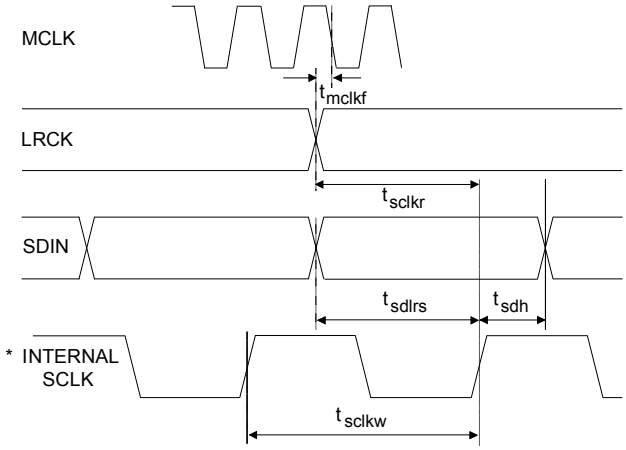
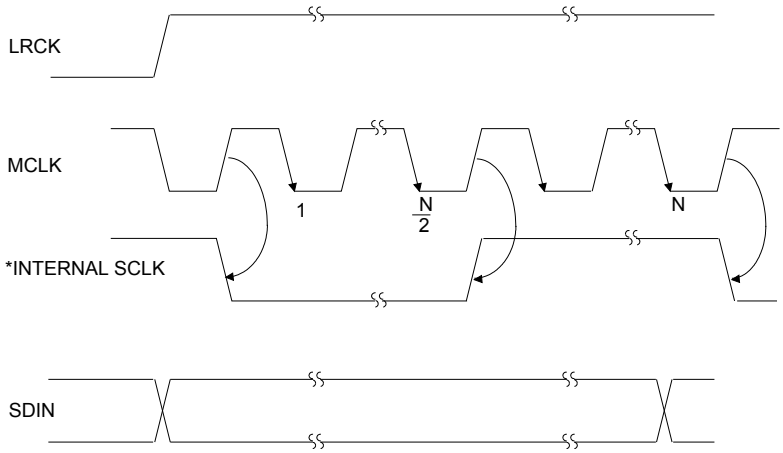


Figure 1. External Serial Clock Mode Input Timing



The SCLK pulses shown are internal to the CS4354.

Figure 2. Internal Serial Clock Mode Input Timing



* The SCLK pulses shown are internal to the CS4354.
N equals MCLK divided by SCLK

Figure 3. Internal Serial Clock Generation

DIGITAL INTERFACE CHARACTERISTICS

Test conditions (unless otherwise specified): GND = 0 V; all voltages with respect to ground.

Parameters		Symbol	Min	Typ	Max	Units
High-level input voltage	1.8 V ≤ VL ≤ 5.0 V	V_{IH}	0.7xVL	-	-	V
Low-level input voltage	1.8 V ≤ VL ≤ 5.0 V	V_{IL}	-	-	0.3xVL	V
Input leakage current		I_{in}	-	-	±10	µA
Input capacitance			-	8	-	pF

INTERNAL POWER-ON RESET THRESHOLD VOLTAGES

Test conditions (unless otherwise specified): GND = 0 V; all voltages with respect to ground.

Parameters	Symbol	Min	Typ	Max	Units
Internal reset asserted at power-on	V_{on1}	-	0.2	-	V
Internal reset released at power-on	V_{on2}	-	3.6	-	V
Internal reset asserted at power-off	V_{off}	-	3.1	-	V

Table 1. Power-On Reset Threshold Voltages

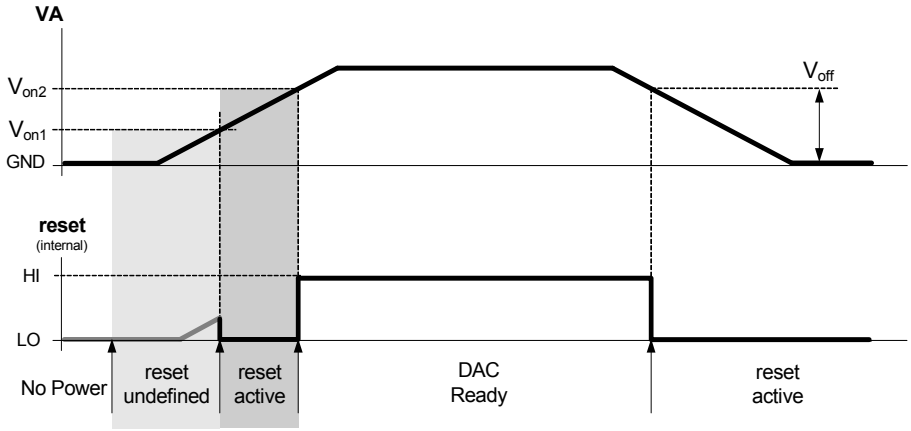


Figure 4. Power-On Reset Threshold Sequence

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise specified): VA = 5 V, VL = 3.3 V; GND = 0 V; SDIN = 0; all voltages with respect to ground.

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies						
Power supply current (Note 15)	Normal operation (Note 16)	I_{VA}	-	10	13	mA
		I_{VL}	-	0.1	0.2	mA
	Power-down (Note 17)	I_{VA}	-	0.5	-	mA
		I_{VL}	-	1	-	µA
Power dissipation (all supplies) (Note 15)	Normal Operation (Note 16)		-	50	65	mW
	Power-Down (Note 17)		-	2.5	-	mW
Power supply rejection ratio (Note 18)	(1 kHz)	PSRR	-	60	-	dB
	(60 Hz)		-	60	-	dB
DC Output Voltages						
Pin voltage	FILT+ to GND		-	3.5	-	V
	FLYP to FLYN		-	4.9	-	V
	GND to -VFILT		-	4.7	-	V

Notes: 15. Power supply current increases with increasing sample rate and increasing MCLK frequency. Typical values are based on Fs = 48 kHz and MCLK = 12.288 MHz. Maximum values are based on highest sample rate and highest MCLK frequency; see "Switching Specifications - Serial Audio Interface" on page 8. Variance between speed modes is small.

16. During normal operation, SDIN = 997 Hz sine wave at 0 dBFS with load resistance R_L = 3 kΩ.

17. Power-down is defined as all clock and data lines held static low. All digital inputs have a weak pull-down (approximately 50 kΩ) which is only present during power on reset. Opposing this pull-down will increase the power-down current.

18. Valid with the recommended capacitor values as shown in the "Typical Connection Diagram" on page 12.

2.1 Digital I/O Pin Characteristics

Input and output levels and associated typical power supply voltage are shown in Table 2. Logic levels should not exceed the corresponding power supply voltage.

Pin Name	Power Supply	I/O	Driver	Receiver
MCLK	VL	Input	-	1.8 V - 5 V
LRCK	VL	Input	-	1.8 V - 5 V
SCLK	VL	Input	-	1.8 V - 5 V
SDIN	VL	Input	-	1.8 V - 5 V

Table 2. Digital I/O Pin Characteristics

3. TYPICAL CONNECTION DIAGRAM

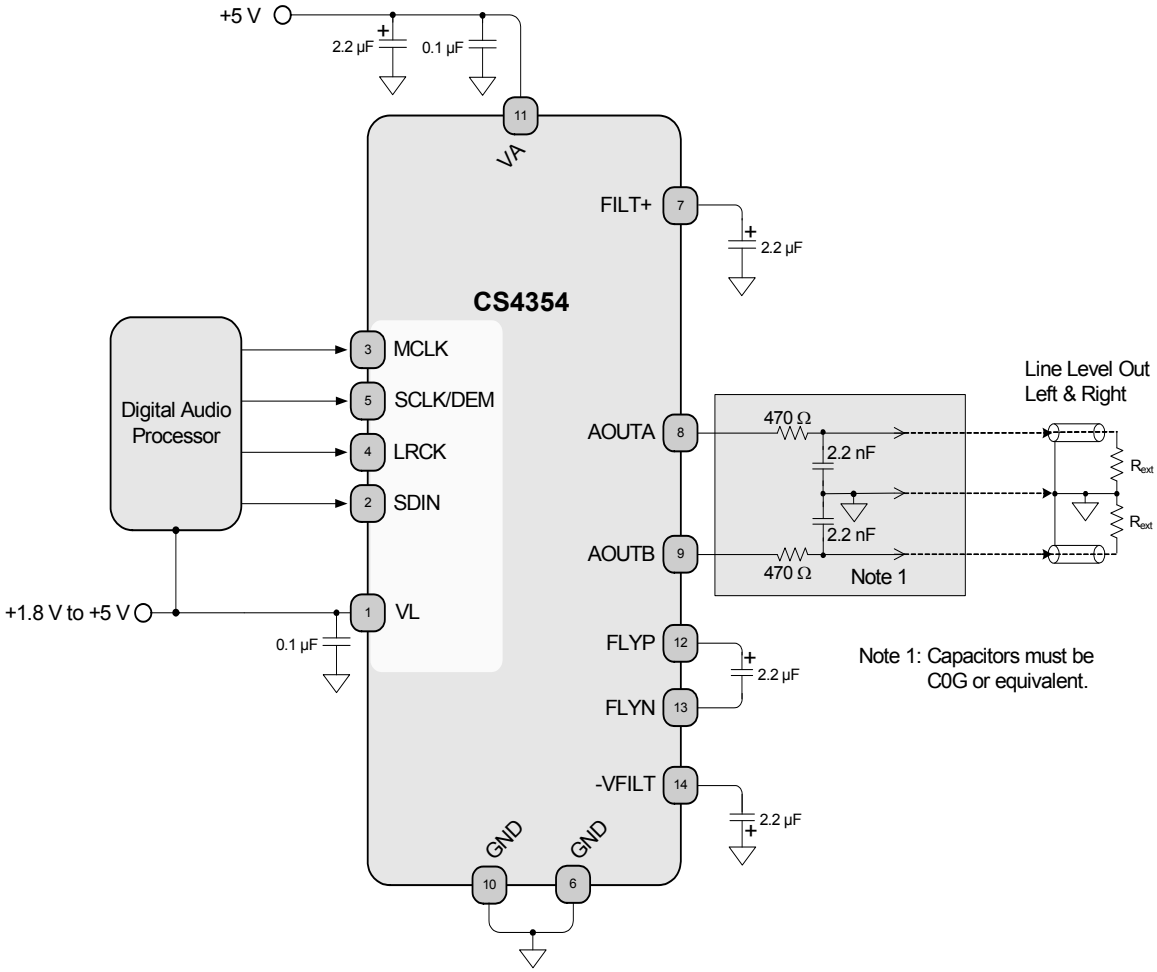


Figure 5. Typical Connection Diagram

4. APPLICATIONS

4.1 Ground-Centered Line Outputs

An on-chip charge pump creates a negative supply which allows the full-scale output swing to be centered around ground. This eliminates the need for large DC-blocking capacitors which create audible pops at power-on and provides improved low frequency response. See the DAC Analog Characteristics table for the complete specifications of the full-scale output voltage. It should be noted that external output impedance between the AOUTx pin and the load will lower the voltage delivered to the load.

4.2 Sample Rate Range/Operational Mode Detect

The CS4354 operates in one of three operational modes. The device will auto-detect the correct mode when the input sample rate (Fs), defined by the LRCK frequency, falls within one of the ranges illustrated in Table 3. Sample rates outside the specified range for each mode are not supported. In addition to a valid LRCK frequency, a valid serial clock (SCLK) and master clock (MCLK) must also be applied to the device for speed mode auto-detection; see Figure 9.

Input Sample Rate (Fs)	Mode
30 kHz - 54 kHz	Single-Speed Mode
84 kHz - 108 kHz	Double-Speed Mode
170 kHz - 216 kHz	Quad-Speed Mode

Table 3. CS4354 Operational Mode Auto-Detect

4.3 System Clocking

The device requires external generation of the master (MCLK), left/right (LRCK) and serial (SCLK) clocks. The left/right clock, defined also as the input sample rate (Fs), must be synchronously derived from the MCLK signal according to specified ratios. The specified ratios of MCLK to LRCK, along with several standard audio sample rates and the required MCLK frequency, are illustrated in Table 4 on page 13.

Refer to Section 4.6 for the required SCLK timing associated with the selected Digital Interface Format and to "Switching Specifications - Serial Audio Interface" on page 8 for the maximum allowed clock frequencies.

LRCK (kHz)	MCLK (MHz)						
	128x	192x	256x	384x	512x	768x	1024x
32	-	-	8.1920	12.2880	16.3840	24.5760	32.7680
44.1	-	-	11.2896	16.9344	22.5792	33.8688	45.1580
48	-	-	12.2880	18.4320	24.5760	36.8640	49.1520
88.2	11.2896	16.9344	22.5792	33.8688	45.1584	-	-
96	12.2880	18.4320	24.5760	36.8640	49.1520	-	-
176.4	22.5792	33.8688	45.1584	-	-	-	-
192	24.5760	36.8640	49.1520	-	-	-	-
Mode	QSM			DSM		SSM	

Table 4. Common MCLK and LRCK Frequencies

4.4 Serial Clock

The serial clock controls the shifting of data into the input data buffers. The CS4354 supports both external and internal serial clock generation modes. Refer to Figure 6 for a diagram of the I²S data format.

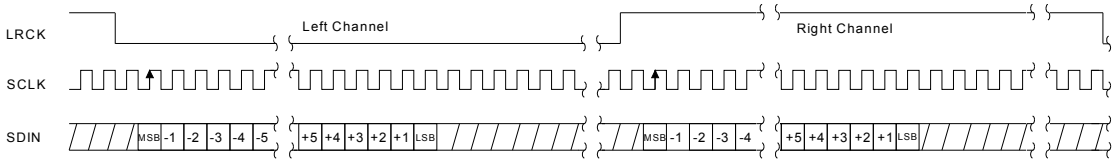


Figure 6. CS4354 Data Format (I²S)

In order to support selectable de-emphasis without a dedicated pin, pin 5 (SCLK/DEM) functions both as a serial clock input and a de-emphasis select. In typical applications where de-emphasis is not required, the SCLK/DEM pin is the input for an external serial clock - this is known as the External Serial Clock Mode. To enable de-emphasis selection, the Internal Serial Clock Mode has to be used. Sections 4.4.1 and 4.4.2 describe this feature in detail.

4.4.1 External Serial Clock Mode

The CS4354 will enter the External Serial Clock Mode when 16 low to high transitions are detected on the SCLK/DEM pin during any phase of the LRCK period. When this mode is enabled, the Internal Serial Clock Mode and de-emphasis filter are disabled (see Figure 9 for flow diagram).

In the External Serial Clock Mode, the CS4354 will support up to 24-bit I²S data, with data valid on the rising edge of SCLK.

4.4.2 Internal Serial Clock Mode

The CS4354 will switch to Internal Serial Clock Mode if no low to high transitions are detected on the SCLK/DEM pin for 2 consecutive frames of LRCK (see Figure 9 for flow diagram). In the Internal Serial Clock Mode, the serial clock is internally derived and synchronous with MCLK and LRCK. The SCLK/LRCK frequency ratio is either 32, 48, or 64 depending on the speed mode and MCLK frequency. Operation in this mode is identical to operation with an external serial clock synchronized with LRCK. This mode allows access to the digital de-emphasis function. Refer to Table 5 for details (all frequencies listed as multiples of LRCK frequency).

Speed Mode	MCLK =	128x	192x	256x	384x	512x	768x	1024x
SSM		-	-	64x	48x	64x	64x	64x
DSM		-	48x	-	-	-	-	-
QSM		-	32x	32x	-	-	-	-

Table 5. Internal SCLK Frequencies

4.4.2.1 De-Emphasis Control

The device includes on-chip digital de-emphasis. Figure 7 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve scales with changes in the sample rate, Fs. The de-emphasis error will increase for sample rates other than 44.1 kHz.

When the SCLK/DEM pin is connected to VL (internal SCLK mode), the 44.1 kHz de-emphasis filter is activated. When the SCLK/DEM pin is connected to GND, the de-emphasis filter is disabled. For more information see “Internal Serial Clock Mode” on page 14.

De-emphasis selection is disabled in the external SCLK mode.

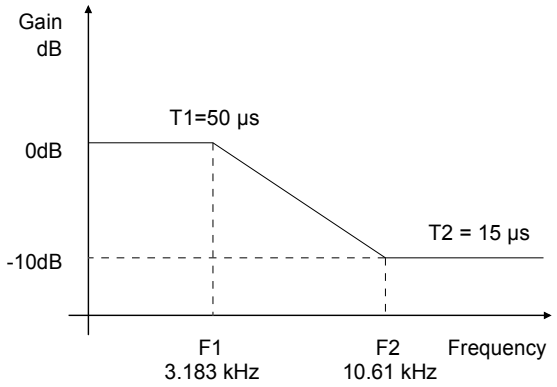


Figure 7. De-Emphasis Curve, Fs = 44.1 kHz

Note: De-emphasis is only available in Single-Speed Mode.

4.5 Internal High-Pass Filter

The CS4354 includes an internal digital high-pass filter. This filter prevents a constant digital offset from creating a DC voltage on the analog output pins. The filter's corner frequency is well below the audio band; see "Combined Digital and On-Chip Analog Filter Characteristics" on page 7 for filter specifications.

4.6 Digital Interface Format

The device accepts audio samples in the industry standard I²S format only.

For an illustration of the required relationship between the LRCK, SCLK and SDIN, see Figure 6 on page 14. SDIN is valid on the rising edge of SCLK. For more information about serial audio formats, refer to Cirrus Logic Application Note AN282: *The 2-Channel Serial Audio Interface: A Tutorial*, available at http://www.cirrus.com.

4.7 Internal Power-On Reset

The CS4354 features an internal power-on reset (POR) circuit. This circuit monitors the VA supply and automatically asserts or releases an internal reset of the DAC's digital circuitry when the supply reaches defined thresholds (see "Internal Power-On Reset Threshold Voltages" on page 10). No external clocks are required for the POR circuit to function.

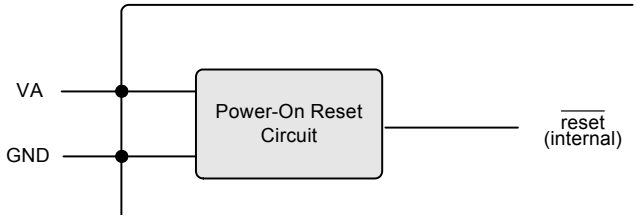


Figure 8. Internal Power-On Reset Circuit

When power is first applied, the POR circuit monitors the VA supply voltage to determine when it reaches a defined threshold, V_{on1}. At this time, the POR circuit asserts the internal reset low, resetting all of the digital circuitry. Once the VA supply reaches the secondary threshold, V_{on2}, the POR circuit releases the internal reset.

When power is removed and the VA voltage reaches a defined threshold, V_{off}, the POR circuit asserts the internal reset low, resetting all of the digital circuitry.

Note: For correct operation of the internal POR circuit, the voltage on VL must rise before or simultaneously with VA.

4.8 Initialization

When power is first applied, the DAC enters a reset (low power) state at the beginning of the initialization sequence. In this state, the AOUTx pins are weakly pulled to ground and FILT+ is connected to GND.

The device will remain in the reset state until V_{ON2} is reached. Once V_{ON2} is reached, the internal digital circuitry is reset and the DAC enters a power-down state until MCLK is applied.

Once MCLK is valid, the device enters an initialization state in which the charge pump powers up and charges the capacitors for the negative voltage supply.

Once LRCK is valid, the number of MCLK cycles is counted relative to the LRCK period to determine the MCLK/LRCK frequency ratio. Next, the device enters the power-up state in which the interpolation filters and delta-sigma modulators are turned on, the internal voltage reference, FILT+, powers up to normal operation, the analog output pull-down resistors are removed, and power is applied to the output amplifiers.

If a valid SCLK is applied, the device will clock in data according to the applied SCLK. If no SCLK is present, the device will clock in data using the derived internal SCLK (see Figure 3 on page 9) and will apply the de-emphasis filter according to Section 4.4.2.1 on page 14.

After this power-up state sequence is complete, normal operation begins and analog output is generated.

If valid MCLK, LRCK, and SCLK are applied to the DAC before V_{ON2} is reached, the total time from V_{ON2} to the analog audio output from AOUTx is less than 50 ms.

See Figure 9 for a diagram of the device's states and transition conditions.

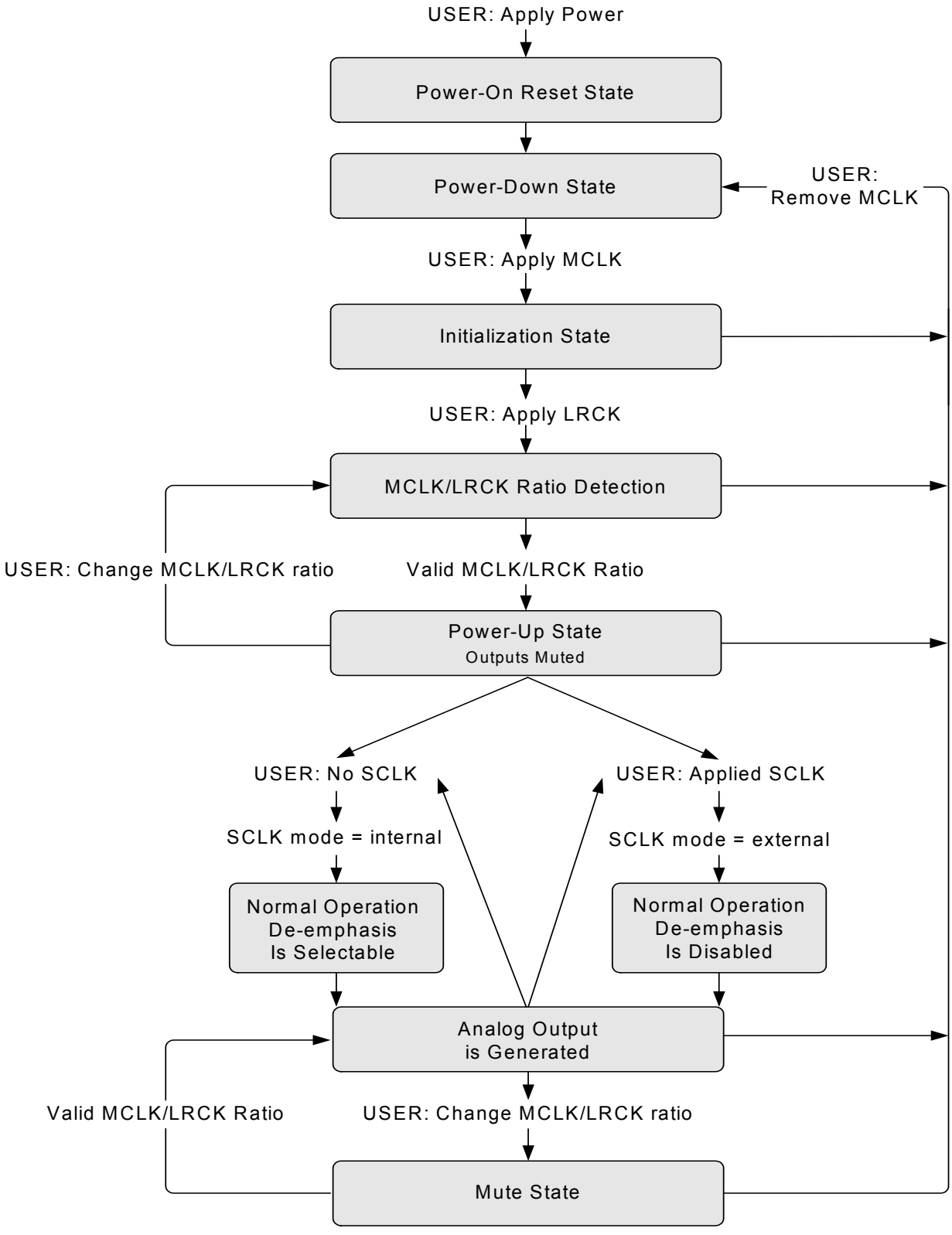


Figure 9. Initialization and Power-Down Sequence Diagram

4.9 Recommended Operational Sequences

The following sequences are recommended for minimal pops and clicks when transitioning between different states of operation.

4.9.1 Power-Up

1. Turn on power supplies.
2. Wait for power supply voltages to stabilize.
3. Apply the serial port clocks and data.

   Provide the correct MCLK, LRCK, and SCLK (only in External Serial Clock Mode); please refer to Section 4.4 on page 14 for common clock frequencies in the External Serial Clock Mode, and supported modes in the Internal Serial Clock Mode. The sequence will complete and audio will be output from the AOUTx pins within 50 ms after valid clocks are applied.

4.9.2 Power-Down

1. Stop LRCK.
2. Wait 5 ms.
3. Stop MCLK without applying any glitched pulses to the MCLK pin.

   A glitched pulse is any pulse that is shorter than the period defined by the minimum/maximum MCLK signal duty cycle specification and the nominal frequency of the input MCLK signal. A transient may occur on the analog outputs if the MCLK signal duty cycle specification is violated when the MCLK signal is removed during normal operation; see “Switching Specifications - Serial Audio Interface” on page 8.
4. Turn off power supplies.

4.9.3 Sample Rate Change

1. Stop LRCK.
2. Wait 5 ms.
3. Stop MCLK without applying any glitched pulses to the MCLK pin.

   A glitched pulse is any pulse that is shorter than the period defined by the minimum/maximum MCLK signal duty cycle specification and the nominal frequency of the input MCLK signal. A transient may occur on the analog outputs if the MCLK signal duty cycle specification is violated when the MCLK signal is removed during normal operation; see “Switching Specifications - Serial Audio Interface” on page 8.
4. Wait 2 ms.

   This wait time is dictated by the discharge time of the recommended 2.2 µF FILT+ capacitor (see “Typical Connection Diagram” on page 12). Higher capacitance values will require longer wait times.
5. Apply the serial port clocks and data.

   Provide the correct MCLK, LRCK, and SCLK (only in External Serial Clock Mode); please refer to Section 4.4 on page 14 for common clock frequencies in the External Serial Clock Mode, and supported modes in the Internal Serial Clock Mode. The sequence will complete, and audio will be output from the AOUTx pins within 50 ms after valid clocks are applied.

4.10 Grounding and Power Supply Arrangements

As with any high-resolution converter, the CS4354 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. The “Typical Connection Diagram” on page 12

shows the recommended power arrangements with VA and VL connected to clean supplies. It is strongly recommended that a single ground plane be used with the GND pins connected to the common plane; this is important because both pin 6 and pin 10 provide analog ground reference to the CS4354. Should it be necessary to split the ground planes, the CS4354 should be placed entirely in the analog plane. In this configuration, it is critical that the digital and analog ground planes be tied together with a low-impedance connection, ideally a strip of copper on the printed circuit board, at a single point near the CS4354.

All signals, especially clocks, should be kept away from the FILT+ pin in order to avoid unwanted coupling into the DAC.

4.10.1 Capacitor Placement

Decoupling capacitors should be placed as close to the device as possible, with the low-value ceramic capacitor being the closest. To further minimize impedance, these capacitors should be located on the same PCB layer as the device. See DC Electrical Characteristics for the voltage present across pin pairs. This is useful for choosing appropriate capacitor voltage ratings and orientation if electrolytic capacitors are used.

The CDB4354 evaluation board demonstrates the optimum layout and power supply arrangements.

5. COMBINED DIGITAL AND ON-CHIP ANALOG FILTER RESPONSE PLOTS

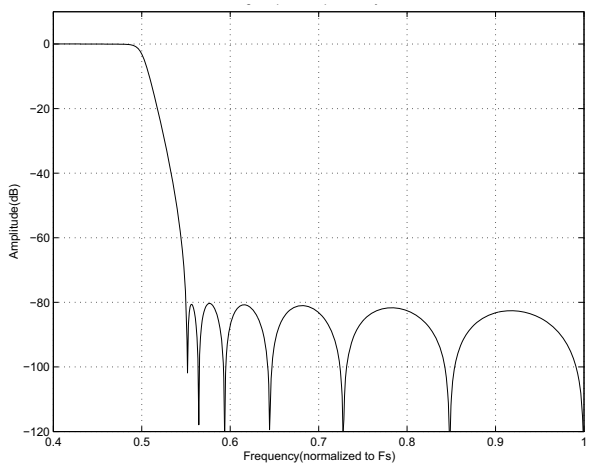


Figure 10. Single-Speed Stopband Rejection

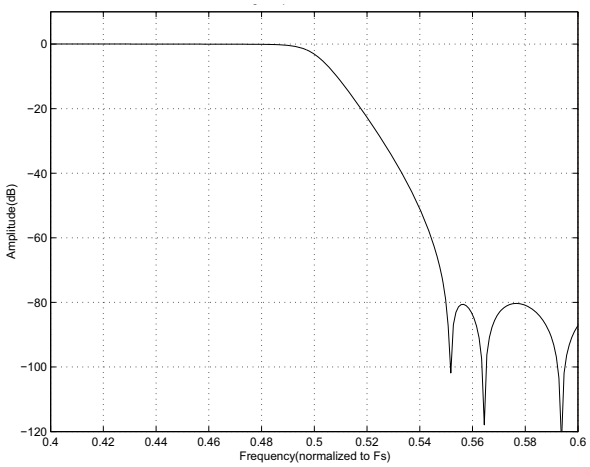


Figure 11. Single-Speed Transition Band

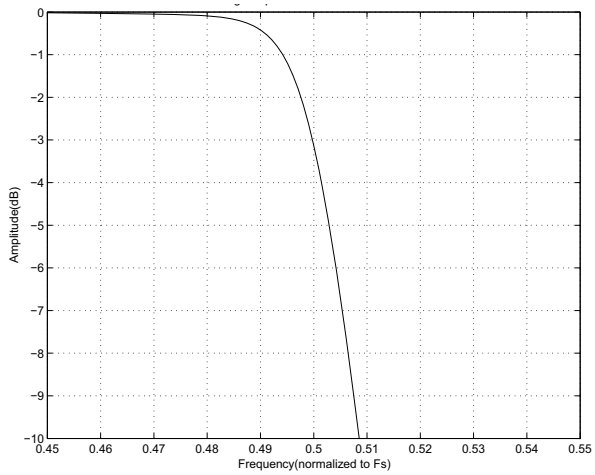


Figure 12. Single-Speed Transition Band (detail)

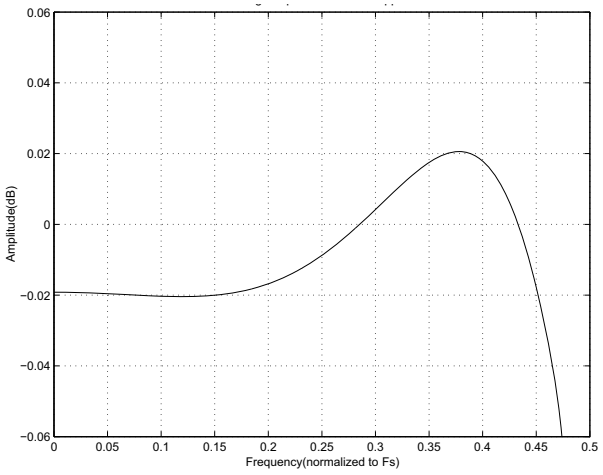


Figure 13. Single-Speed Passband Ripple

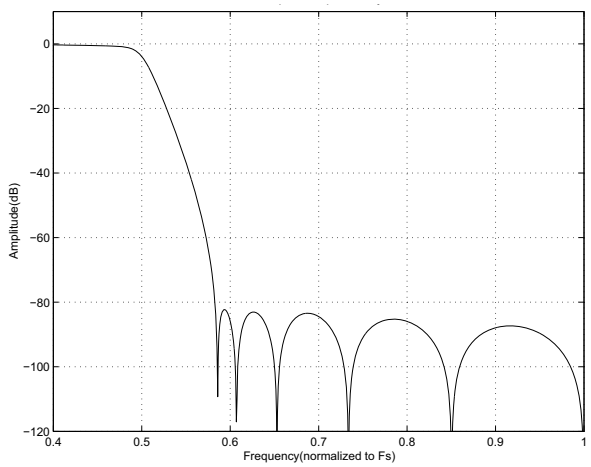


Figure 14. Double-Speed Stopband Rejection

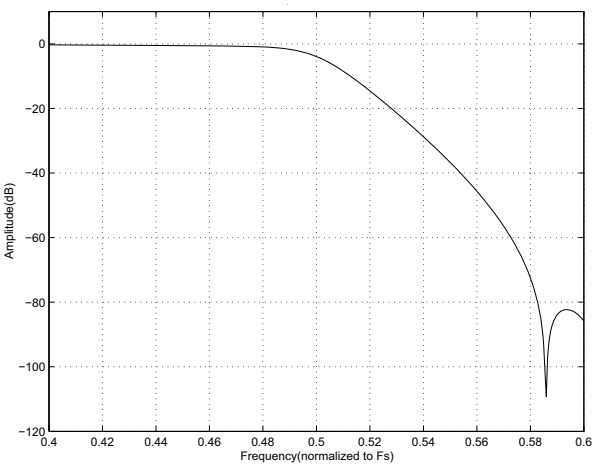


Figure 15. Double-Speed Transition Band

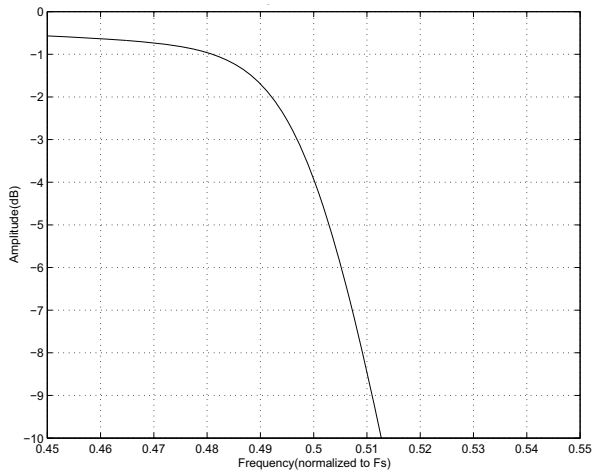


Figure 16. Double-Speed Transition Band (detail)

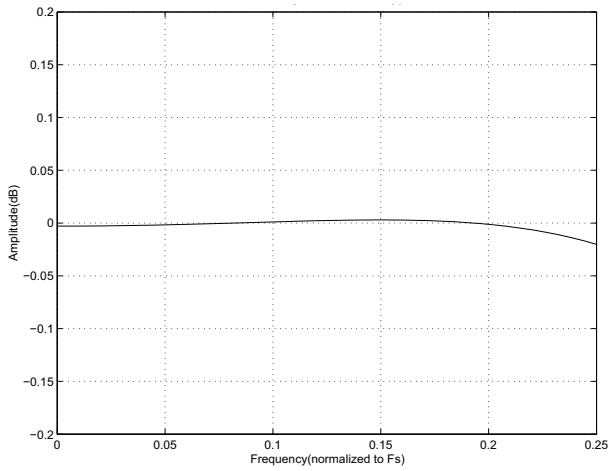


Figure 17. Double-Speed Passband Ripple

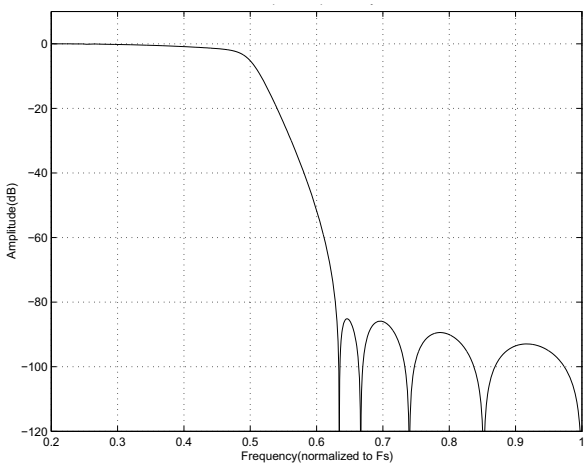


Figure 18. Quad-Speed Stopband Rejection

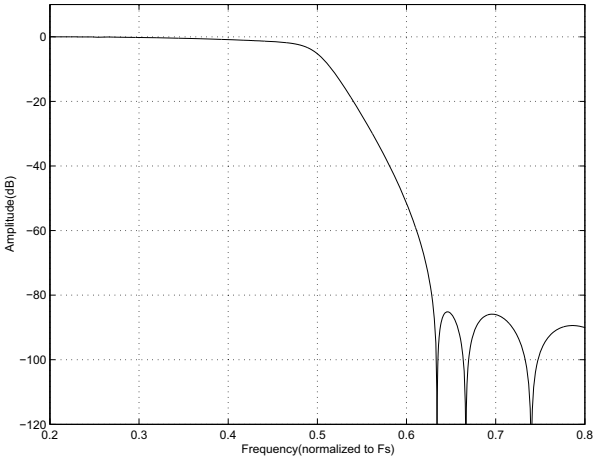


Figure 19. Quad-Speed Transition Band

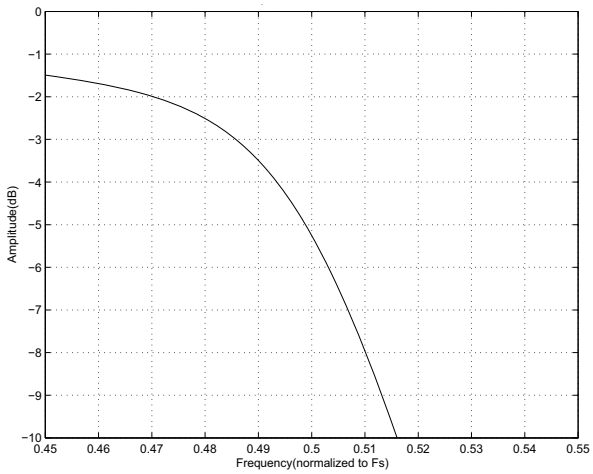


Figure 20. Quad-Speed Transition Band (detail)

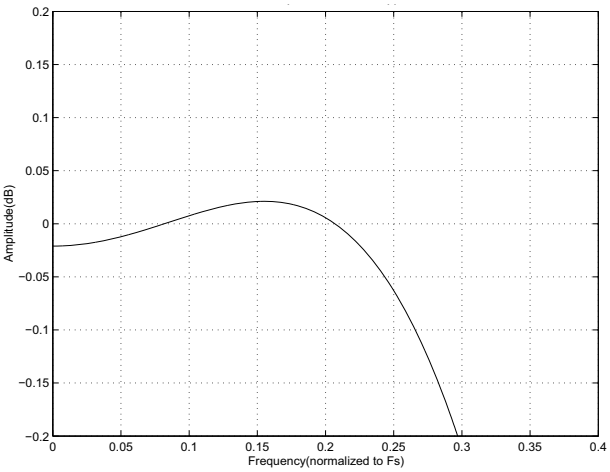


Figure 21. Quad-Speed Passband Ripple

6. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full-scale RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

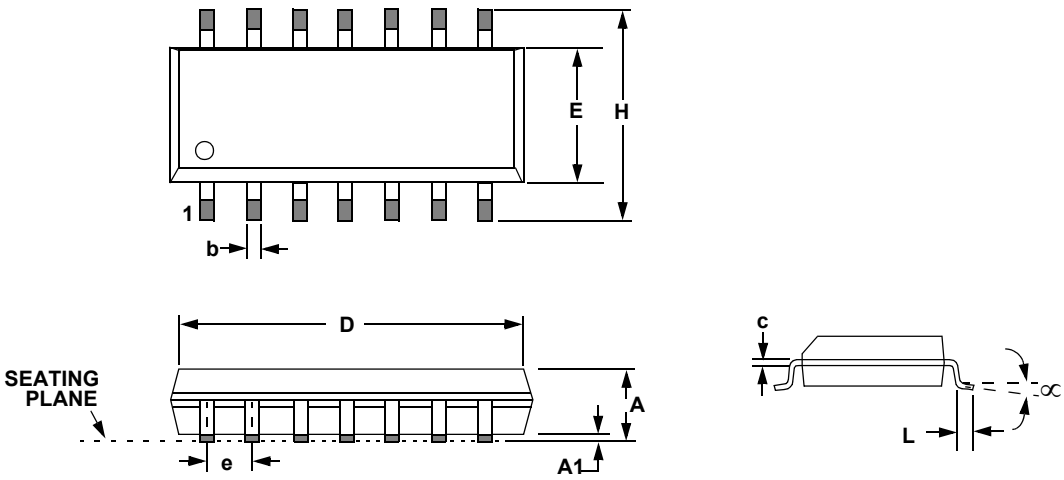
Total Harmonic Distortion + Noise (THD+N)

The ratio of the RMS value of the signal to the RMS sum of all other spectral components over the specified bandwidth (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels.

7. PACKAGE INFORMATION

7.1 Dimensions

14L SOIC (150 MIL BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.0600	-	0.0680	1.524	-	1.727
A1	0.0040	-	0.0098	0.102	-	0.249
b	0.0138	-	0.0200	0.351	-	0.508
C	0.0075	-	0.0098	0.190	-	0.250
D	0.3380	-	0.3440	8.585	-	8.738
E	0.1520	-	0.1574	3.861	-	3.998
e	-	0.050 BSC	-	-	1.270 BSC	-
H	0.2300	-	0.2440	5.842	-	6.198
L	0.0160	-	0.0350	0.406	-	0.889
∝	0°	-	8°	0°	-	8°

JEDEC #: MS-012

Controling Dimension is Millimeters

7.2 Thermal Characteristics

Parameter		Symbol	Min	Typ	Max	Units
Junction-to-Ambient Thermal Impedance	2-layer board	θ_{JA}	-	110	-	°C/Watt
	4-layer board		-	86	-	

8. ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS4354	5 V Stereo Audio DAC with 2 V_{RMS} Line Output	14-pin SOIC	YES	Commercial	-40° to +85° C	Rail	CS4354-CSZ
						Tape & Reel	CS4354-CSZR
CDB4354	CS4354 Evaluation Board		-	-	-	-	CDB4354

9. REVISION HISTORY

Release	Changes
F1 JUNE 2011	Changed 1.8 V < VL ≤ 5.0 V to 1.8 V ≤ VL ≤ 5.0 V for both high- and low-level input voltage parameters in Digital Interface Characteristics section on page 10.
F2 SEP 2011	Updated MCLK duty cycle specification to 35%/65% from 45%/55% in Switching Specifications - Serial Audio Interface section on page 8.
F3 OCT 2014	Updated “A” dimensions in Section 7.1. (Data sheet change only; no change has been made to the physical device.)

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.