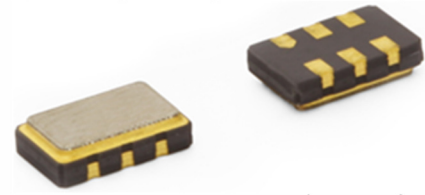


Model CA50P/L

Automotive Grade LVPECL or LVDS Clock



Part Dimensions:
5.0 x 3.2 x 1.3mm • 60.7734mg

Features

- AEC-Q200 Compliant
- Very Low Phase Jitter Performance, 500fs Maximum
- Ceramic Surface Mount Package
- Operating Temperature Ranges to -40°C to +125°C
- Fundamental and 3rd Overtone Crystal Designs
- Frequency Range 13.5 – 160MHz *
- +2.5V or +3.3V Operation [+1.8V available, LVDS only]
- Output Enable Standard
- Tape and Reel Packaging, EIA-481

Standard Frequencies

* See Page 9 for common frequencies.
Check with factory for availability of frequencies not listed.

Applications

- Automotive Electronics
- Mobile Multimedia/Infotainment
- IoT and IIoT
- Ethernet/GbE/SyncE
- Audio/Video Systems
- Wireless Communication
- SerDes
- Medical Electronics
- Commercial Military & Aerospace

Description

CTS Model CA50P/L is a low cost, small size, Clock Oscillator [XO] developed for use in automotive electronics operating over extended temperature ranges. CA50P/L has optional LVPECL or LVDS compatible outputs, offers excellent stability and low jitter/phase noise performance.

Ordering Information

Model		Output Type	Frequency Code [MHz]	Frequency Stability	Temperature Range	Supply Voltage	Packaging
CA	50	P	XXX or XXXX	3	G	L	T
Code Package Size		Code Frequency		Code Temp. Range		Code Packing	
50	5.0x3.2mm	Product Frequency Code ¹		I -40°C to +85°C		T 1k pcs./reel	
Code Output		Code Stability		Code Stability		Code Voltage	
P	LVPECL	5 ±25ppm		3 ±50ppm		M +1.8Vdc	
L	LVDS	4 ±30ppm		2 ±100ppm		N +2.5Vdc	
						L +3.3Vdc	

Notes:

- 1] Refer to document 016-1454-0, Frequency Code Tables. 3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.
- 2] Available with stability codes 4, 3, 2 and 7.
- 3] Available with stability codes 3, 2 and 7.

**Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.**

This product is specified for use only in standard commercial applications. Supplier disclaims all express and implied warranties and liability in connection with any use of this product in any non-commercial applications or in any application that may expose the product to conditions that are outside of the tolerances provided in its specification.



Electrical Specifications

Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.5	-	5.0	V
Supply Voltage [Note 1]	V_{CC}	$\pm 5\%$	1.710 2.375 3.135	1.8 2.5 3.3	1.890 2.625 3.465	V
Supply Current						
LVPECL	I_{CC}	$V_{CC} = +2.5V$ or $+3.3V$ @ Maximum Load	-	55	80	mA
LVDS			-	45	60	
LVDS		$V_{CC} = +1.8$ @ Maximum Load	-	7	20	
Operating Temperature	T_A	-	-40 -40	+25	+85 +105 +125	$^{\circ}C$
Storage Temperature	T_{STG}	-	-55	-	+125	$^{\circ}C$

1.] LVDS output only for +1.8V option.

Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range						
LVPECL	f_0	$V_{CC} = +2.5V$ or $+3.3V$		13.5 - 160		MHz
LVDS				13.5 - 160		
LVDS			$V_{CC} = +1.8V$	13.5 - 160		
Frequency Stability [Note 2]	$\Delta f/f_0$	-		25, 30, 50, 100 or 150		\pm ppm
Aging	$\Delta f/f_{25}$	First Year @ $+25^{\circ}C$, nominal V_{CC}	-3	-	3	ppm

2.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		LVPECL		-
Output Load	R_L	Terminated to $V_{CC} - 2.0V$	-	50	-	Ohms
Output Voltage Levels	V_{OH} V_{OL}	PECL Load, Temperature Range	$V_{CC} - 1.025$ $V_{CC} - 1.810$	-	$V_{CC} - 0.880$ $V_{CC} - 1.620$	V
Output Duty Cycle	SYM	@ $V_{CC} - 1.3V$	45	-	55	%
Rise and Fall Time	T_R, T_F	@ 20%/80% Levels, $R_L = 50$ Ohms	-	0.3	0.7	ns
Output Type	-	-		LVDS		-
Output Load	R_L	Between Outputs	-	100	-	Ohms
Output Voltage Levels	V_{OH} V_{OL}	LVDS Load	- 0.90	1.43 1.10	1.60 -	V
Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
Differential Output Voltage	V_{OD}	$R_L = 100$ Ohms	247	330	454	mV
Offset Voltage	V_{OS}	LVDS Load	1.125	1.25	1.375	V
Rise and Fall Time	T_R, T_F	@ 20%/80% Levels, $R_L = 100$ Ohms	-	0.4	0.7	ns

Electrical Specifications

Output Parameters

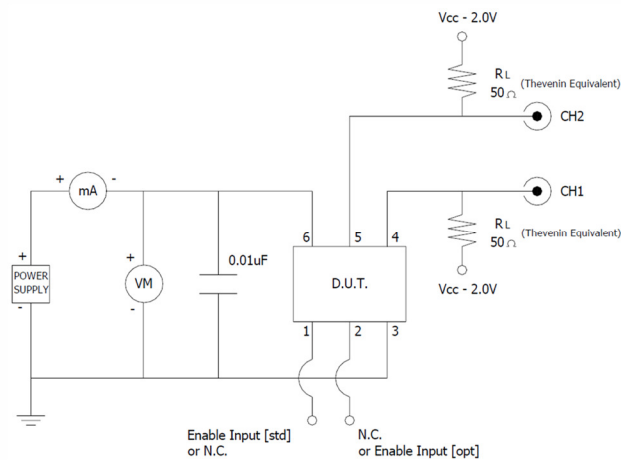
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Start Up Time	T_S	Application of V_{CC}	-	2	10	ms
Enable Function		Standby [oscillator stopped]				
Enable Input Voltage	V_{IH}	Pin 1 or 2 Logic '1', Output Enabled	$0.7V_{CC}$	-	-	V
Disable Input Voltage	V_{IL}	Pin 1 or 2 Logic '0', Output Disabled	-	-	$0.3V_{CC}$	V
Disable Time	T_{PLZ}	Pin 1 or 2 Logic '0', Output Disabled	-	-	200	ns
Standby Current	I_{ST}	Pin 1 Logic '0', Output Disabled	-	-	15	μA
Enable Time	T_{PLZ}	Pin 1 or 2 Logic '1', Output Enabled	-	-	10	ms
Phase Jitter, RMS	t_{jrms}	40MHz - 160MHz, Bandwidth 12kHz to 20MHz	-	300	500	fs
		10MHz - 39.999MHz, Bandwidth 12kHz to 5MHz	-	500	<1	ps

Enable Truth Table

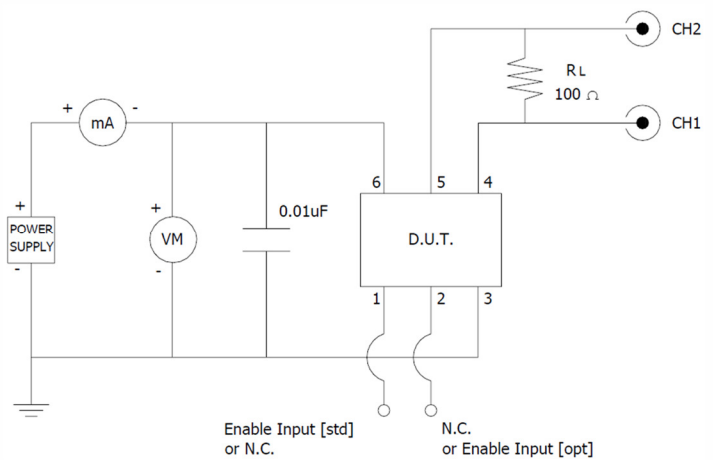
Pin 1	Pin 4 & Pin 5
Logic '1'	Output Enabled
Open	Output Enabled
Logic '0'	Output Disabled, High Impedance

Test Circuit

LVPECL

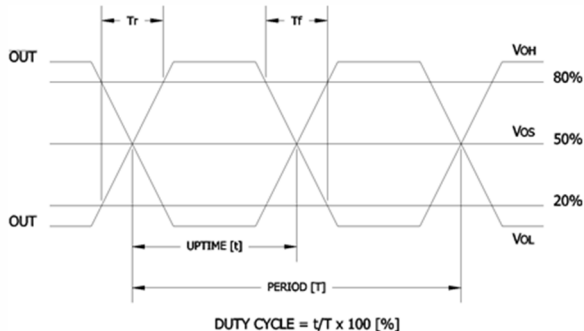


LVDS



Output Waveform

LVPECL or LVDS



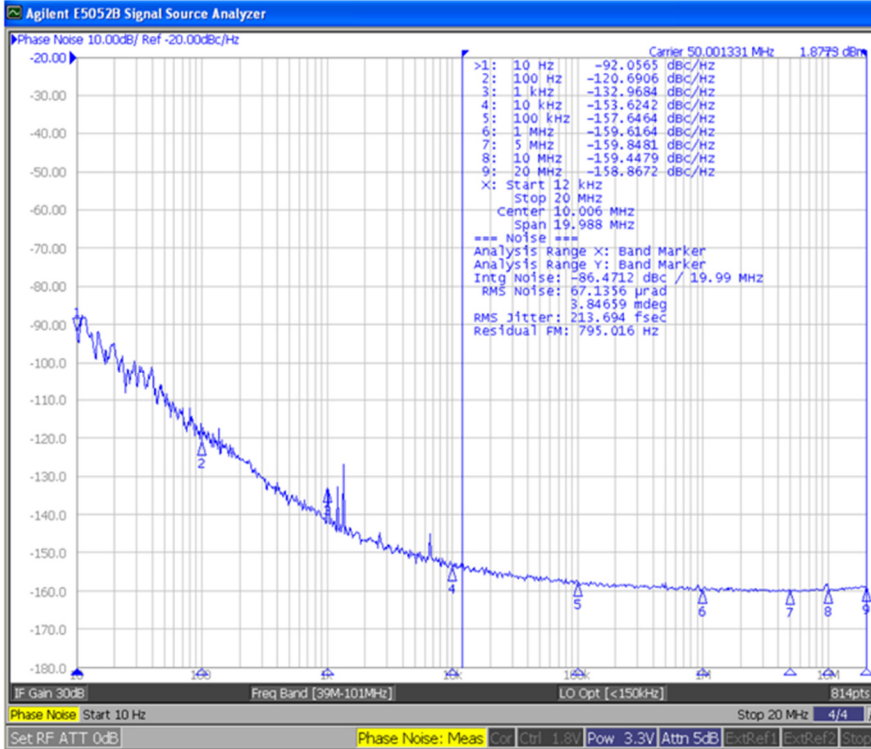


Electrical Specifications

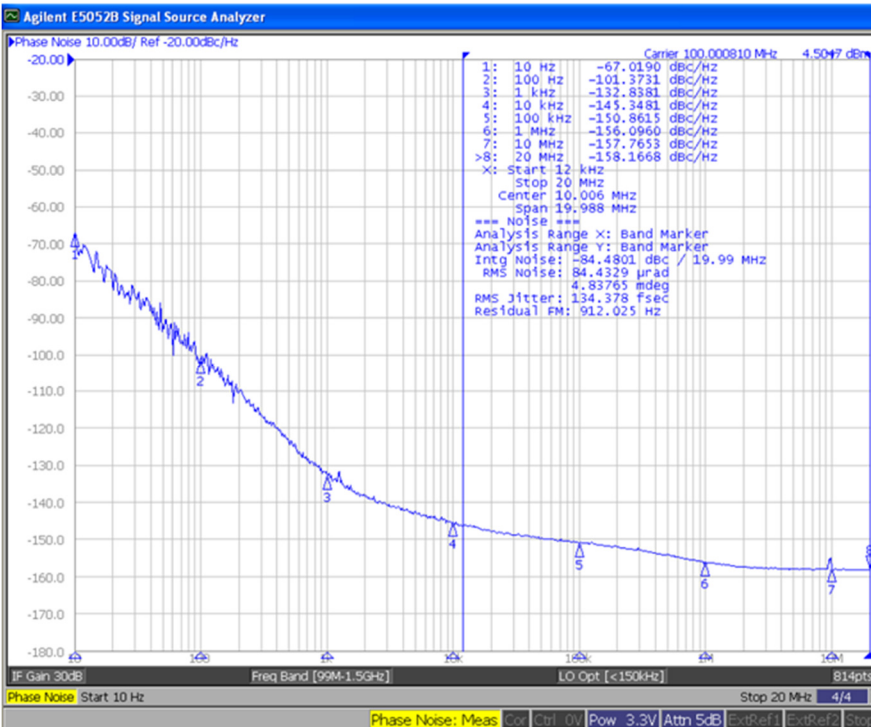
Performance Data

Phase Noise [typical]

50MHz, LVPECL, $V_{CC} = +3.3V$, $T_A = +25^\circ C$



100MHz, LVPECL, $V_{CC} = +3.3V$, $T_A = +25^\circ C$

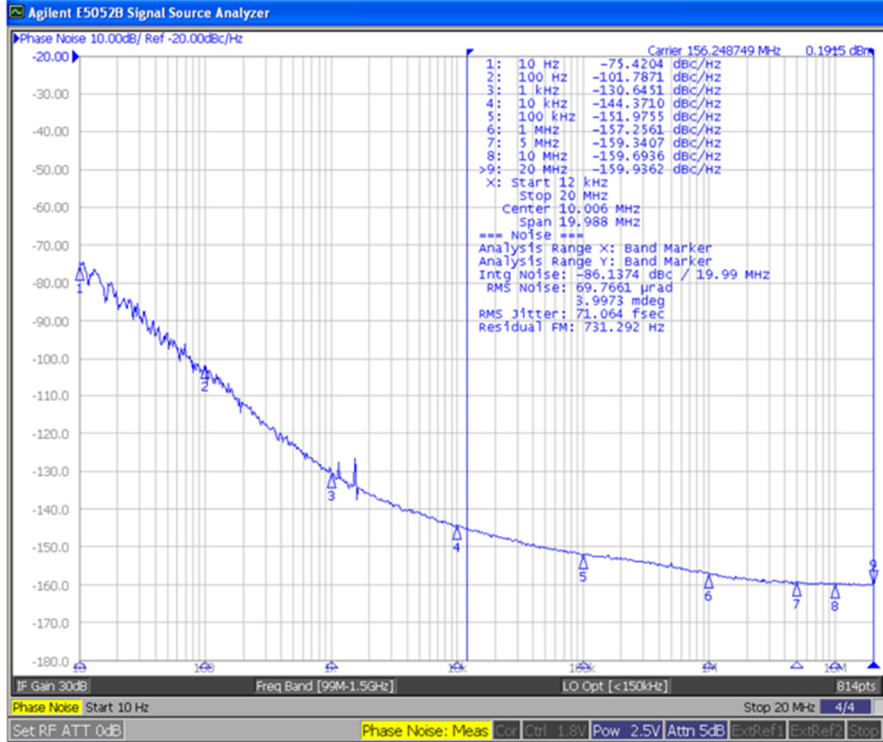


Electrical Specifications

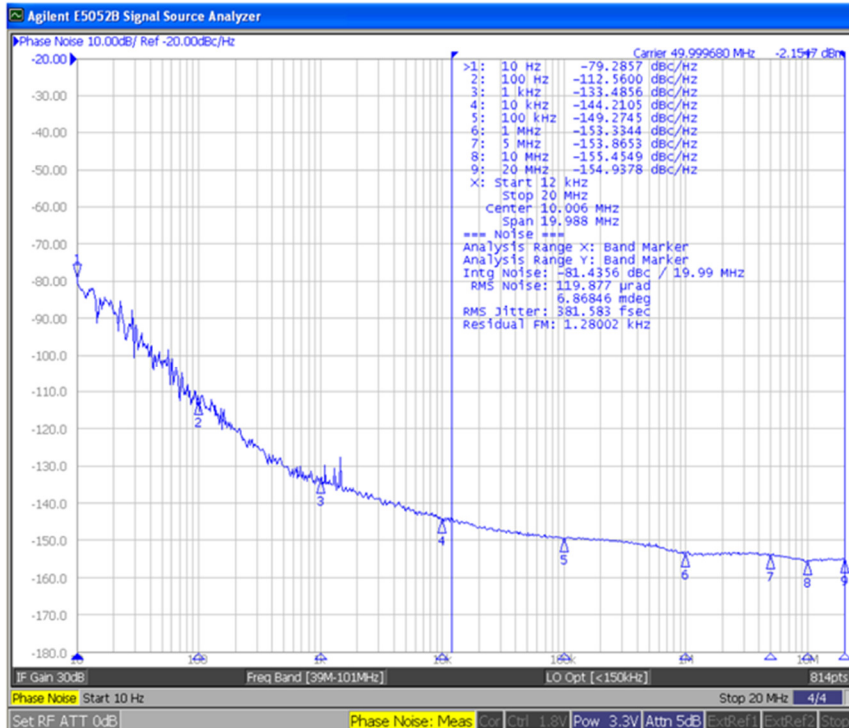
Performance Data

Phase Noise [typical]

156.25MHz, LVPECL, $V_{CC} = +2.5V$, $T_A = +25^\circ C$



50MHz, LVDS, $V_{CC} = +3.3V$, $T_A = +25^\circ C$



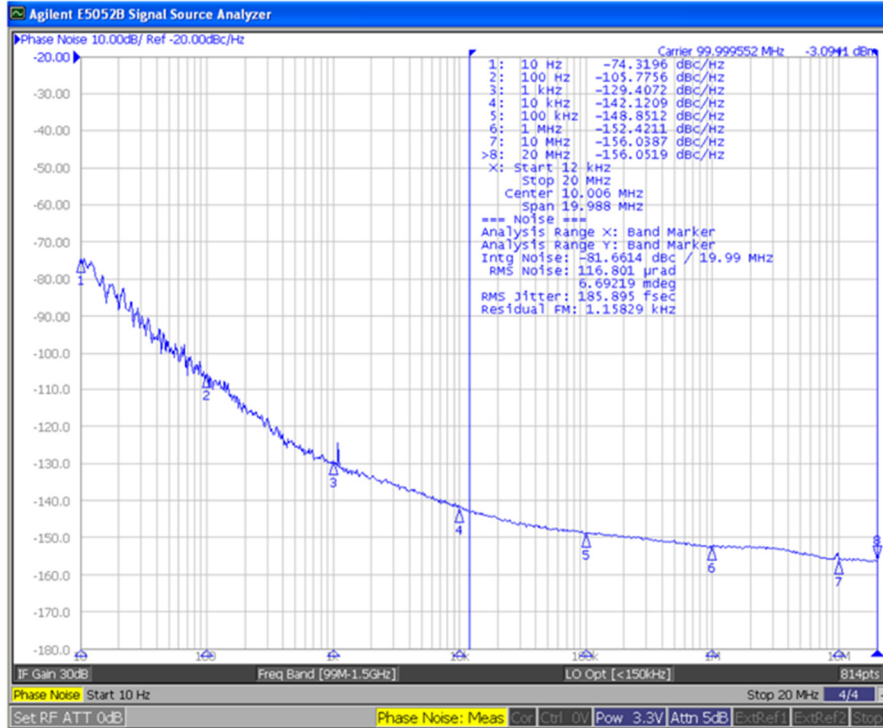


Electrical Specifications

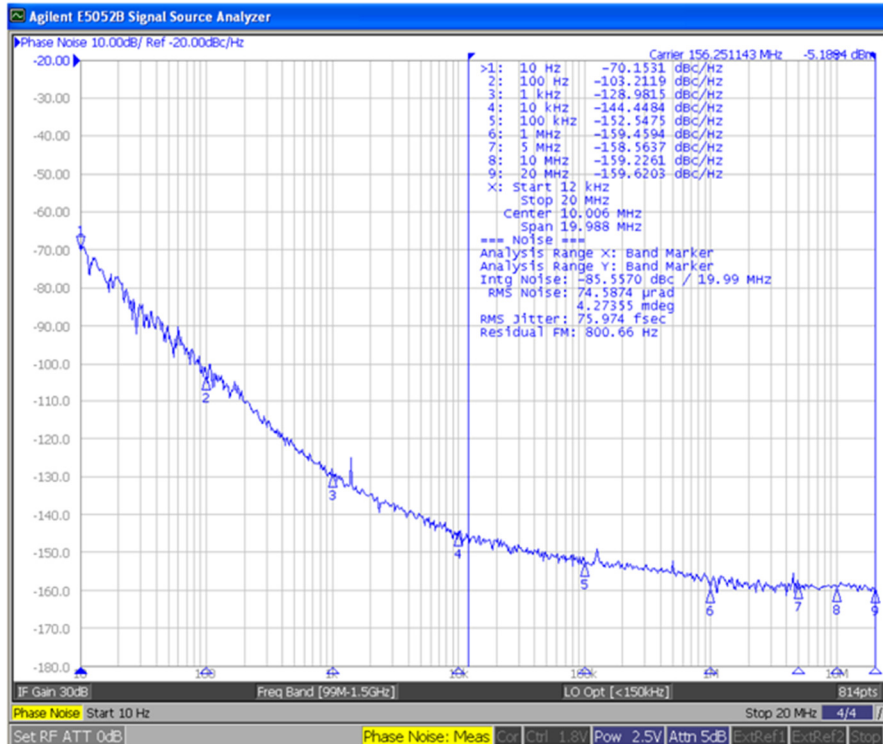
Performance Data

Phase Noise [typical]

100MHz, LVDS, $V_{CC} = +3.3V$, $T_A = +25^\circ C$

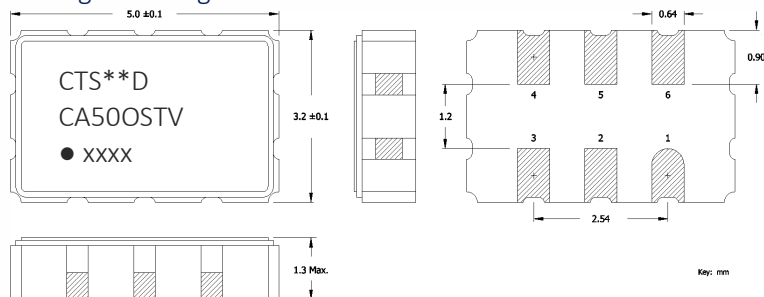


156.25MHz, LVDS, $V_{CC} = +2.5V$, $T_A = +25^\circ C$



Mechanical Specifications

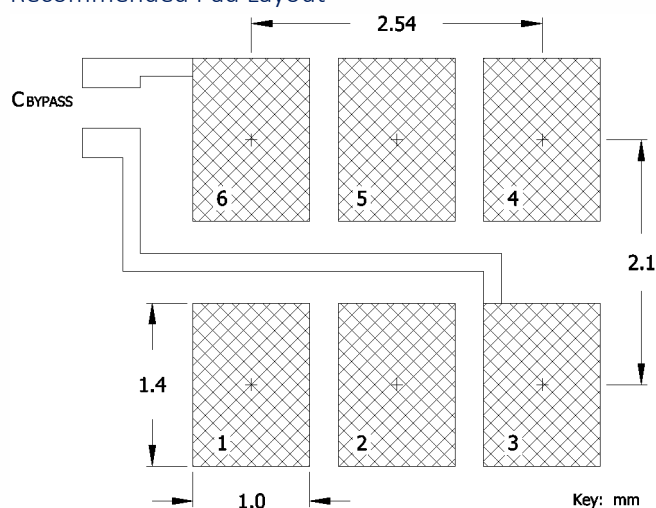
Package Drawing



Marking Information

- ** - Manufacturing Site Code.
- D - Date Code. See Table I for codes.
- O - Output Type; P or E = LVPECL, L or V = LVDS.
- ST - Frequency Stability/Temperature Code. [Refer to Ordering Information]
- V - Voltage Code; 3 = 3.3V, 2 = 2.5V.
- xxxx - Frequency Code.
3-digits, frequencies below 100MHz
4-digits, frequencies 100MHz or greater
[See document 016-1454-0, Frequency Code Tables.]

Recommended Pad Layout



Notes

- Termination pads (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
- MSL = 1.

Pin Assignments

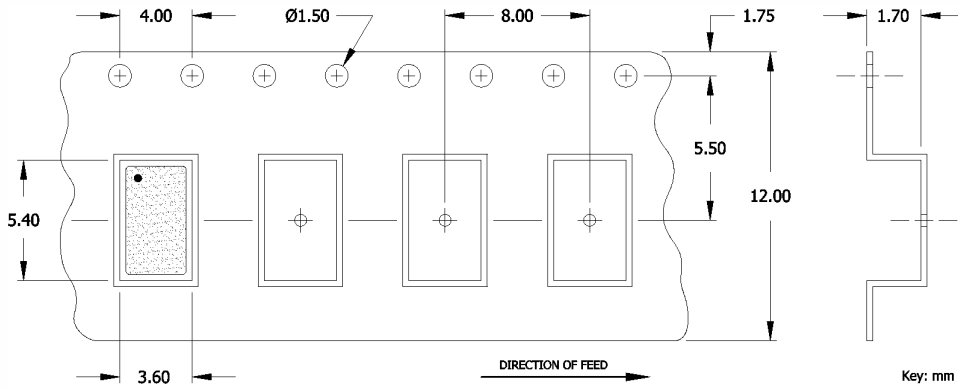
Pin	Symbol	Function
1	EOH or N.C.	Enable [std] or No Connect
2	N.C. or EOH	No Connect or Enable [opt]
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	V _{CC}	Supply Voltage

Table I - Date Code, Beginning year 2021

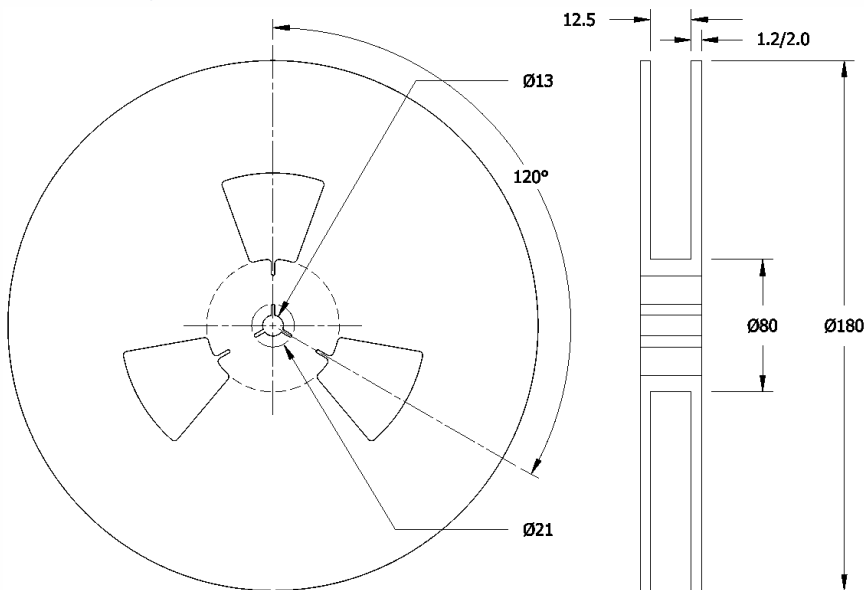
MONTH					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
YEAR																
2021	2025	2029	2033	2037	A	B	C	D	E	F	G	H	J	K	L	M
2022	2026	2030	2034	2038	N	P	Q	R	S	T	U	V	W	X	Y	Z
2023	2027	2031	2035	2039	a	b	c	d	e	f	g	h	j	k	l	m
2024	2028	2032	2036	2040	n	p	q	r	s	t	u	v	w	x	y	z

Packaging - Tape and Reel

Tape Drawing



Reel Drawing



Notes

1. Device quantity is 1k pieces maximum per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.



Addendum

Common Frequencies Available – MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
25.000000	250						
50.000000	500						
74.175800	74A						
74.250000	742						
100.000000	1000						
125.000000	1250						
133.000000	1330						
150.000000	1500						
155.520000	1555						
156.250000	1562						
160.000000	1600						
