

# 74ABT2240

## Octal Buffer/Line Driver with 25Ω Series Resistors in the Outputs

### General Description

The ABT2240 is an inverting octal buffer and line driver designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers, and bus-oriented transmitters/receivers.

The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

### Features

- Guaranteed latchup protection
- High impedance glitch-free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability

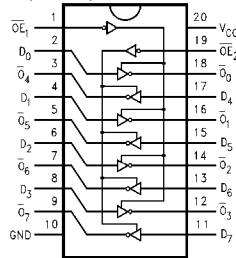
### Ordering Code:

Order Number	Package Number	Package Description
74ABT2240CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ABT2240CSJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT2240CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ABT2240CMTCT	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending letter suffix "X" to the ordering code.

### Connection Diagram

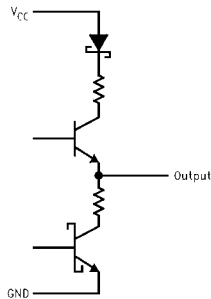
Pin Assignment for SOIC, SSOP, TSSOP and EIAJ



### Pin Descriptions

Pin Names	Descriptions
$\overline{OE}_1, \overline{OE}_2$	Output Enable Input (Active LOW)
$D_0-D_7$	Data Inputs
$\overline{O}_0-\overline{O}_7$	Outputs

### Schematic of Each Output



### Truth Table

$\overline{OE}_1$	$I_{0-3}$	$\overline{O}_{0-3}$	$\overline{OE}_2$	$I_{4-7}$	$\overline{O}_{4-7}$
H	X	Z	H	X	Z
L	H	L	L	H	L
L	L	H	L	L	H

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

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Absolute Maximum Ratings (Note 1)		DC Latchup Source Current (Across Comm Operating Range)	
Storage Temperature	-65°C to +150°C		-300 mA
Ambient Temperature under Bias	-55°C to +125°C	Over Voltage Latchup (I/O)	10V
Junction Temperature under Bias	-55°C to +150°C	<b>Recommended Operating Conditions</b>	
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V	Free Air Ambient Temperature	-40°C to +85°C
Input Voltage (Note 2)	-0.5V to +7.0V	Supply Voltage	+4.5V to +5.5V
Input Current (Note 2)	-30 mA to +5.0 mA	Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
Voltage Applied to Any Output in the Disabled or Power-off State	-0.5V to 5.5V	Data Input	50 mV/ns
in the HIGH State	-0.5V to V <sub>CC</sub>	Enable Input	20 mV/ns
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)	<b>Note 1:</b> Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.	
		<b>Note 2:</b> Either voltage limit or current limit is sufficient to protect inputs.	

## DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.5			V	Min	I <sub>OH</sub> = -3 mA
		2.0			V	Min	I <sub>OH</sub> = -32 mA
V <sub>OL</sub>	Output LOW Voltage			0.8	V	Min	I <sub>OL</sub> = 15 mA
I <sub>IH</sub>	Input HIGH Current			1	μA	Max	V <sub>IN</sub> = 2.7V (Note 3) V <sub>IN</sub> = V <sub>CC</sub>
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-1	μA	Max	V <sub>IN</sub> = 0.5V (Note 3)
				-1	μA	Max	V <sub>IN</sub> = 0.0V
V <sub>ID</sub>	Input Leakage Test				V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OZH</sub>	Output Leakage Current			10	μA	0 - 5.5V	V <sub>OUT</sub> = 2.7V; $\overline{OE}_n = 2.0V$
I <sub>OZL</sub>	Output Leakage Current			-10	μA	0 - 5.5V	V <sub>OUT</sub> = 0.5V; $\overline{OE}_n = 2.0V$
I <sub>OS</sub>	Output Short-Circuit Current			-275	mA	Max	V <sub>OUT</sub> = 0.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0	V <sub>OUT</sub> = 5.5V; All Others GND
I <sub>CCH</sub>	Power Supply Current			50	μA	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current			30	mA	Max	All Outputs LOW
I <sub>CCZ</sub>	Power Supply Current			50	μA	Max	$\overline{OE}_n = V_{CC}$ All Others at V <sub>CC</sub> or GND
I <sub>CCT</sub>	Additional Outputs Enabled			1.5	mA		V <sub>I</sub> = V <sub>CC</sub> - 2.1V
	I <sub>CC</sub> /Input Outputs 3-STATE			1.5	mA	Max	Enable Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V
	Outputs 3-STATE			50	μA		Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V All Others at V <sub>CC</sub> or GND
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> (Note 3)	No Load		0.1	mA/ MHz	Max	Outputs Open $\overline{OE}_n = GND$ (Note 4) One Bit Toggling, 50% Duty Cycle

**Note 3:** Guaranteed, but not tested.

**Note 4:** For 8 bits toggling, I<sub>CCD</sub> < 0.8 mA/MHz.

## AC Electrical Characteristics

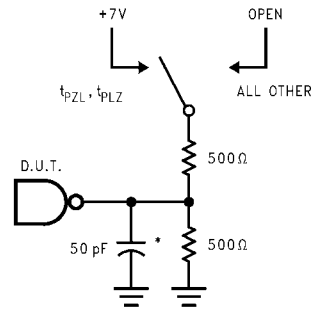
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V-5.5V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation	1.0		4.9	1.0	4.9	ns
t <sub>PHL</sub>	Delay Data to Outputs	1.5		5.3	1.5	5.3	
t <sub>PZH</sub>	Output Enable	1.5		6.6	1.5	6.6	ns
t <sub>PZL</sub>	Time	2.7		6.9	2.7	6.9	
t <sub>PHZ</sub>	Output Disable	1.9		6.4	1.9	6.4	ns
t <sub>PLZ</sub>	Time	1.9		6.4	1.9	6.4	

## Capacitance

Symbol	Parameter	Typ	Units	Conditions T <sub>A</sub> = 25°C
C <sub>IN</sub>	Input Capacitance	5.0	pF	V <sub>CC</sub> = 0V
C <sub>OUT</sub> (Note 5)	Output Capacitance	9.0	pF	V <sub>CC</sub> = 5.0V

Note 5: C<sub>OUT</sub> is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

### AC Loading



\*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

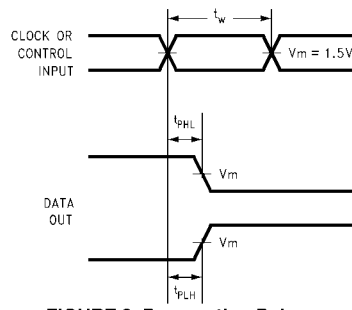


FIGURE 2. Propagation Delay, Pulse Width Waveforms

Amplitude	Rep. Rate	$t_w$	$t_r$	$t_f$
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

### AC Waveforms

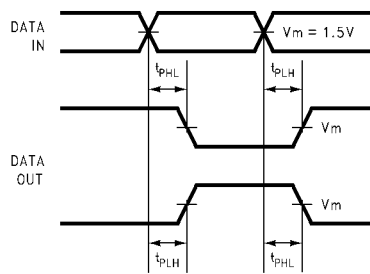


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

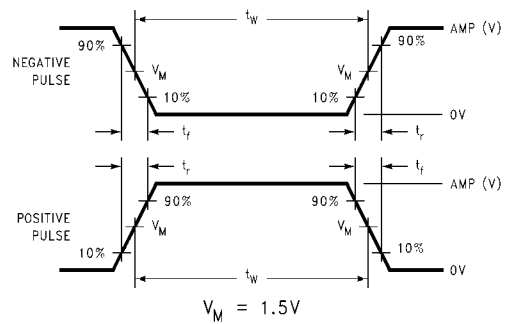


FIGURE 6. Test Input Signal Levels

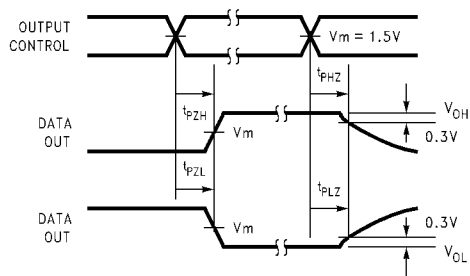


FIGURE 5. 3-STATE Output HIGH and LOW Enable and Disable Times

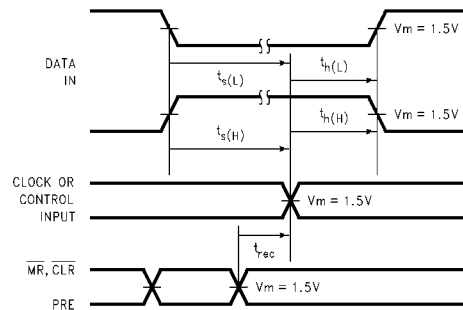
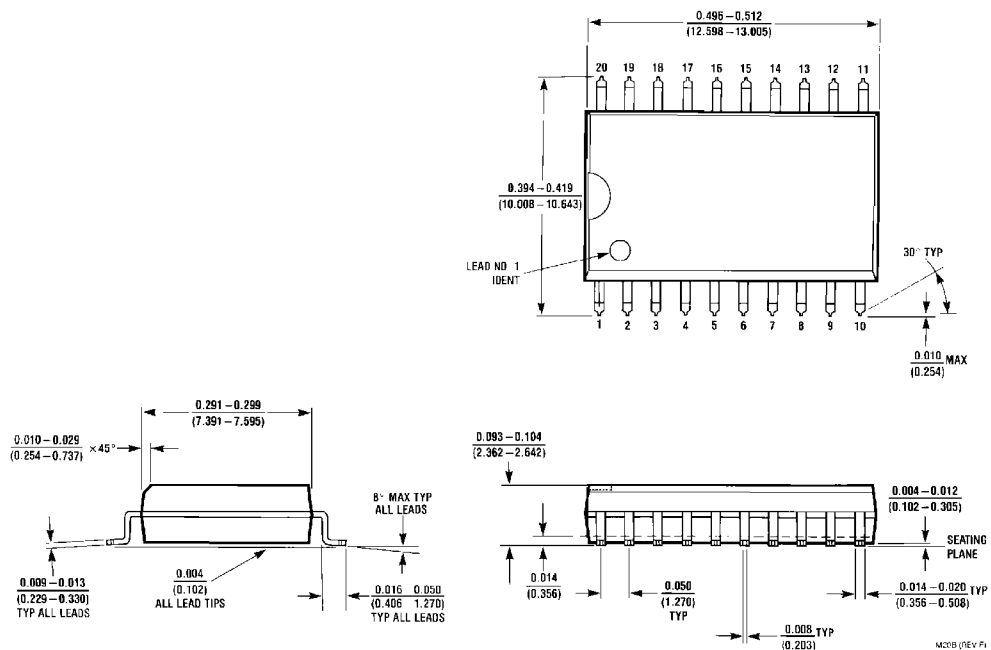
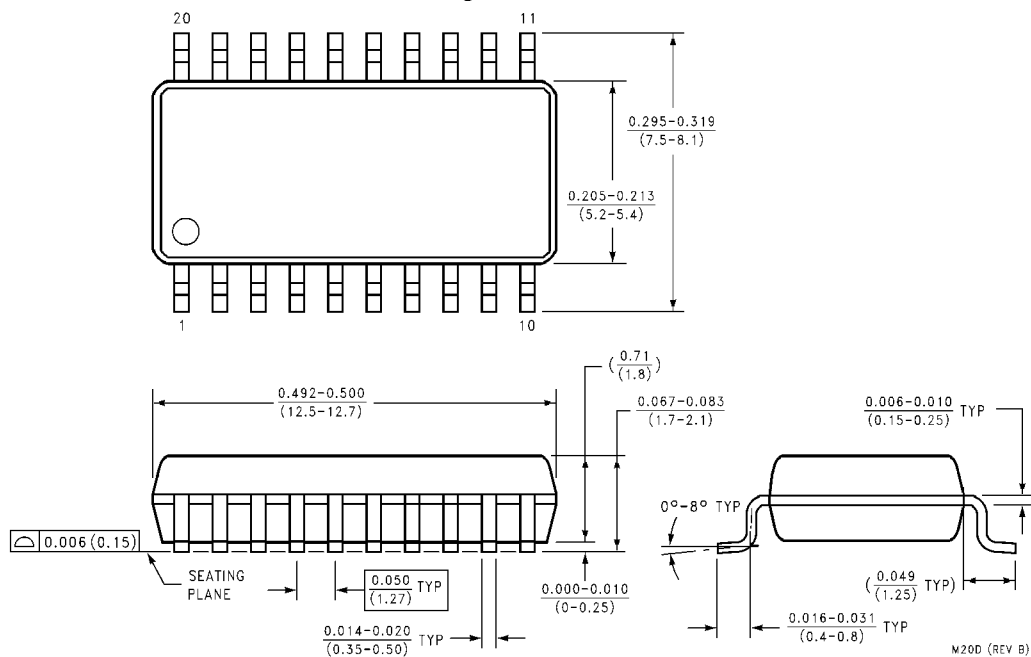


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

**Physical Dimensions** inches (millimeters) unless otherwise noted

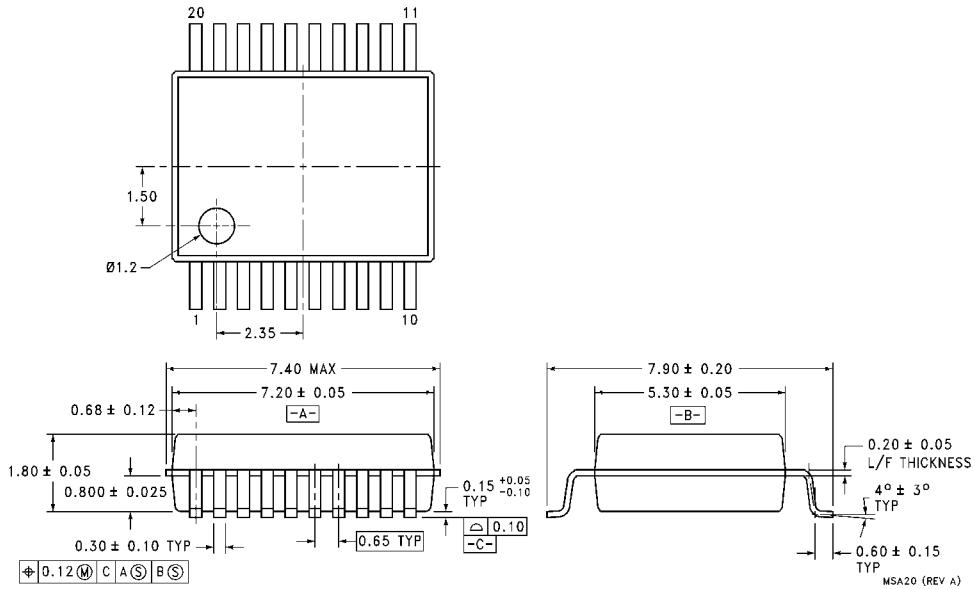


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body  
Package Number M20B**



**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**

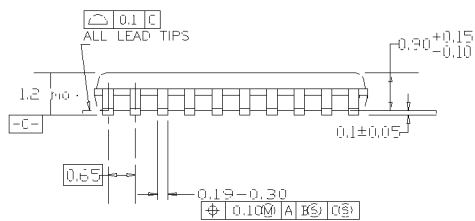
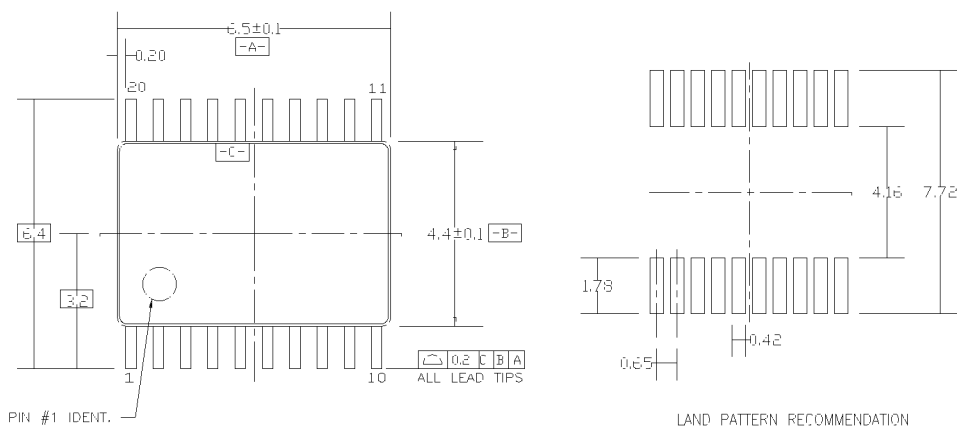
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



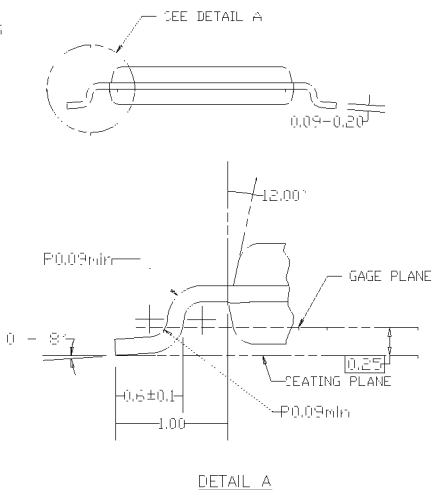
**20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide  
Package Number MSA20**

MSA20 (REV A)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153. VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC20**

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