FOCUS LCDs
LCDs MADE SIMPLE®
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TFT | CHARACTER | UWVD | FSC | SEGMENT | CUSTOM | REPLACEMENT

# TFT Display Module

Part Number

E43RB1-FW405-C

Overview:

- 4.3-inch TFT: (62.5) (H)x105.55(V) mm
- 480(RGB)x800 pixels
- MIPI Interface
- All View/Wide Temp
- White LED back-light
- Transmissive/ Normally Black
- Capacitive Touch Panel
- 405 NITS
- Controller: ILI9806E
- RoHS Compliant

## Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT-LCD Panel, driver circuit, capacitive touch panel and backlight unit. The resolution of the 4.3" TFT-LCD contains 480x800 pixels and can display up to 65K/262K/16.7M colors.

## TFT Features

| General Information Items | Specification | Unit | Note |
|---|---|---|---|
| | Main Panel | | |
| TFT Display area (AA) | 56.16(H)*93.60(V) (4.3inch) | mm | - |
| Driver element | TFT active matrix | - | - |
| Display colors | 16.7M | colors | - |
| Number of pixels | 480(RGB)x800 | dots | - |
| TFT Pixel arrangement | RGB vertical stripe | - | - |
| Pixel pitch | 0.117 (H) x 0.117 (V) | mm | - |
| Viewing angle | ALL | - | - |
| TFT Controller IC | ILI9806E | - | - |
| LCM Interface | MIPI | - | - |
| Display mode | Transmissive/ Normally Black | - | - |
| Operating temperature | -20～+70 | ℃ | - |
| Storage temperature | -30～+80 | ℃ | - |
| Module Bonding | Tape bonding between LCM CTP | - | - |

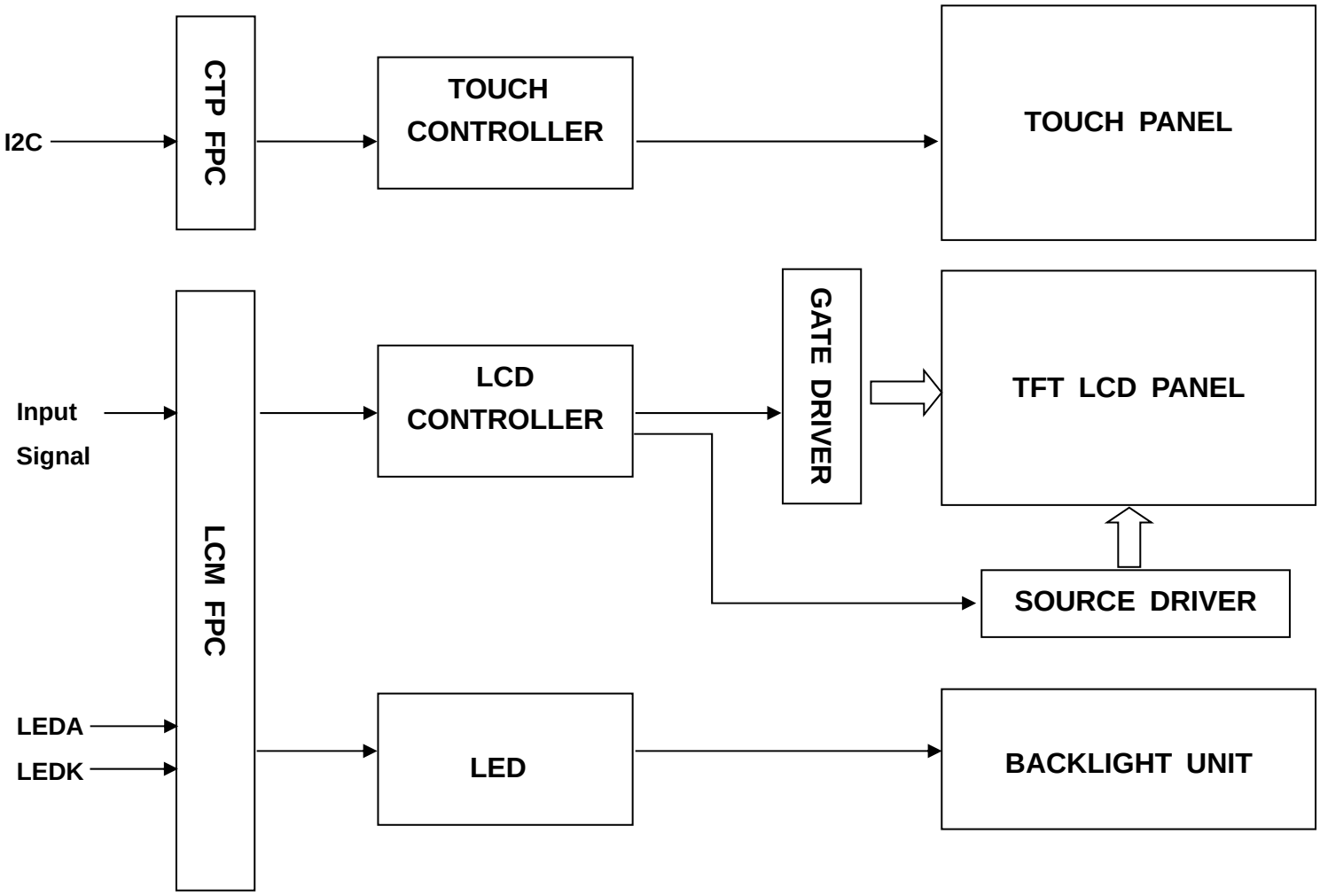
## CTP Features

| General Information Items | Specification | Unit | Note |
|---|---|---|---|
| | Main Panel | | |
| Structure | G+G | - | - |
| Controller IC | GT911 | - | - |
| Interface | I2C | - | - |
| Slave Address | 0x5D(7bit) or 0x14(7bit) | - | - |
| Touch Mode | Five Points and Gestures | - | - |

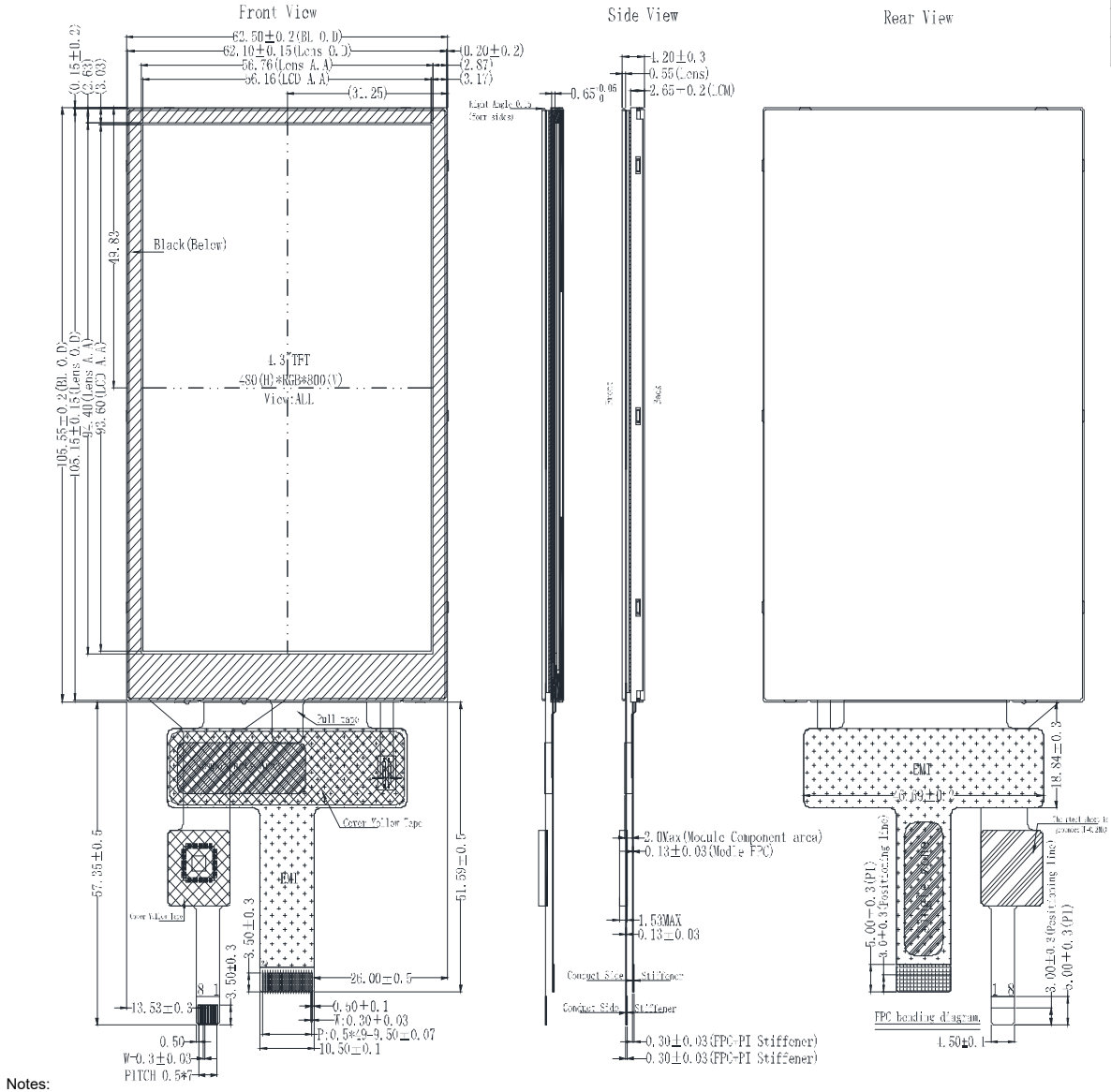
## Mechanical Information

| Item | | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Module size | Height (H) | | 62.5 | | mm | - |
| | Vertical (V) | | 105.55 | | mm | - |
| | Depth (D) | | 4.2 | | mm | - |
| Weight | | | TBD | | g | - |

## 1. Block Diagram



## 2. Outline Dimensions




| Rev. | Description | Date |
|---|---|---|
| 1.0 | First | 3/8/22 |
| | | |

FPC LOGIC

| Pin | Logic |
|---|---|
| 1 | GND |
| 2 | VDDT0 |
| 3 | VDDT0 |
| 4 | SCL |
| 5 | SDA |
| 6 | TXT |
| 7 | RST |
| 8 | GND |

| Number | Pin Name |
|---|---|
| 1 | NC |
| 2 | LEDK |
| 3 | NC |
| 4 | LEDA |
| 5 | NC |
| 6 | VCI |
| 7 | IOVCC |
| 8 | TE |
| 9 | RESET |
| 10 | GND |
| 11 | MIPI_D1P |
| 12 | MIPI_D1N |
| 13 | GND |
| 14 | MIPI_CLP |
| 15 | MIPI_CLN |
| 16 | GND |
| 17 | MIPI_D0P |
| 18 | MIPI_D0N |
| 19 | GND |
| 20 | GND |

Notes:
1. Display type 4.3" TFT TFT LCD, 16.7M Colors
2. Display Mode Normally Black
3. Viewing Direction: All
4. TFT Driver ID: ILI9806E
5. Touch Type: CTP
6. Backlight: White 8 LED 40mA 12.8v (+- 0.3v)
7. TFT Interface MIPI
8. ROHS Compliant



| | | | |
|---|---|---|---|
| Model Name: E43RB1-FW405-C | | FOCUS LCDs LCDs MADE SIMPLE® | |
| General Tol: ± 0.2 | | | |
| Approvals | Date | Drawing No.: | Scale: |
| DWN: | | | |
| CHK: | | Size: | Unit: mm / Page: 1/1 |
| APP: | | | |

# 3. Input Terminal Pin Assignment

| NO. | Symbol | Description | I/O |
|---|---|---|---|
| 1 | NC | NOT CONNECTED | |
| 2 | LEDK | Cathode pin of backlight | P |
| 3 | NC | NOT CONNECTED | |
| 4 | LEDA | Anode pin of backlight | P |
| 5 | NC | NOT CONNECTED | |
| 6 | VCI | Supply Voltage (3.3v). | P |
| 7 | IOVCC | I/O Power supply voltage | P |
| 8 | TE | Tearing Effect Output - leave open when not used | O |
| 9 | RESET | External Reset Input - initializes chip, low input. Execute a power-on reset after supplying power | I |
| 10 | GND | GROUND | P |
| 11 | MIPI_D1P | MIPI DSI differential data pair (DSI-Dn+/-). If MIPI are not used, they should be connected to DGND. | I/O |
| 12 | MIPI_D1N | | |
| 13 | GND | GROUND | |
| 14 | MIPI_CLP | MIPI DSI differential clock pair (DSI-CLK+/-). If MIPI are not used, they should be connected to DGND. | I |
| 15 | MIPI_CLN | | |
| 16 | GND | GROUND | P |
| 17 | MIPI_D0P | MIPI DSI differential data pair (DSI-Dn+/-). If MIPI are not used, they should be connected to DGND | I/O |
| 18 | MIPI_D0N | | |
| 19 | GND | GROUND | P |
| 20 | GND | GROUND | P |

*I: Input, O: Output, P: Power*

### 3.1 CTP

| NO. | Symbol | Description | I/O |
|---|---|---|---|
| 1 | GND | Ground | P |
| 2 | VDDIO | I/O power supply voltage | -- |
| 3 | VDD | Supply voltage | P |
| 4 | SCL | I2C clock input | I |
| 5 | SDA | I2C data input and output | I |
| 6 | INT | External interrupt to host | I |
| 7 | RST | External reset. Low is active. | I |
| 8 | GND | Ground | P |

*I: Input, O: Output, P: Power*

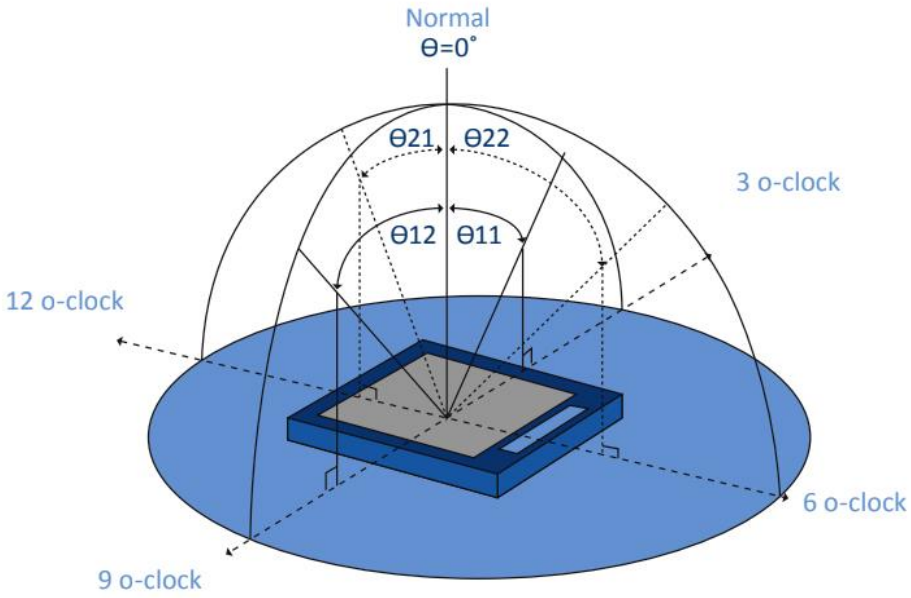
# 4. LCD Optical Characteristics

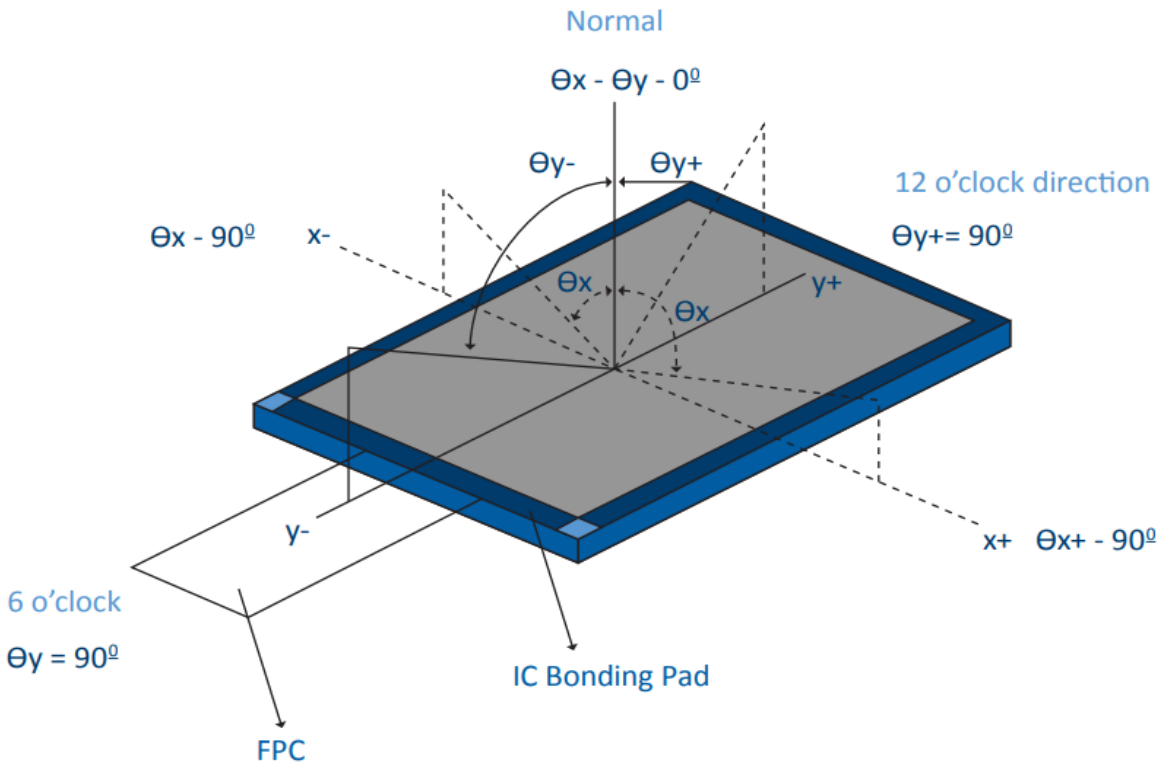
## 4.1 Optical Specifications

| Item | | Symbol | Condition | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Contrast Ratio | | CR | θ=0 Normal viewing angle | 1000 | 1300 | -- | % | (1)(2) |
| Response Time | Rising | TR+TF | | -- | 35 | 40 | msec | (4) |
| | Falling | | | | | | | |
| Color Gamut | | S(%) | | 59 | 64 | -- | % | (5) |
| Color Filter Chromaticity | White | $W_X$ | | 0.2746 | 0.3146 | 0.3546 | | (5)(6) |
| | | $W_Y$ | | 0.3208 | 0.3608 | 0.4008 | | |
| | Red | $R_X$ | | 0.5956 | 0.6356 | 0.6756 | | |
| | | $R_Y$ | | 0.3113 | 0.3513 | 0.3913 | | |
| | Green | $G_X$ | | 0.2720 | 0.3120 | 0.3520 | | |
| | | $G_Y$ | | 0.5324 | 0.5724 | 0.6124 | | |
| | Blue | $B_X$ | | 0.1042 | 0.1442 | 0.1842 | | |
| | | $B_Y$ | | 0.0219 | 0.0619 | 0.0659 | | |
| Viewing angle | Hor. | ΘL | CR≥10 | 70 | 80 | -- | degree | (1)(6) |
| | | ΘR | | 70 | 80 | -- | | |
| | Ver. | ΘT | | 70 | 80 | -- | | |
| | | ΘB | | 70 | 80 | -- | | |
| Option View Direction | | ALL | | | | | | |

**Optical Specification Reference Notes:**

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.

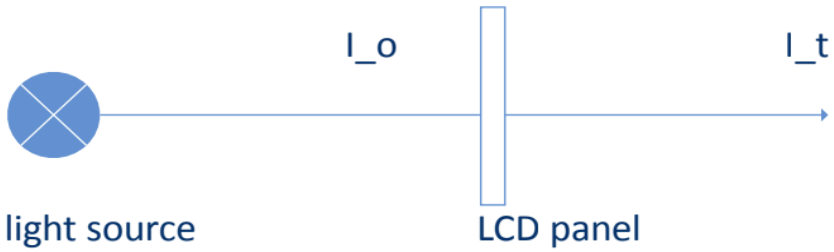


(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving.

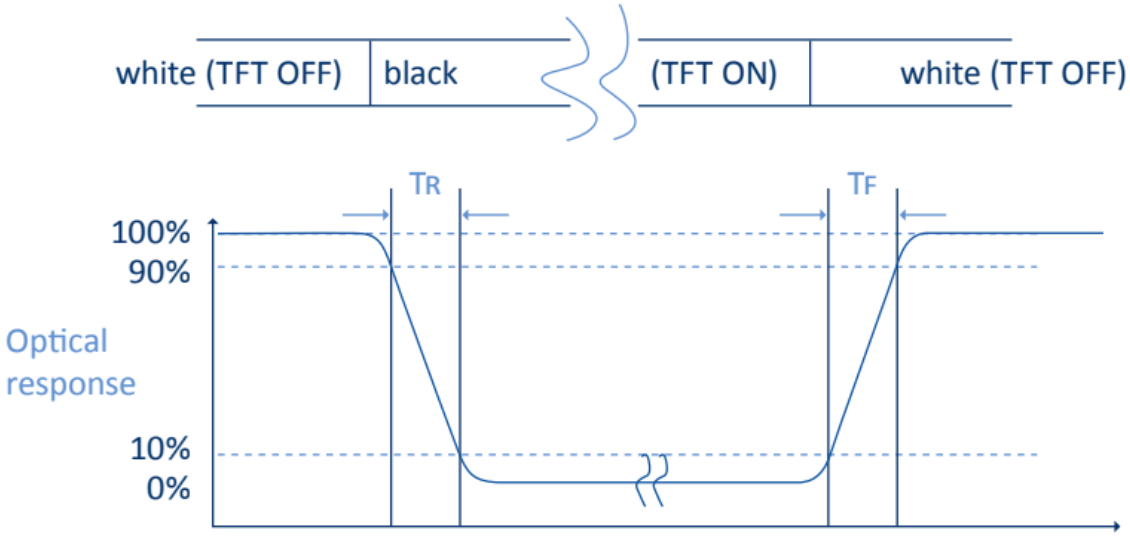



The transmittance is defined as:

$$Tr = \frac{It}{Io}\ x\ 100\%$$

Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90% to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut: Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

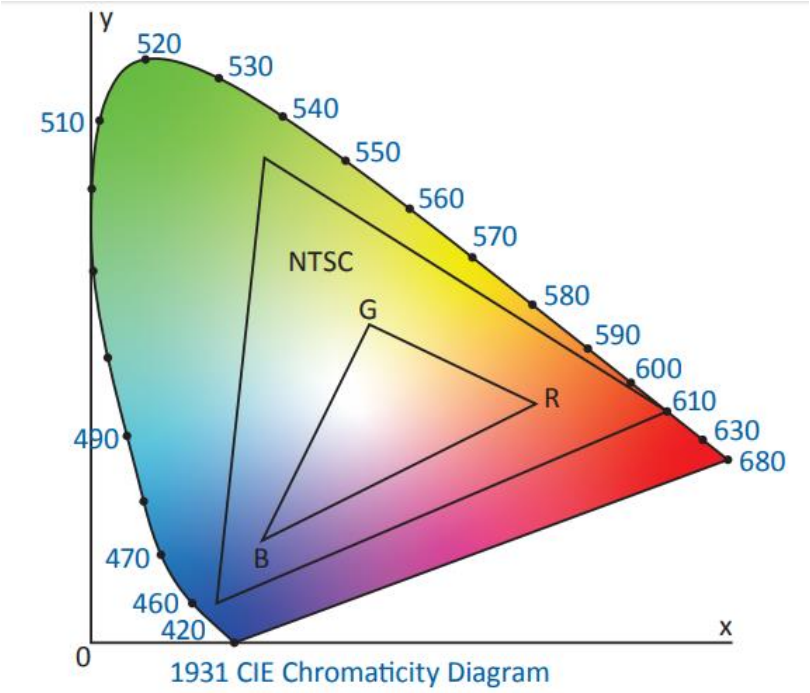
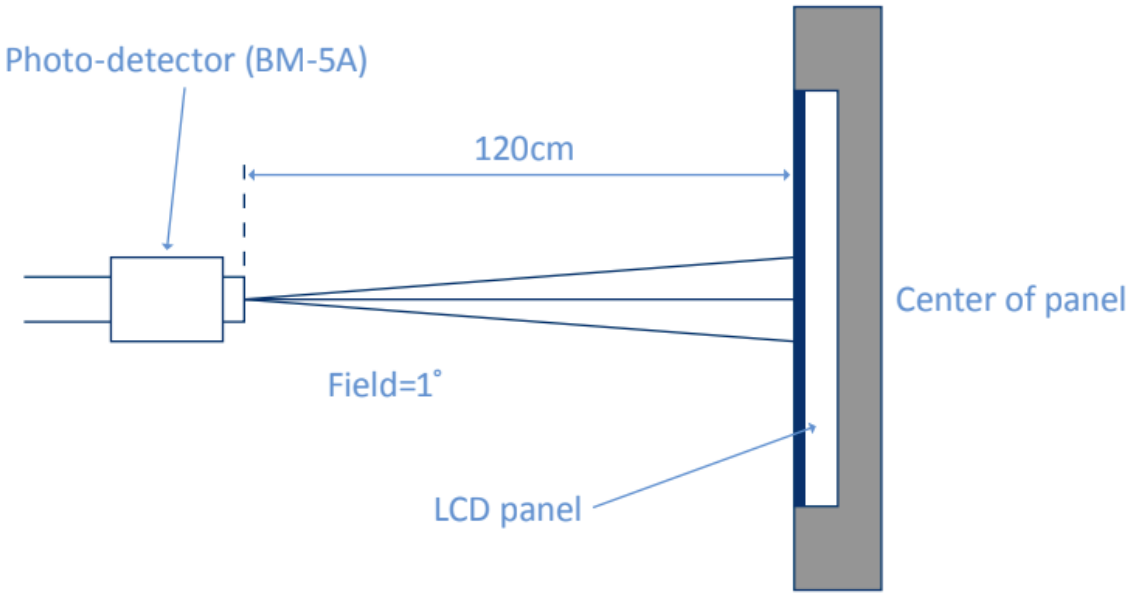


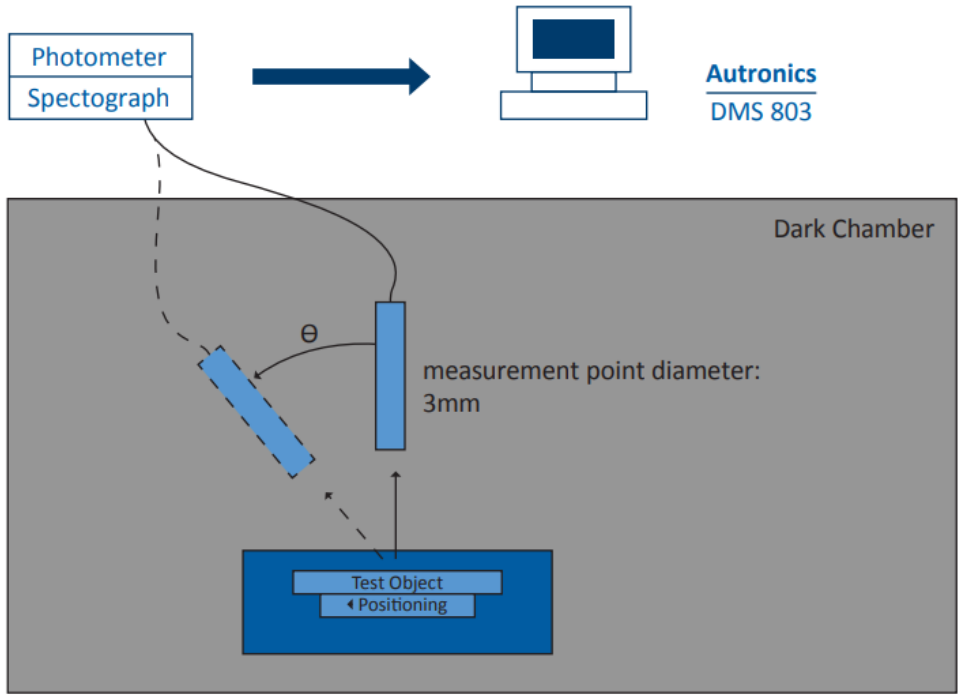

Fig. 1931 CIE chromacity diagram

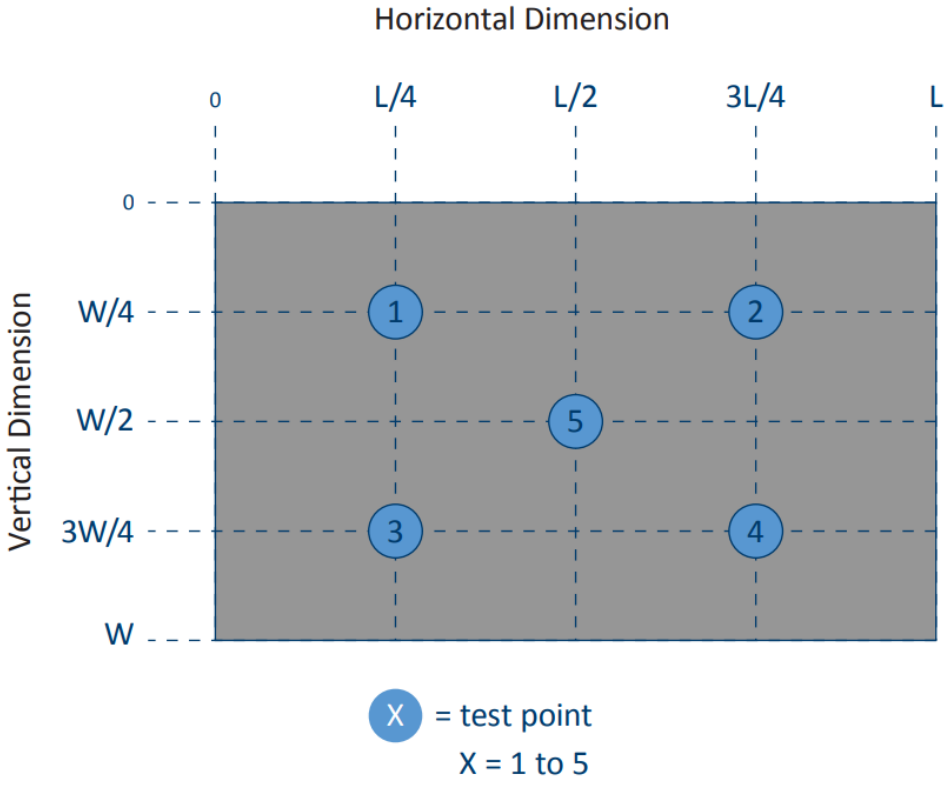
$$\text{Color gamut: } S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$$

(6) Definition of Optical Measurement Setup:



(6) Optical Measurement Setup Continued:
The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.



# 5. TFT Electrical Characteristics

## 5.1 Absolute Maximum Rating (Ta=25 ˚C, VSS=0V)

| Characteristics | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Digital Supply Voltage | VDD | -0.3 | 4.6 | V |
| Operating Temperature | TOP | -20 | +70 | ℃ |
| Storage Temperature | TST | -30 | +80 | ℃ |

*NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.*

## 5.2 DC Electrical Characteristics

| Characteristics | Symbol | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Digital Supply Voltage | VCI | 2.5 | 3.3 | 3.6 | V | |
| Normal Mode Current Consumption | ICC | -- | 30 | 60 | mA | |
| Level Input Voltage | VIH | 0.7*VDDIO | -- | VDDIO | V | |
| | VIL | GND | -- | 0.3*VDDIO | V | |
| Level Output Voltage | VOH | 0.8*VDDIO | -- | VDDIO | V | |
| | VOL | GND | -- | 0.2*VDDIO | V | |
| Digital interface supply Voltage | VDDIO | 1.65 | 1.8 | 3.6 | V | |

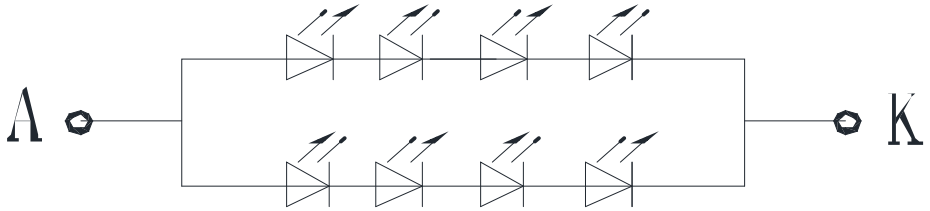
## 5.3 LED Backlight Characteristics

| Item | Symbol | Min | Typ. | Max | Unit | Note |
|---|---|---|---|---|---|---|
| Forward Current | IF | 35 | 40 | -- | mA | |
| Forward Voltage | VF | -- | 12.8 | -- | V | |
| LCM Luminance | LV | 360 | 405 | -- | cd/m2 | Note 3 |
| LED lifetime | Hr | 50000 | -- | -- | hour | Note1 & 2 |
| Uniformity | AVg | 80 | -- | -- | % | Note 3 |

The back-light system is edge-lighting type with 8 chips White LED.

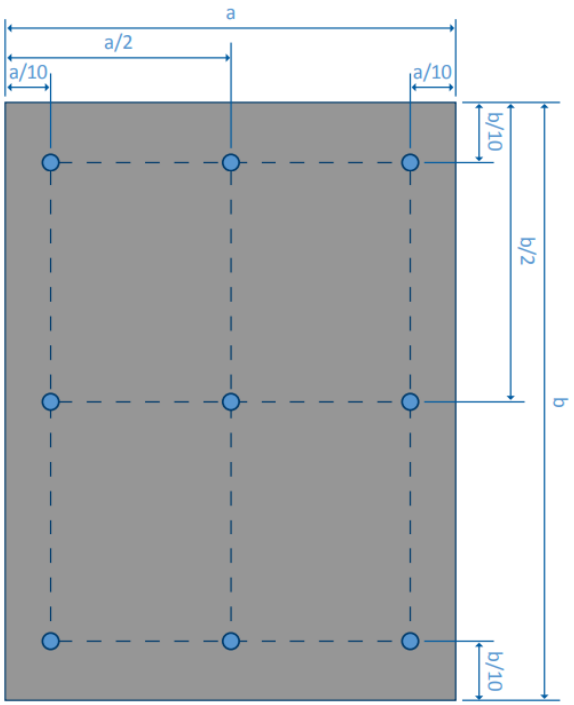
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25 ±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=20mA. The LED lifetime could be decreased if operating IL is larger than 20mA. The constant current driving method is suggested.




B/L Circuit

Note 3: Luminance Uniformity of these 9 points is defined as below:




$$\text{Luminance} = \frac{\text{(Total Luminance of 9 points)}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

# 6. AC Timing Characteristics

## 6.1 Timing for DSI Video Mode

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DCLK Frequency | FCLK | - | -67 | - | MHz |
| Horizontal display area | HDISP | - | 800 | - | Clock |
| Horizontal Sync Width | hpw | 1 | 4 | - | Clock |
| Horizontal Sync Back Porch | hbp | 1 | 38 | - | Clock |
| Horizontal Sync Front Porch | hfp | 1 | 16 | - | Clock |
| Vertical Display Area | VDISP | - | 1280 | - | Line |
| Vertical Sync Width | vs | 1 | 4 | - | Line |
| Vertical Sync Back Porch | vbp | 1 | 10 | - | Line |
| Vertical Sync Front Porch | vfp | 1 | 8 | - | Line |
| Frame Rate | | - | 60 | - | Hz |

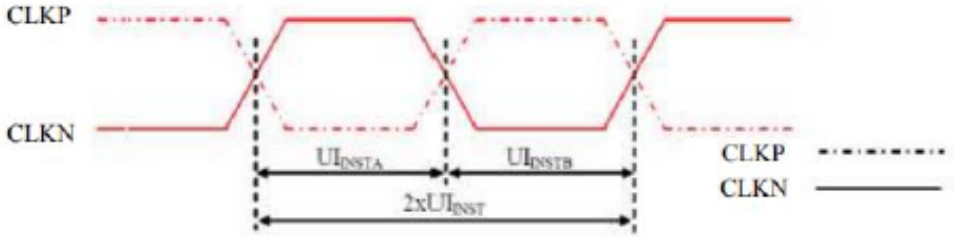



**Figure 116: DSI Clock Channel Timing**

**Table 38: DSI Clock Channel Timing**

| Signal | Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| CLKP/N | $2xUI_{INST}$ | Double UI instantaneous | *Note 2* | 25 | ns |
| CLKP/N | $UI_{INSTA}$,$UI_{INSTB}$ (Note 1) | UI instantaneous Half | *Note 2* | 12.5 | ns |

***Notes:***

*1. UI = UIINSTA = UIINSTB*

*2. Define the minimum value, see Table 39.*

**Table 39: Limited Clock Channel Speed**

| Data type | Two Lanes speed | Three Lanes speed | Four Lanes speed |
|---|---|---|---|
| Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel | 566 Mbps | 466 Mbps | 366 Mbps |
| Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel | 637 Mbps | 525 Mbps | 412 Mbps |
| Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel | 850 Mbps | 700 Mbps | 550 Mbps |
| Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel | 850 Mbps | 700 Mbps | 550 Mbps |

## 6.2 AC Timing Diagrams

### 6.2.1 High Speed Mode - Data Clock Channel Timing

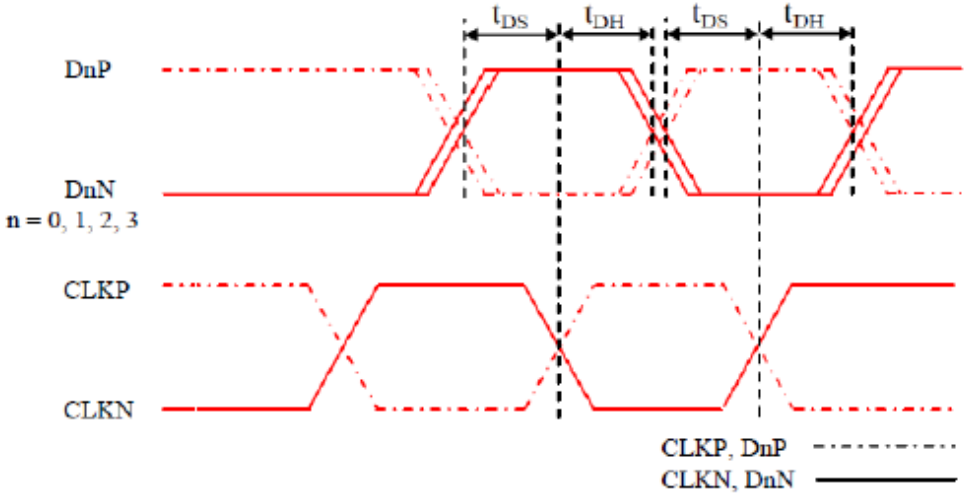



**Figure 119: DSI Data to Clock Channel Timings**

**Table 40: DSI Data to Clock Channel Timings**

| Signal | Symbol | Parameter | Min | Max |
|---|---|---|---|---|
| DnP/N , n=0 and 1 | $t_{DS}$ | Data to Clock Setup time | 0.15xUI | - |
| | $t_{DH}$ | Clock to Data Hold Time | 0.15xUI | - |

### 6.2.2 High Speed Mode - Rise and Fall Timing

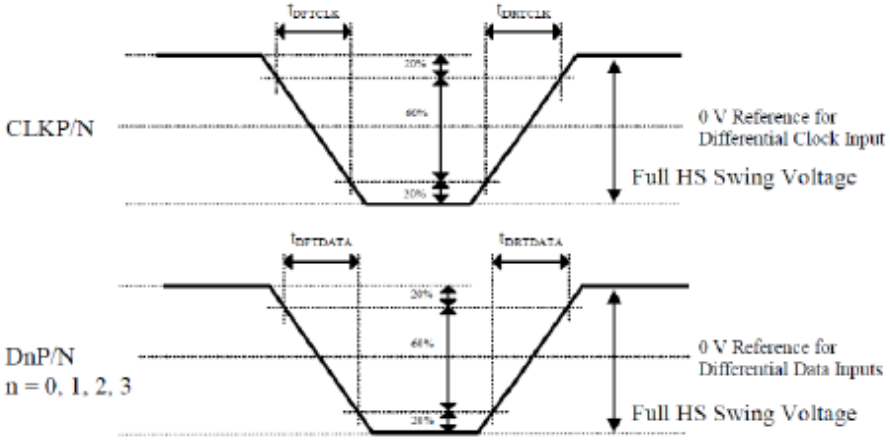



**Figure 120: Rising and Falling Timings on Clock and Data Channels**

**Table 41: Rise and Fall Timings on Clock and Data Channels**

| Parameter | Symbol | Condition | Specification | | |
|---|---|---|---|---|---|
| | | | Min | Typ | Max |
| Differential Rise Time for Clock | $t_{DRTCLK}$ | CLKP/N | 150 ps | - | 0.3UI (Note) |
| Differential Rise Time for Data | $t_{DRTDATA}$ | DnP/N n=0 and 1 | 150 ps | - | 0.3UI (Note) |
| Differential Fall Time for Clock | $t_{DFTCLK}$ | CLKP/N | 150 ps | - | 0.3UI (Note) |
| Differential Fall Time for Data | $t_{DFTDATA}$ | DnP/N n=0 and 1 | 150 ps | - | 0.3UI (Note) |

*Note: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

### 6.2.3 Low Speed Mode - Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

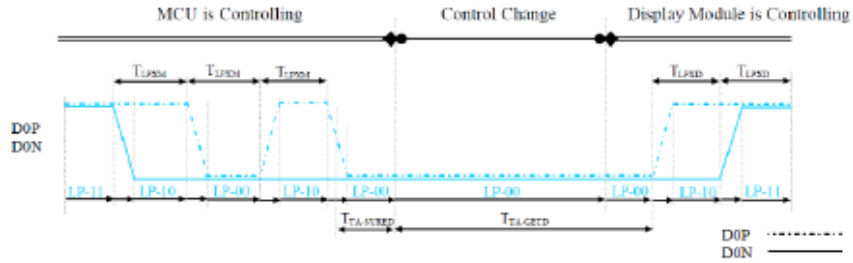



**Figure 121: BTA from the MCU to the Display Module**

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

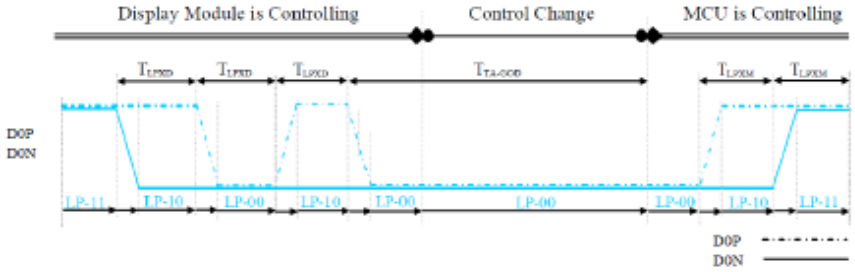



**Figure 122: BTA from the Display Module to the MCU**

**Table 42: Low Power State Period Timings – A**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| D0P/N | $T_{LPXM}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods<br>MCU → Display Module (ILI9881C) | 50 | 75 | ns |
| D0P/N | $T_{LPXD}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods<br>Display Module (ILI9881C) → MCU | 50 | 75 | ns |
| D0P/N | $T_{TA-SURED}$ | Time-out before the Display Module (ILI9881C) starts driving | $T_{LPXD}$ | $2xT_{LPXD}$ | ns |

**Table 43: Low Power State Period Timings – B**

| Signal | Symbol | Description | Time | Unit |
|---|---|---|---|---|
| D0P/N | $T_{TA-GETD}$ | Time to drive LP-00 by Display Module (ILI9881C) | $5xT_{LPXD}$ | ns |
| D0P/N | $T_{TA-GOD}$ | Time to drive LP-00 after turnaround request - MCU | $4xT_{LPXD}$ | ns |

## 6.3 Data Lanes from Low Power Mode to High Speed Mode

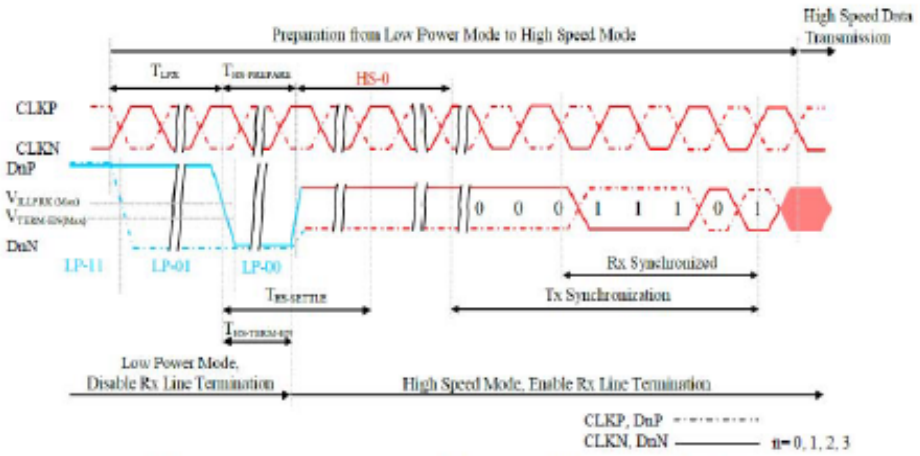



**Figure 123: Data Lanes - Low Power Mode to High Speed Mode Timings**

**Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| DnP/N, n = 0 and 1 | $T_{LPX}$ | Length of any Low Power State Period | 50 | - | ns |
| DnP/N, n = 0 and 1 | $T_{HS-PREPARE}$ | Time to drive LP-00 to prepare for HS Transmission | 40+4xUI | 85+6xUI | ns |
| DnP/N, n = 0 and 1 | $T_{HS-TERM-EN}$ | Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX | - | 35+4xUI | ns |

## 6.4 Data Lanes from High Power Mode to High Speed Mode

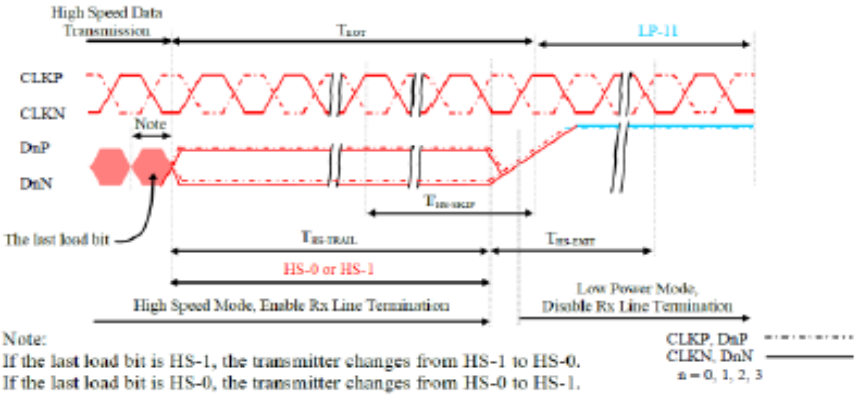



**Figure 124: Data Lanes - High Speed Mode to Low Power Mode Timings**

**Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| DnP/N, n = 0 and 1 | $T_{HS-SKIP}$ | Time-Out at Display Module (ILI9881C) to ignore transition period of EoT | 40 | 55+4xUI | ns |
| DnP/N, n = 0 and 1 | $T_{HS-EXIT}$ | Time to driver LP-11 after HS burst | 100 | - | ns |

## 6.5 DSI Clock Burst - High Speed Mode to/from Low Power Mode

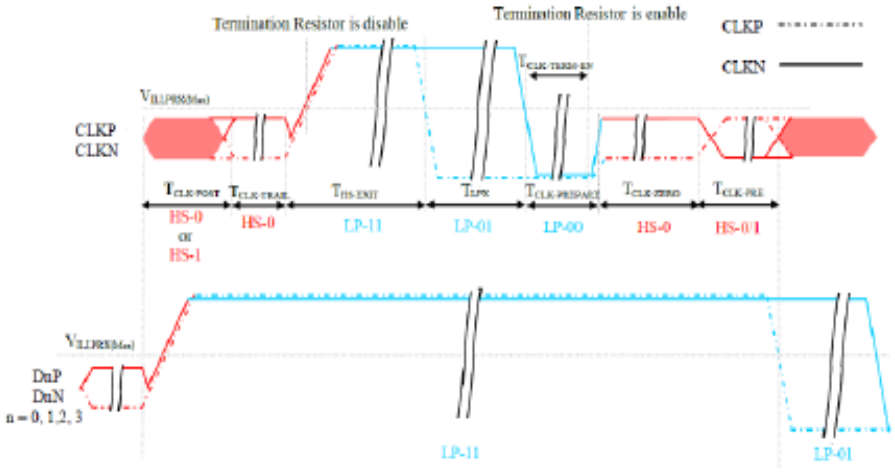



**Figure 125: Clock Lanes - High Speed Mode to/from Low Power Mode Timings**

**Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| CLKP/N | $T_{CLK-POST}$ | Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode | 60+52xUI | - | ns |
| CLKP/N | $T_{CLK-TRAIL}$ | Time to drive HS differential state after last payload clock bit of a HS transmission burst | 60 | - | ns |
| CLKP/N | $T_{HS-EXIT}$ | Time to drive LP-11 after HS burst | 100 | - | ns |
| CLKP/N | $T_{CLK-PREPARE}$ | Time to drive LP-00 to prepare for HS transmission | 38 | 95 | ns |
| CLKP/N | $T_{CLK-TERM-EN}$ | Time-out at Clock Lane to enable HS termination | - | 38 | ns |
| CLKP/N | $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | Minimum lead HS-0 drive period before starting Clock | 300 | - | ns |
| CLKP/N | $T_{CLK-PRE}$ | Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode | 8xUI | - | ns |

# 7. CTP Electrical Characteristics

## 7.1 Absolute Maximum Rating

| Characteristics | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Power Supply Voltage | VDD | 2.66 | 3.47 | V |
| Operating Temperature | TOP | -20 | +70 | ℃ |
| Storage Temperature | TST | -30 | +80 | ℃ |

***Table 7.1: CTP Absolute Maximum Rating Characteristics***

*NOTE: If used beyond the absolute maximum ratings, the quality of the product may be permanently damaged. It is strongly recommended that the device be used within the electrical characteristics in normal operations. If exposed to the conditions not within the electrical characteristics, it may affect the reliability of the device.*

## 7.2 DC Electrical Characteristics (Ta=25˚C)

| Item | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Power Supply Voltage/VDD | 2.66 | 3.3 | 3.47 | V | |
| Normal mode operating current | -- | 8 | 14.5 | mA | |
| Green mode operating current | -- | 3.3 | -- | mA | |
| Sleep mode operating current | 70 | -- | 120 | uA | |
| Doze mode operating current | -- | 0.78 | -- | mA | |
| Digital Input low voltage/VIL | -0.3 | -- | 0.25*VDD | V | |
| Digital Input high voltage/VIH | 0.75*VDD | -- | VDD+0.3 | V | |
| Digital Output low voltage/VOL | -- | -- | 0.15*VDD | V | |
| Digital Output high voltage/VOH | 0.85*VDD | -- | -- | V | |

## 7.3 AC Electrical Characteristics

| Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|
| OSC Oscillation Frequency | 59 | 60 | 61 | Mhz | |
| I/O Output rise time, low to high | - | 14 | - | ns | |
| I/O Output fall time, high to low | - | 14 | - | ns | |

# 8. Cautions and Handling Precautions

## 8.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

## 8.2 Storage and Transportation.

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.