FAIRCHILD SEMICONDUCTOR™

March 1998

74F299
Octal Universal Shift/Storage Register with Common Parallel I/O Pins

General Description

The 'F299 is an 8-bit universal shift/storage register with 3-STATE outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs, Q_0–Q_7, are provided to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

Features

- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- 3-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

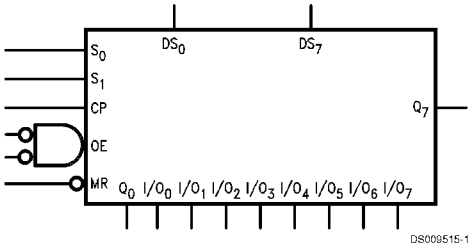
Ordering Code:

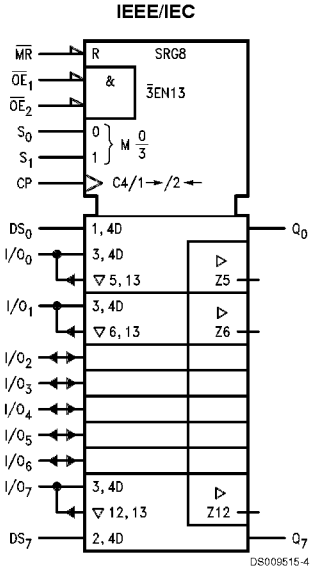
Commercial	Military	Package Number	Package Description
74F299PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F299DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F299SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F299SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F299FM (Note 2)	W20A	20-Lead Cerpack
	54F299LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

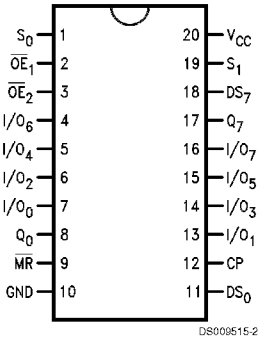
Logic Symbols





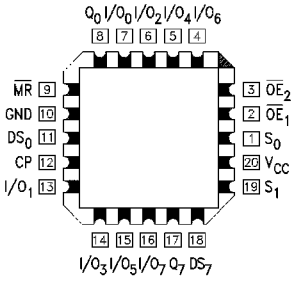
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



DS009515-2

Pin Assignment for LCC



DS009515-3

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/−0.6 mA
DS_0	Serial Data Input for Right Shift	1.0/1.0	20 µA/−0.6 mA
DS_7	Serial Data Input for Left Shift	1.0/1.0	20 µA/−0.6 mA
S_0, S_1	Mode Select Inputs	1.0/2.0	20 µA/−1.2 mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 µA/−0.6 mA
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs (Active LOW)	1.0/1.0	20 µA/−0.6 mA
I/O_0–I/O_7	Parallel Data Inputs or	3.5/1.083	70 µA/−0.65 mA
	3-STATE Parallel Outputs	150/40(33.3)	−3 mA/24 mA (20 mA)
Q_0, Q_7	Serial Outputs	50/33.3	−1 mA/20 mA

Functional Description

The 'F299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

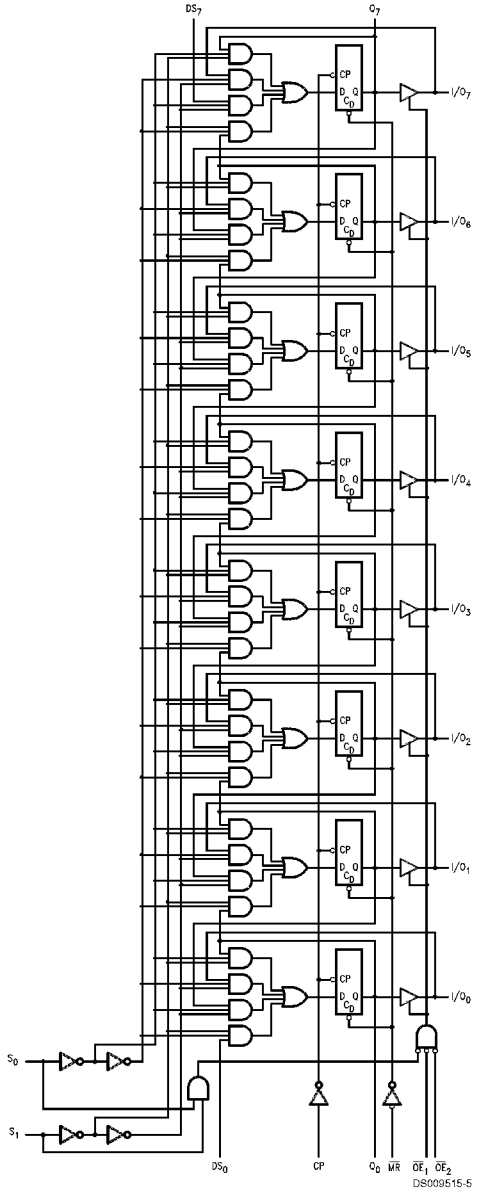
A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-STATE outputs are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0–Q_7 = LOW
H	H	H	⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 3)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 4)	−0.5V to +7.0V
Input Current (Note 4)	−30 mA to +5.0 mA
ESD Last Passing Voltage (Min)	4000V
Voltage Applied to Output in HIGH State (with V_{CC} = 0V) Standard Output 3-STATE Output	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Note 3: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 4: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA (Q_0, Q_7, I/O_n)
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA (I/O_n)
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA (Q_0, Q_7, I/O_n)
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA (I/O_n)
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA (Q_0, Q_7, I/O_n)
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA (I/O_n)
V_{OL}	Output LOW Voltage	54 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74 10% V_{CC}			0.5			I_{OL} = 20 mA (Q_0, Q_7)
		74 10% V_{CC}			0.5			I_{OL} = 24 mA (I/O_n)
I_{IH}	Input HIGH Current	54F			20.0	µA	Max	V_{IN} = 2.7V (CP, DS_0, DS_7, S_0, S_1, $\overline{MR}$, $\overline{OE}_1$, $\overline{OE}_2$)
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	µA	Max	V_{IN} = 7.0V (CP, DS_0, DS_7, S_0, S_1, $\overline{MR}$, $\overline{OE}_1$, $\overline{OE}_2$)
		74F			7.0			
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)	54F			1.0	mA	Max	V_{IN} = 5.5V (I/O_n)
		74F			0.5			
I_{CEX}	Output HIGH Leakage Current	54F			250	µA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 µA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	µA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (CP, DS_0, DS_7, $\overline{MR}$, $\overline{OE}_1$, $\overline{OE}_2$)
					−1.2			V_{IN} = 0.5V (S_0, S_1)
I_{IH}+ I_{OZH}	Output Leakage Current				70	µA	Max	$V_{I/O}$ = 2.7V (I/O_n)
I_{IL}+ I_{OZL}	Output Leakage Current				−650	µA	Max	$V_{I/O}$ = 0.5V (I/O_n)

DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V_{CC}	Conditions
		Min	Typ	Max			
I_{OS}	Output Short-Circuit Current	−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test			500	µA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		68	95	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		68	95	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		68	95	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74F			54F		74F		Units
		T_A = +25°C V_{CC} = +5.0V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Input Frequency	70	100		85		70		MHz
t_{PLH}	Propagation Delay	4.0	7.0	8.0	4.0	9.0	4.0	8.5	
t_{PHL}	CP to Q_0 or Q_7	4.5	6.5	8.0	4.5	9.5	4.5	8.5	ns
t_{PLH}	Propagation Delay	3.5	7.0	9.0	3.5	10.0	3.5	10.0	
t_{PHL}	CP to I/O_n	4.0	8.5	9.0	4.0	11.0	4.0	10.0	
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	5.5	7.5	9.5	5.5	12.5	5.5	10.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	5.5	11.0	10.0	5.5	12.0	5.5	10.5	
t_{PZH}	Output Enable Time	3.5	6.0	8.0	3.0	9.5	3.5	9.0	
t_{PZL}	$\overline{OE}$ to I/O_n	4.0	7.0	10.0	4.0	13.0	4.0	11.0	ns
t_{PHZ}	Output Disable Time	2.0	4.5	6.0	1.5	7.0	2.0	7.0	
t_{PLZ}	$\overline{OE}$ to I/O_n	1.0	4.0	5.5	1.0	6.5	1.0	6.5	
t_{PZH}	Output Enable Time	3.5		9.0	3.0	10.5	3.5	10.0	ns
t_{PZL}	S_n to I/O_n	4.0		10.0	4.0	13.0	4.0	11.0	
t_{PHZ}	Output Disable Time	2.5		6.0	1.5	7.0	2.5	7.0	ns
t_{PLZ}	S_n to I/O_n	1.5		5.5	1.0	6.5	1.5	6.5	

AC Operating Requirements

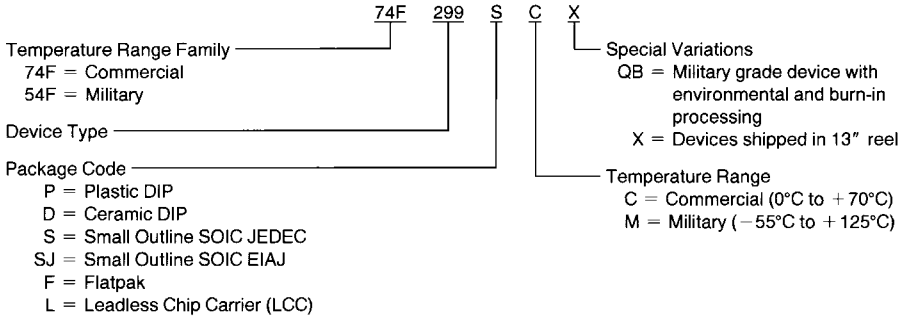
Symbol	Parameter	74F		54F		74F		Units
		T_A = +25°C V_{CC} = +5.0V		T_A, V_{CC} = Mil		T_A, V_{CC} = Com		
		Min	Max	Min	Max	Min	Max	
$t_s(H)$	Setup Time, HIGH or LOW	8.5		10.0		8.5		
$t_s(L)$	S_0 or S_1 to CP	8.5		7.5		8.5		ns
$t_h(H)$	Hold Time, HIGH or LOW	0		0		0		
$t_h(L)$	S_0 or S_1 to CP	0		0		0		
$t_s(H)$	Setup Time, HIGH or LOW	5.0		5.0		5.0		
$t_s(L)$	I/O_n, DS_0 or DS_7 to CP	5.0		5.0		5.0		ns
$t_h(H)$	Hold Time, HIGH or LOW	2.0		2.0		2.0		
$t_h(L)$	I/O_n, DS_0 or DS_7 to CP	2.0		2.0		2.0		

AC Operating Requirements (Continued)

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$		54F T_A, V_{CC} = Mil		74F T_A, V_{CC} = Com		Units
		Min	Max	Min	Max	Min	Max	
$t_w(H)$	CP Pulse Width	5.0		5.0		5.0		ns
$t_w(L)$	HIGH or LOW	5.0		5.0		5.0		
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW	5.0		6.0		5.0		ns
t_{rec}	Recovery Time, $\overline{MR}$ to CP	7.0		12.0		7.0		ns

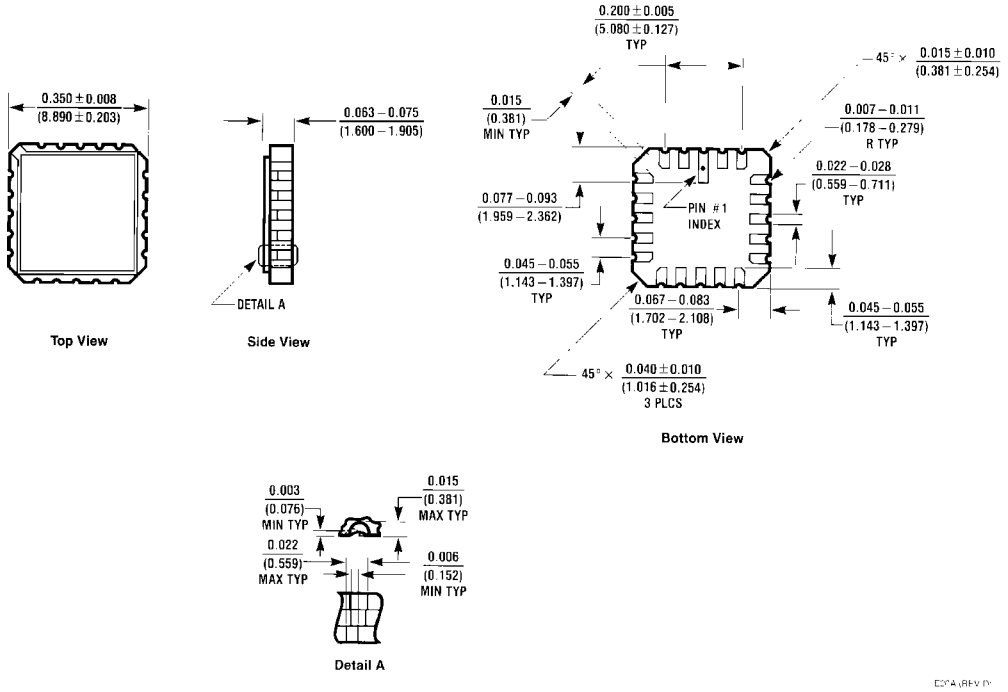
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

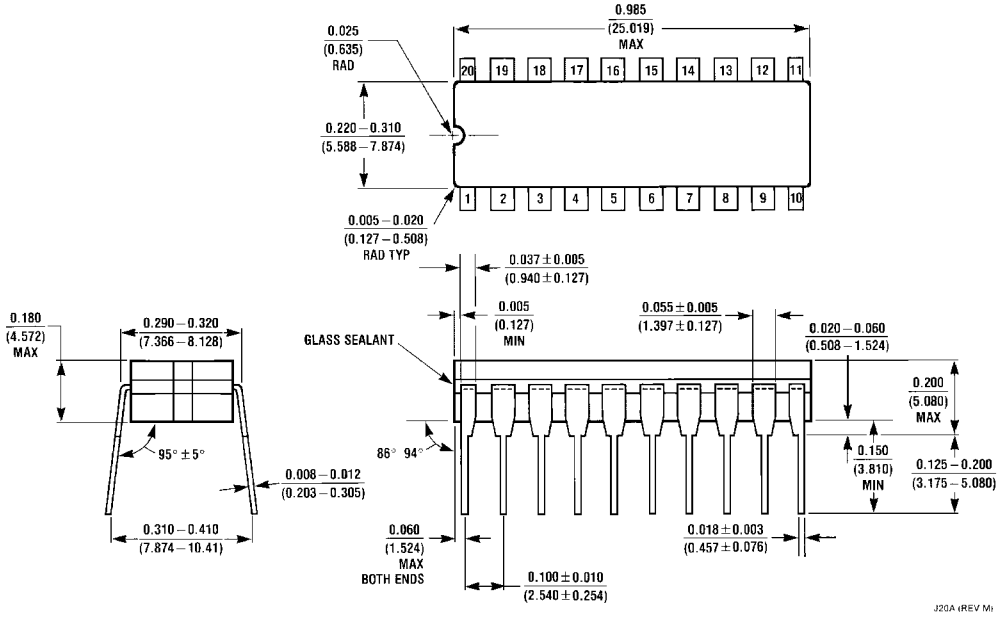


DS009515-6

Physical Dimensions inches (millimeters) unless otherwise noted

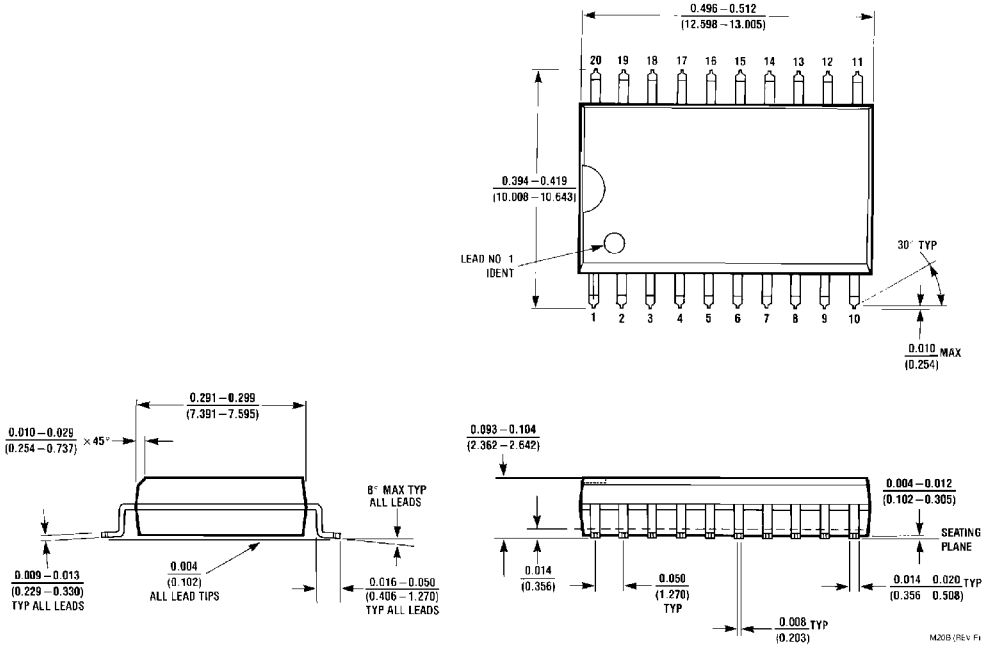


20-Lead Ceramic Leadless Chip Carrier (L)
Package Number E20A



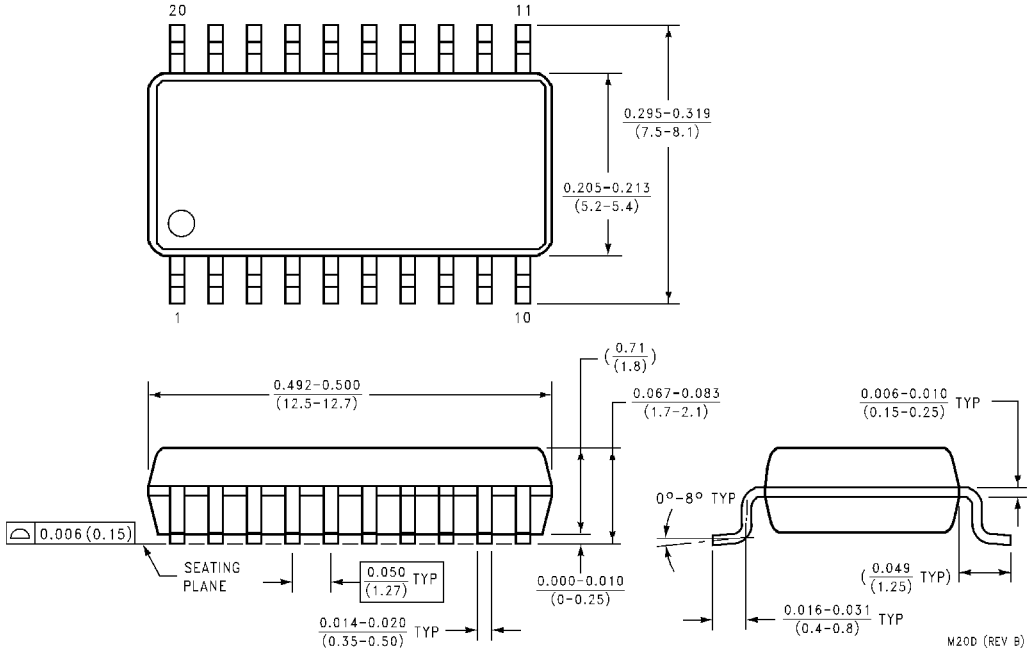
20-Lead Ceramic Dual-In-Line Package (D)
Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

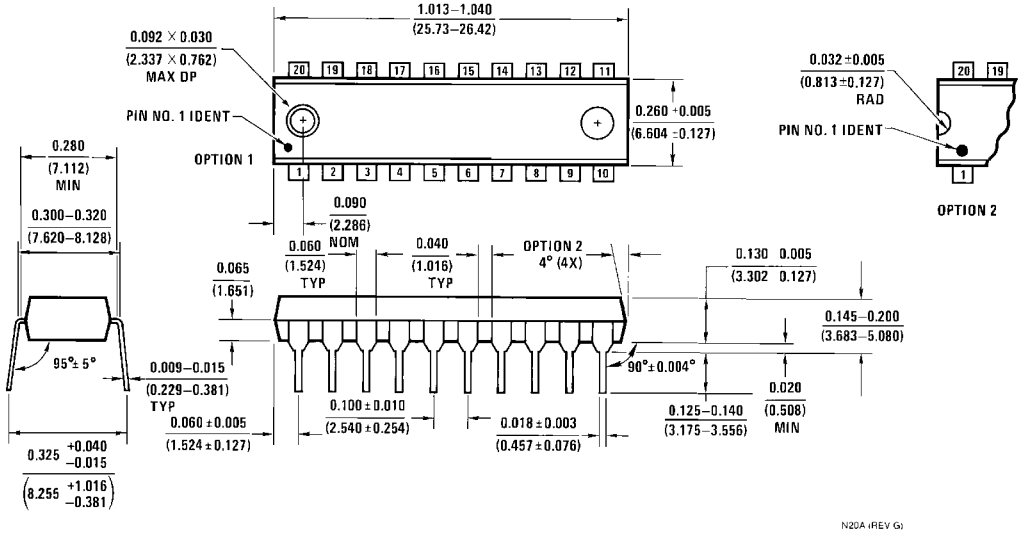


20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

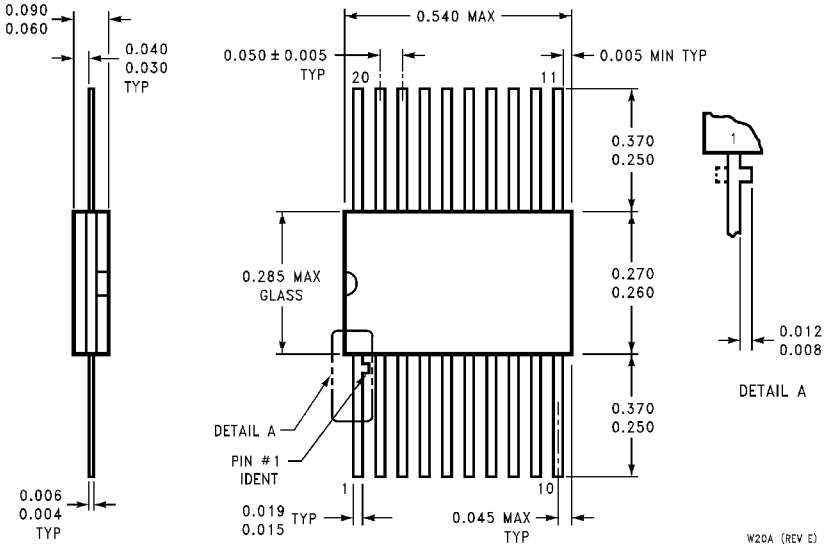


20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
Package Number MD20D



20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
Package Number N20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Cerpack
Package Number W20A

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel: 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

www.fairchildsemi.com