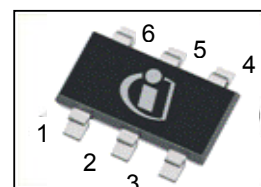
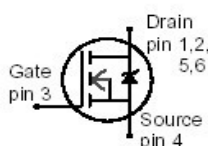


OptiMOS[®] 2 Small-Signal-Transistor
Features

- N-channel
- Enhancement mode
- Logic level (4.5V rated)
- Avalanche rated
- dv/dt rated
- Pb-free lead plating; RoHS compliant
- Qualified according to AEC Q101


Product Summary

V_{DS}		30	V
$R_{DS(on),max}$	$V_{GS}=10\text{ V}$	25	$m\Omega$
	$V_{GS}=4.5\text{ V}$	38	
I_D		7.1	A

PG-TSOP-6


Type	Package	Tape and Reel Information	Marking	Lead Free	Packing
BSL302SN	PG-TSOP-6	L6327 = 3000 pcs. / reel	sPE	Yes	Non dry

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_A=25\text{ °C}$	7.1	A
		$T_A=70\text{ °C}$	5.7	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ °C}$	28	
Avalanche energy, single pulse	E_{AS}	$I_D=7.1\text{ A}$, $R_{GS}=25\ \Omega$	30	mJ
Reverse diode dv/dt	dv/dt	$I_D=7.5\text{ A}$, $V_{DS}=16\text{ V}$, $di/dt=200\text{ A}/\mu\text{s}$, $T_{j,max}=150\text{ °C}$	6	kV/ μs
Gate source voltage	V_{GS}		± 20	V
Power dissipation ¹⁾	P_{tot}	$T_A=25\text{ °C}$	2	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 150	$^{\circ}\text{C}$
ESD Class		JESD22-A114-HBM	0 (0V to 250V)	
Soldering Temperature			260 $^{\circ}\text{C}$	
IEC climatic category; DIN IEC 68-1			55/150/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - minimal footprint	R_{thJS}		-	-	50	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	230	
		6 cm ² cooling area ¹⁾	-	-	62.5	

Electrical characteristics, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=250\text{ }\mu\text{A}$	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=30\text{ }\mu\text{A}$	1.2	1.70	2	
Drain-source leakage current	I_{DSS}	$V_{DS}=20\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$	-	-	1	μA
		$V_{DS}=20\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ }^\circ\text{C}$	-	-	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=5.7\text{ A}$	-	27	38	$\text{m}\Omega$
		$V_{GS}=10\text{ V}, I_D=7.1\text{ A}$	-	18	25	
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=7.1\text{ A}$		16	-	S

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (single layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air. ($t < 5\text{ sec.}$)

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	564	750	pF
Output capacitance	C_{oss}		-	202	269	
Reverse transfer capacitance	C_{rss}		-	28	43	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=7.1\text{ A}, R_G=1.6\ \Omega$	-	6.4	-	ns
Rise time	t_r		-	2.8	-	
Turn-off delay time	$t_{d(off)}$		-	13.7	-	
Fall time	t_f		-	1.9	-	

Gate Charge Characteristics

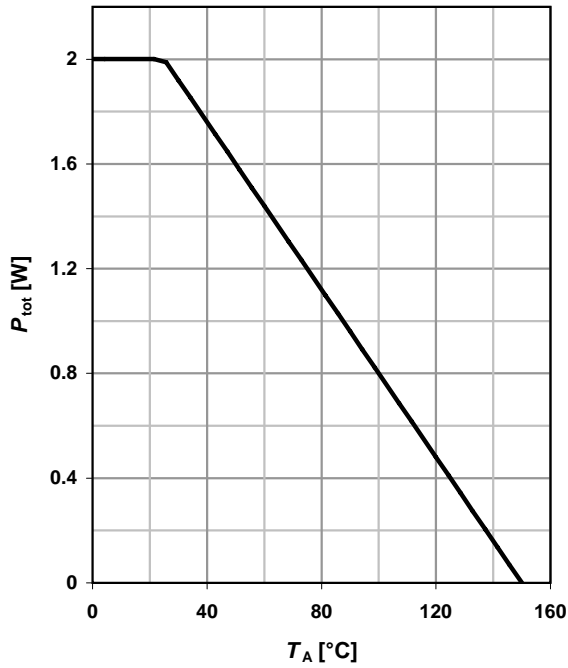
Gate to source charge	Q_{gs}	$V_{DD}=15\text{ V}, I_D=7.1\text{ A},$ $V_{GS}=0\text{ to }5\text{ V}$	-	1.78	2.37	nC
Gate to drain charge	Q_{gd}		-	1.2	1.8	
Gate charge total	Q_g		-	4.4	6.6	
Gate plateau voltage	$V_{plateau}$		-	3.2	-	V

Reverse Diode

Diode continuous forward current	I_S	$T_A=25\text{ }^\circ\text{C}$	-	-	2.5	A
Diode pulse current	$I_{S,pulse}$		-	-	28	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=7.1\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.8	1.2	V
Reverse recovery time	t_{rr}	$V_R=15\text{ V}, I_F=7.1\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	14.2	-	ns
Reverse recovery charge	Q_{rr}		-	5.1	-	nC

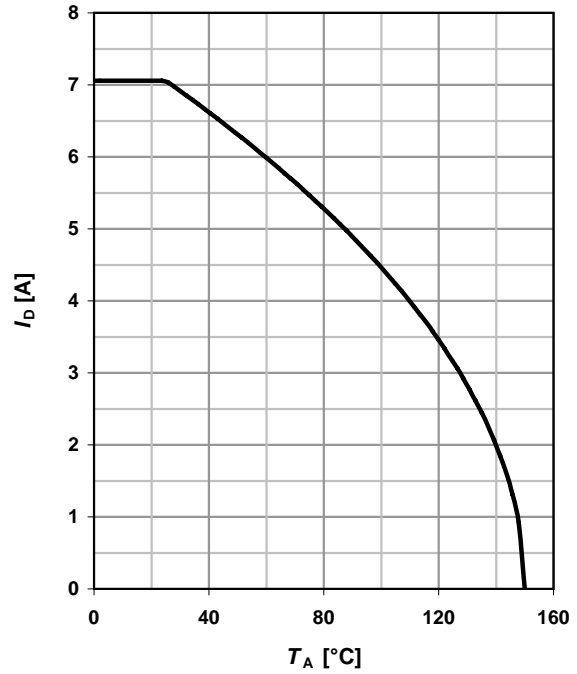
1 Power dissipation

$$P_{tot} = f(T_A)$$



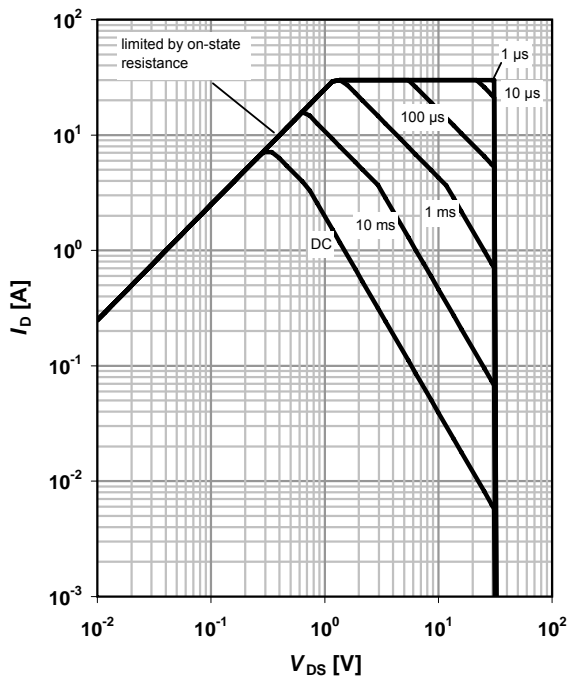
2 Drain current

$$I_D = f(T_A); V_{GS} \geq 10 \text{ V}$$



$$I_D = f(V_{DS}); T_A = 25 \text{ °C}; D = 0$$

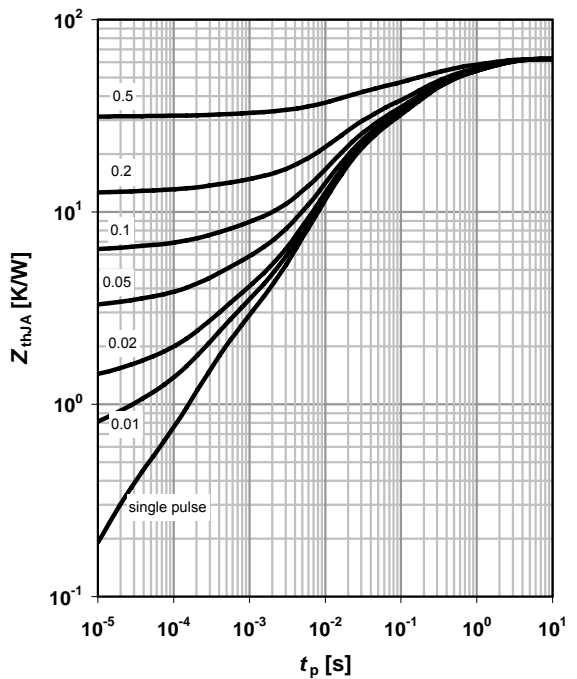
parameter: t_p



4 Max. transient thermal impedance

$$Z_{thJA} = f(t_p)$$

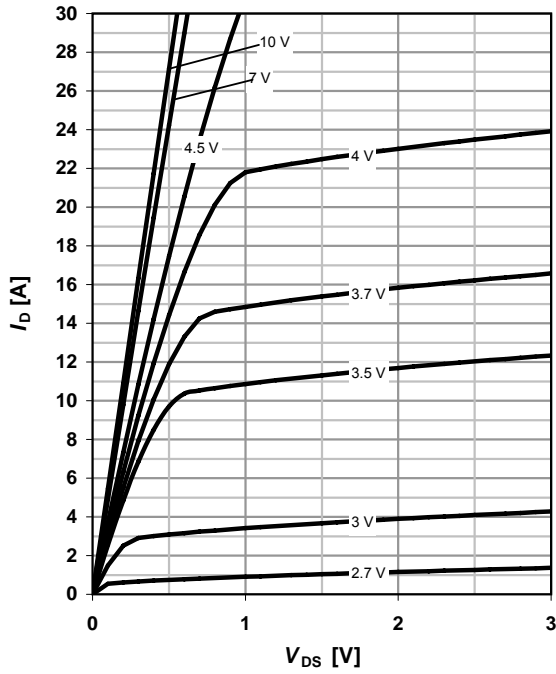
parameter: $D = t_p / T$



5 Typ. output characteristics

$$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$$

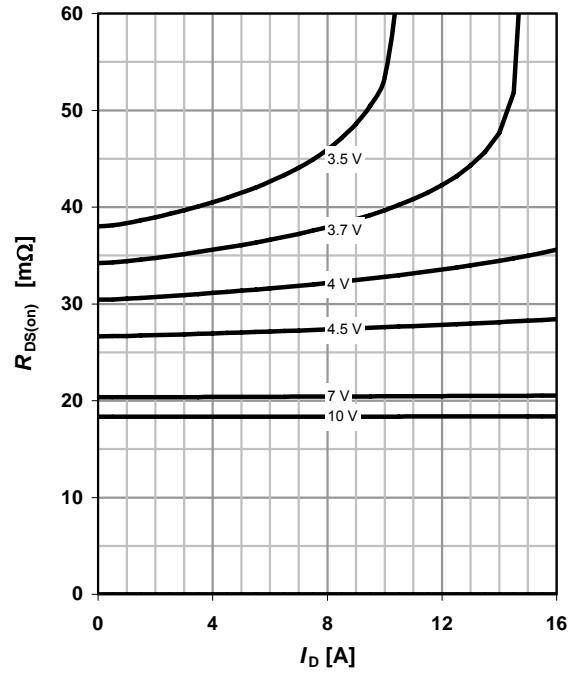
parameter: V_{GS}



6 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$$

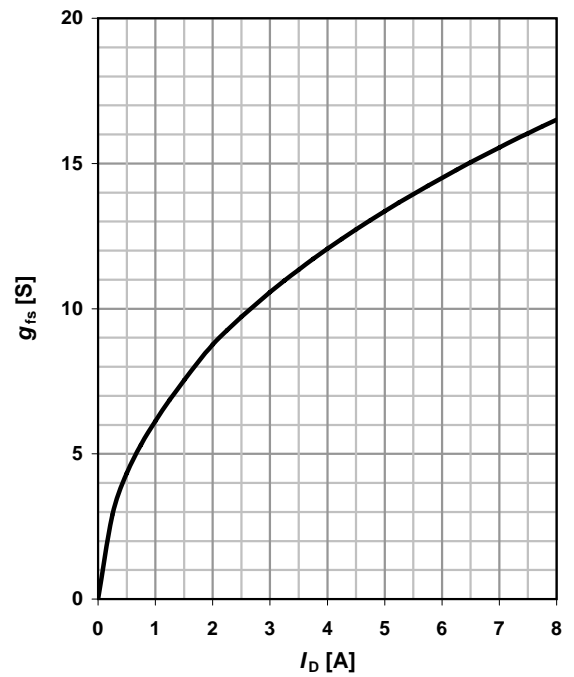
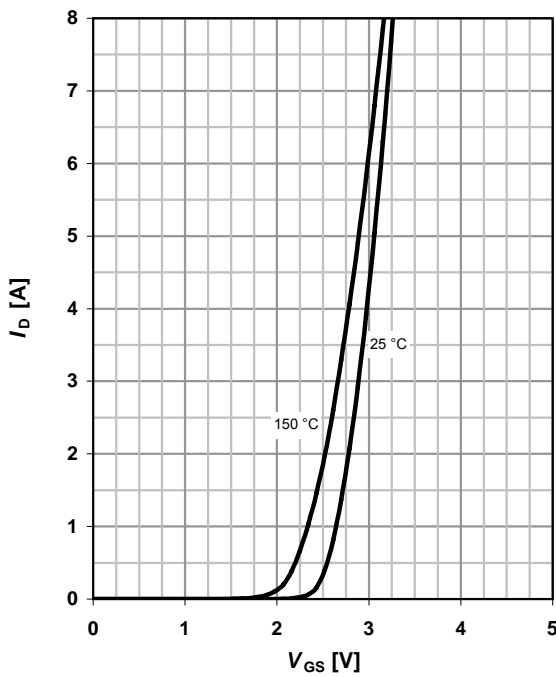
parameter: V_{GS}



8 Typ. forward transconductance

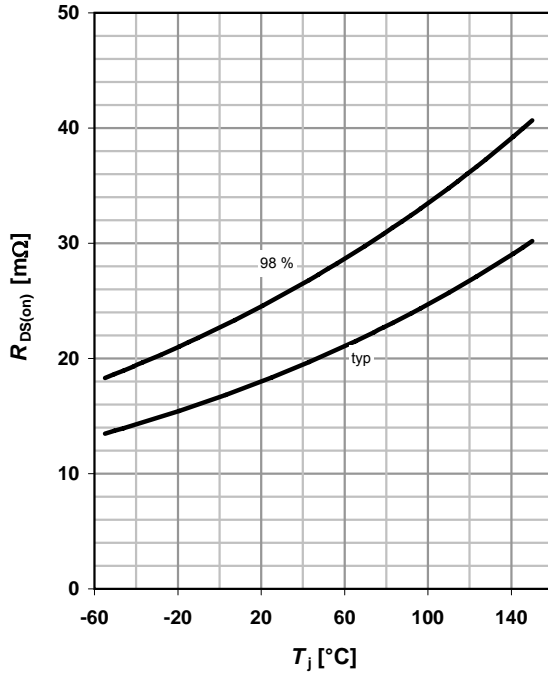
$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$$

$$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$$



9 Drain-source on-state resistance

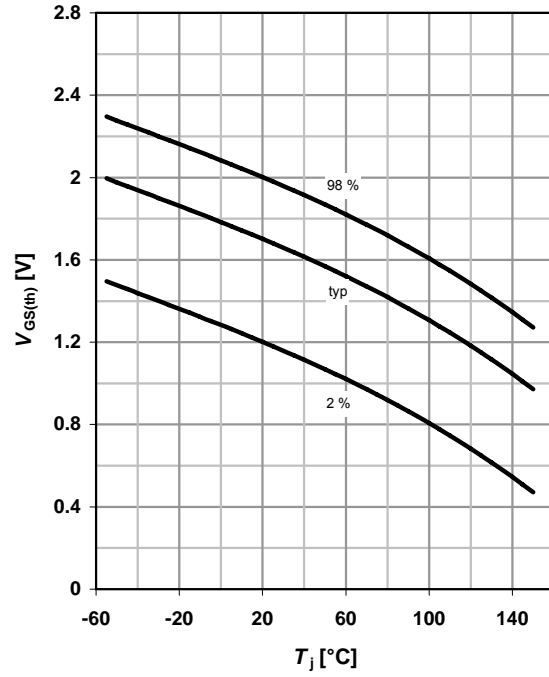
$R_{DS(on)} = f(T_j); I_D = 7.1 \text{ A}; V_{GS} = 10 \text{ V}$



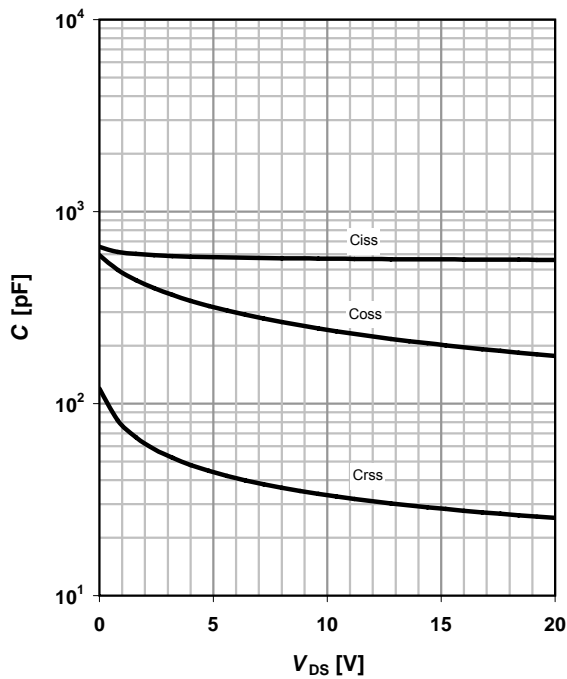
10 Typ. gate threshold voltage

$V_{GS(th)} = f(T_j); V_{DS} = V_{GS}; I_D = 30 \mu\text{A}$

parameter: I_D



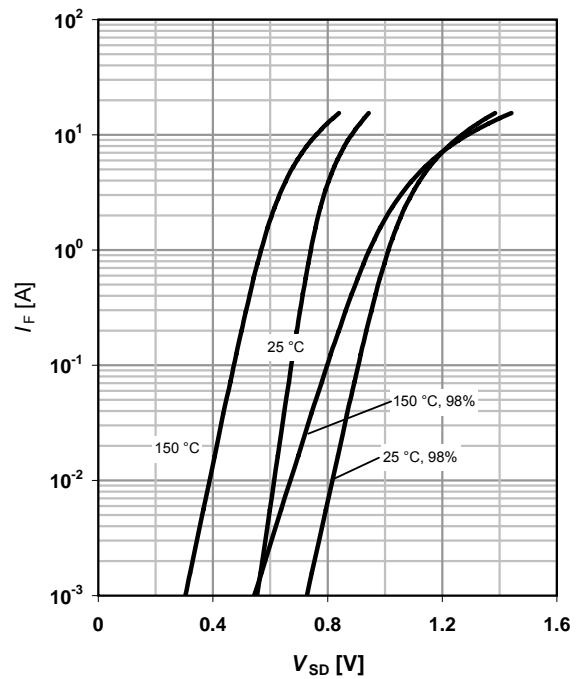
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25^\circ\text{C}$



12 Forward characteristics of reverse diode

$I_F = f(V_{SD})$

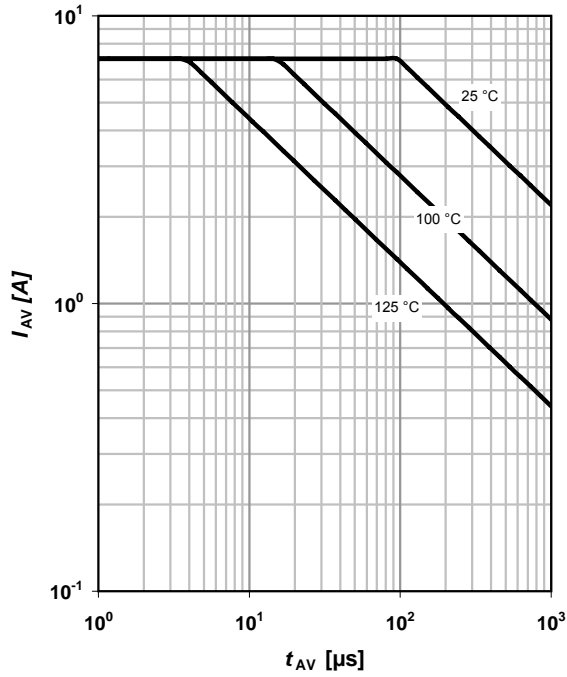
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

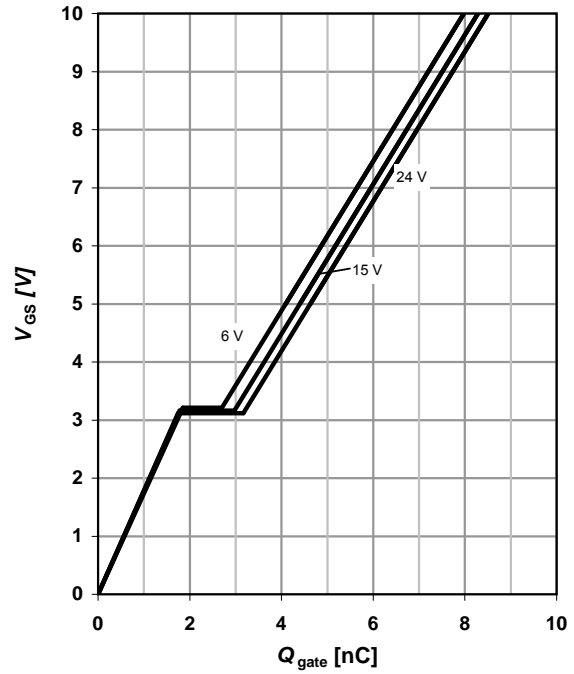
parameter: $T_{j(start)}$



14 Typ. gate charge

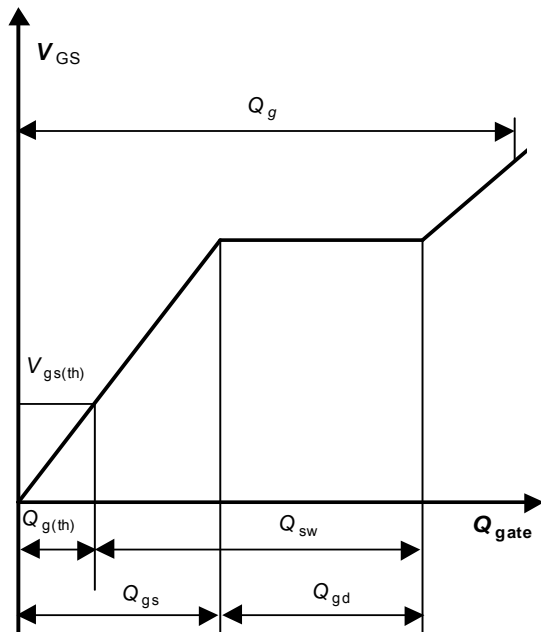
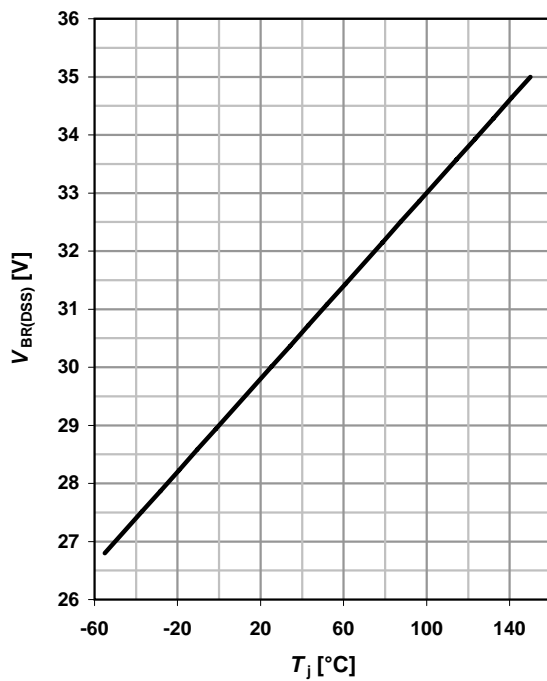
$V_{GS}=f(Q_{gate}); I_D=7.1 \text{ A pulsed}$

parameter: V_{DD}



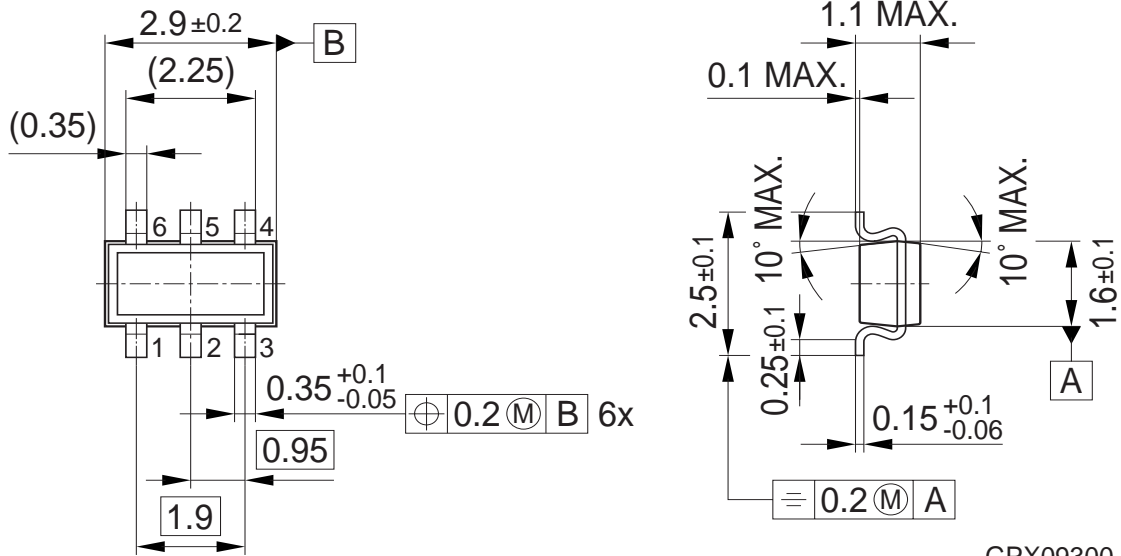
16 Gate charge waveforms

$V_{BR(DSS)}=f(T_j); I_D=250 \mu\text{A}$

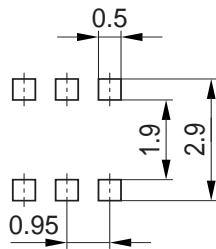


Package Outline:

TSOP6



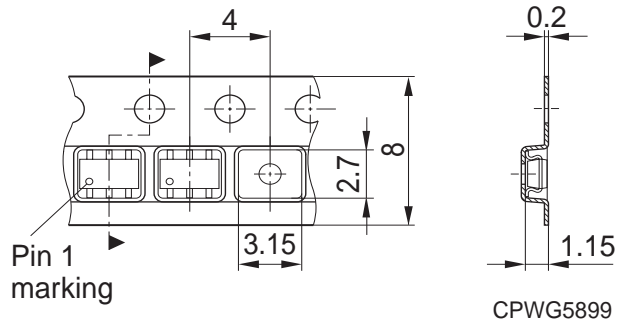
Footprint:



Remark: Wave soldering possible dep. on customers process conditions

HLG09283

Packaging:



Dimensions in mm

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