Description

The DIODES™ AP33510 is a highly integrated, quasi-resonant, flyback, GaN FET controller specially designed for offline flyback power supplies that require low standby power, high-power density, and comprehensive protection.

The controller operates in QR mode at full load. This makes switching events always occur in the drain-source valley, minimizing switching loss. The maximum switching frequency is internally limited to 150kHz. To ensure stable valley switching and prevent transformer audible noise caused by frequency hopping, the AP33510 features a proprietary valley-lockout technique inside.

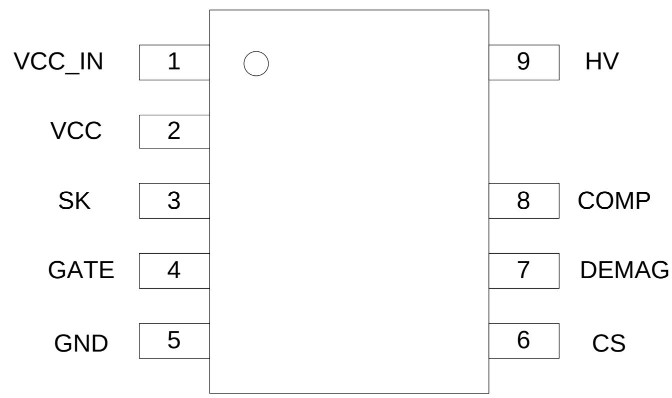
When load decreases from full load, the IC will enter into PFM mode with frequency foldback for higher power conversion efficiency. At no load or light load, the controller will enter burst mode to minimize power consumption, and the minimum switching frequency (about 25kHz) is set to avoid any audible noise.

Piecewise linear line compensation ensures constant output power limit over an entire line voltage range.

To ensure converter ruggedness, the AP33510 implements comprehensive protective features such as brown-in/out detection, cycle-by-cycle current limiting, output OVP/UVP, overload protection, and overtemperature protection.

Pin Assignments

SSOP-9 (Type CJ)



Top View

Features

- Up to 150kHz Quasi-Resonant Operation Mode for High Output Voltage
- Frequency Foldback for High Average Efficiency
- High Reliability Gate Driver for GaN FET
- Built-in High-Voltage Startup
- Soft Start During Startup Process
- Integrated X2 Capacitor Discharge Function
- Adaptive Output Power Limit with Output Voltage
- Non-Audible-Noise Green-Mode Control
- Wide VCC Power Supplied with 120V LDO
- Internal Slope Compensation
- Frequency Dithering for Reducing EMI
- VCC Maintain Mode
- Comprehensive System Protection Features:
  - Secondary Winding Short Protection
  - VCC Overvoltage Protection (VOVP)
  - Line Overvoltage Protection (LOVP)
  - Overload Protection (OLP)
  - Cycle-by-Cycle Over-Current Protection
  - Pin-Fault Protection
  - Brown In/Out Protection (BNI/BNO)
  - Secondary Side OVP (SOVP) and UVP (SUVP)
  - Internal OTP
- Packaged in the SSOP-9 (Type CJ)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/

Applications

- General GaN FET drivers
- Programmable switching AC/DC adapters or quick chargers
- High-density industrial and consumer power supplies

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

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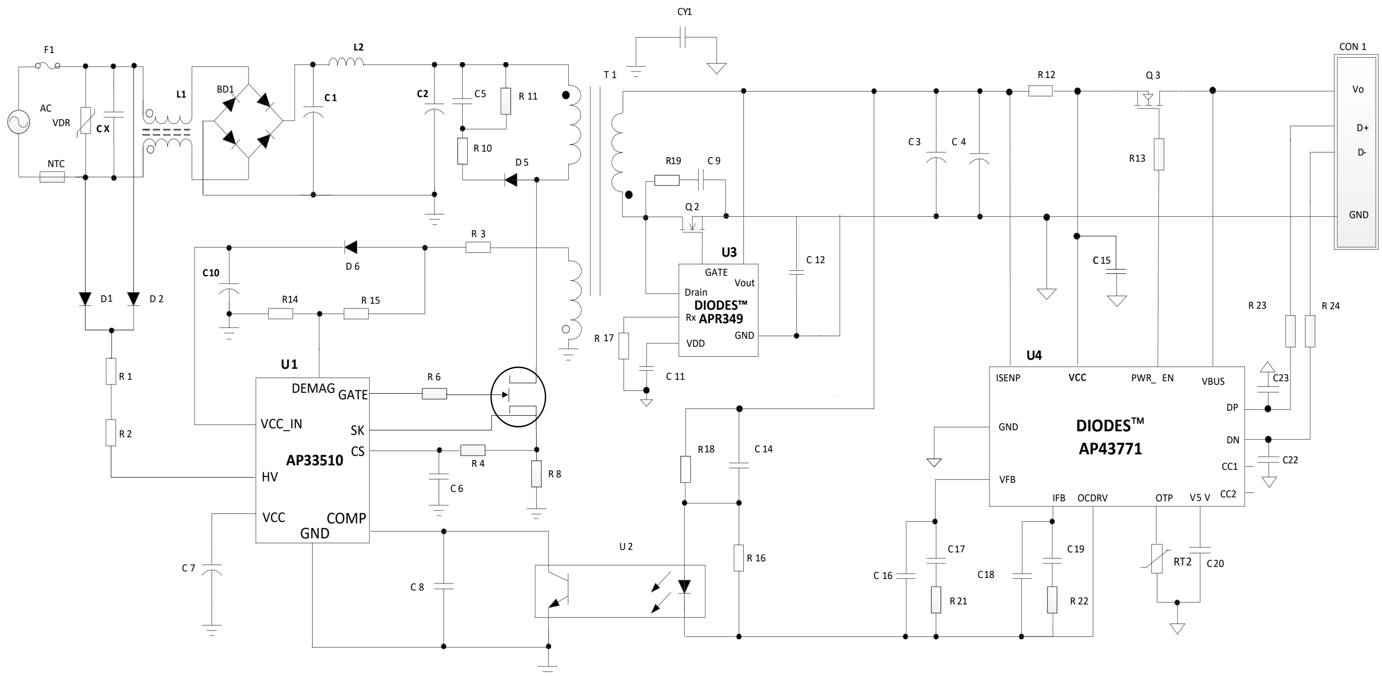
Typical Applications Circuit



Pin Descriptions

Pin Number	Pin Name	Function
1	VCC_IN	Wide range input supply voltage and built-in LDO to produce V_{CC}
2	VCC	Supply voltage of driver and control circuits
3	SK	Connected to GaN's Kelvin source
4	GATE	Gate driver output
5	GND	IC reference ground
6	CS	Primary current sense
7	DEMAG	Demagnetization input. Sense voltage from auxiliary winding
8	COMP	Feedback input. Directly connected to the Opto-coupler
9	HV	High voltage Input. Provide startup current to VCC

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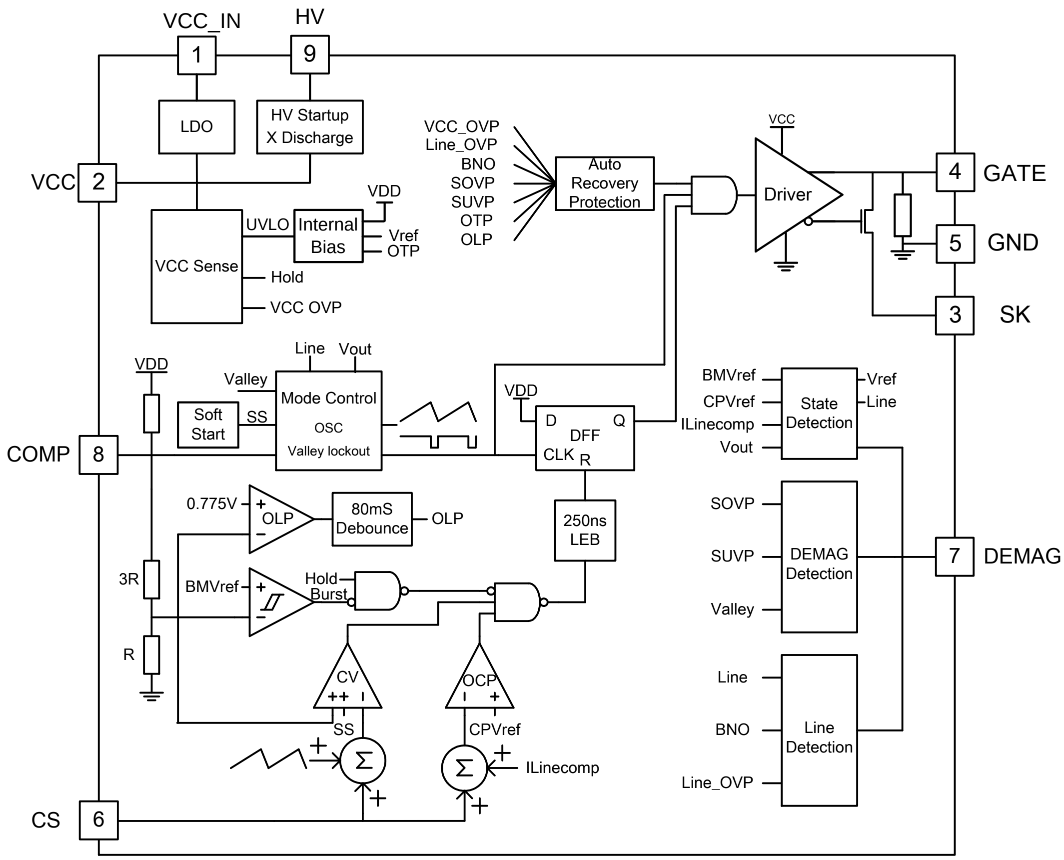
Functional Block Diagram



Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
V_{HV}	HV Pin Input Voltage (Note 5)	-0.3 to 600	V
V_{CC}	Power Supply Voltage	46	V
V_{CC_IN}	LDO Pin Input Voltage	150V	V
V_{COMP}, V_{CS}, V_{DEMAG}, V_{SK}	COMP, CS, DEMAG, SK Pin Input Voltage (Note 6)	-0.3 to 7	V
V_{GATE}	GATE Pin Voltage (Note 6)	-0.3 to 7	V
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 7)	143	°C/W
θ_{JC}	Thermal Resistance (Junction to Case) (Note 7)	10	°C/W
P_D	Power Dissipation at T_A < +25°C	500	mW
T_J	Operating Junction Temperature	-40 to +150	°C
T_{STG}	Maximum Storage Temperature	+150	°C
ESD	Human Body Model (Except HV Pin) (Note 8)	2,000	V
	Charge Device Model	650	V

Notes: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.
5. The drain-source voltage is 80% of V_{DS} in the aging condition.
6. If -0.3V to -0.5V negative voltage is applied to DEMAG/CS/GATE pins, the period of negative pulse is lower than 0.4μs.
7. Test condition: Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch^2 cooling area.
8. HV devices are ESD sensitive (HBM: V_{HV} = 1500V).

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Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	9	40	V
V_{CC_IN}	LDO Pin Input Voltage	—	120	V
T_A	Ambient Temperature	-40	+85	°C

Electrical Characteristics (@ T_A = -40°C to +85°C, V_{CC} = 18V, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Supply Voltage (VCC Pin)						
V_{CC_OVP}	VCC OVP Threshold Voltage	—	41.5	43.5	45.5	V
V_{CC_ON}	VCC On Threshold Voltage	—	16.5	18	19.5	V
V_{CC_UVLO}	VCC UVLO Threshold Voltage	—	6.2	6.7	7.2	V
V_{CC_ET}	VCC Holdup Mode Entry Point	—	7.0	7.5	8.0	V
V_{CC_EX}	VCC Holdup Mode Exit Point	—	—	V_{CC_ET} +0.5	—	V
I_{CC_ST}	Start-up Current	V_{CC} < V_{CC_ON}	—	1	10	µA
I_{CC_OP}	Operating Current	V_{COMP} = 0V, I_{DEMAG} = 0mA	150	300	600	µA
		V_{COMP} = 1.2V	0.7	1.1	1.5	mA
V_{CC}	LDO Regulated Voltage (Power Supply Voltage)	V_{CC} Open, V_{CC_IN} = 10V	8	9	—	V
		V_{CC} Open, V_{CC_IN} = 90V	13	14	15	V
I_{LDO}	Current Limit	V_{CC} = 12V, V_{CC_IN} = 40V	-10	-8.5	-7	mA
GATE Section (GATE Pin)						
V_{GATE_H}	GATE High Voltage	I_{SOURCE} = 10mA, V_{CC} = 7.5V	5	5.4	5.9	V
V_{GATE_L}	GATE Low Voltage	I_{SINK} = 20mA, V_{CC} = 10V	—	0.1	0.5	V
V_{GATE_CLAMP}	GATE Clamp Voltage	V_{CC} = 20V	5.5	6	6.3	V
$t_{GATE-RISE}$	Rising Time	C_L = 1nF	—	450	—	ns
$t_{GATE-FALL}$	Falling Time	C_L = 1nF	—	50	—	ns
Current Sense Section (CS Pin)						
V_{TH_OCP1}	Level 1 OCP Threshold Voltage	I_{DEMAG} = -280µA (Note 10)	0.62	0.65	0.68	V
V_{TH_OCP2}	Level 2 OCP Threshold Voltage	—	1	1.1	1.2	V
V_{TH_SSCP}	SSCP Voltage	—	—	50	65	mV
t_{LEB}	Leading Edge Blanking Time	—	150	250	350	ns
t_{D_OPP}	Overpower Protection Debounce Time	(Note 9)	—	80	—	ms
t_{PD}	Internal Propagation Delay Time	—	—	100	—	ns
Feedback Section (COMP Pin)						
V_{COMP_OP}	Open-Loop Voltage	COMP Pin Open-Circuited	3.2	3.6	3.9	V
V_{COMP_OLP}	OLP Threshold Voltage	—	3.0	3.1	3.2	V
R_{COMP}	Internal Pull-up Resistor	—	14	19	24	kΩ
$K_{COMP-CS}$	The Ratio of V_{COMP} to V_{CS}	—	3.5	4	4.5	V/V
V_{FOLD_ET}	Frequency Foldback Enter Voltage	V_{DEMAG} = 1.7V	—	1.05	—	V
V_{FOLD_EX}	Frequency Foldback Exit Voltage	V_{DEMAG} = 1.7V	—	0.55	—	V
V_{BURST_ENTRY}	Burst Mode Entry Voltage	I_{DEMAG} = -300µA, V_{DEMAG} = 1.1V	—	0.4	—-	V
		I_{DEMAG} = -600µA, V_{DEMAG} = 1.1V	—	0.333	—	V
		I_{DEMAG} = -300µA, V_{DEMAG} = 1.7V	—	0.567	—	V
		I_{DEMAG} = -600µA, V_{DEMAG} = 1.7V	—	0.533	—	V
V_{BURST_HYS}	Burst Mode Hysteresis Voltage	—	—	0.1	—	V

Notes: 9. Data measured in IC test mode.
10. Guaranteed by design.

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Electrical Characteristics (@ T_A = -40 to +85°C, V_{CC} = 18V, unless otherwise specified.) (continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Oscillator Section						
f_{SW_MAX}	Maximum Switching Frequency	V_{COMP} > 1.1V V_{DEMAG} = 1.1V	93	100	107	kHz
		V_{COMP} > 1.1V V_{DEMAG} = 1.7V	—	—	150	kHz
f_{SW_MIN}	Minimum Switching Frequency	—	20	25	30	kHz
t_{ONMAX}	Maximum T_{ON} for QR Mode	—	18	21	24	µs
DEMAG Section (DEMAG Pin)						
t_{BLK_DEMAG}	Blanking Time	—	—	1.5	—	µs
V_{TH_OVP}	V_{OUT} OVP Threshold Voltage	—	4	4.1	4.2	V
V_{TH_OUT}	V_{OUT} Threshold Voltage	—	1.3	1.4	1.5	V
$V_{TH\_OUT\_HYS}$	V_{OUT} Threshold Hysteresis Voltage	—	—	50	—	mV
V_{TH_UVP}	V_{OUT} UVP Threshold Voltage	—	0.45	0.48	0.51	V
t_{D_UVP}	Blanking Time of V_{OUT_UVP}	—	20	25	30	ms
V_{ZCD_DEMAG}	Zero Current Detection Threshold Voltage	(Note 9)	—	35	—	mV
t_{OUT}	Timeout After Last Zero Current Detection	Correlation with t_{BLK_DEMAG} (Note 10)	—	3	—	µs
$V_{CLP\text{-}L}$	Low Level for Clamping Voltage	I_{DEMAG} = -200µA	-150	-50	—	mV
$V_{CLP\text{-}H}$	High Level for Clamping Voltage	I_{DEMAG} = 1mA	4.5	5	—	V
I_{DEMAG_BNI}	Brown-In Protection Threshold Current	—	—	-226	—	µA
I_{DEMAG_BNO}	Brown-Out Protection Threshold Current	—	-227	-209	-191	µA
t_{D_BNO}	Debounce Time of Brown Out	(Note 10)	—	50	—	ms
$I_{DEMAG\text{-}HLSW}$	High/Low Line Switching Threshold Current	—	—	-452	—	µA
t_{D_HLSW}	Debounce Time of High Line to Low Line	(Note 10)	—	20	—	ms
I_{DEMAG_LHSW}	Low/High Line Switching Threshold Current	—	-534	-487	-440	µA
I_{DEMAG_OVP}	Bulk OVP Protection Threshold Current	—	-1336	-1218	-1100	µA
$t_{D\_BulkOVP}$	Delay Time of Bulk OVP	(Note 10)	—	2.8	—	s
I_{DEMAG_MAX}	Maximum DEMAG Sourcing Current	(Note 10)	-1500	—	—	µA
HV Section (HV Pin)						
I_{START}	Start Up Current Sourced from VCC Pin	V_{CC} = 6V, V_{HV} = 100V	1	2	—	mA
$I_{DISCH\text{-}X}$	X-CAP Discharge Current	—	2	3	4	mA
Internal OTP Section						
OTP	OTP Enter	(Note 10)	—	+155	—	°C
	OTP Exit	(Note 10)	—	+140	—	°C

Notes: 9. Data measured in IC test mode.
10. Guaranteed by design.

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Operation Description

The AP33510 is a quasi-mode flyback PWM controller for GaN FET. It covers a wide output range and has an optimized efficiency performance suitable for various output voltages and load conditions. Accounting for the needs of extremely low standby-power requirements, the controller includes an X capacitor discharge circuit that eliminates the need for external power-consuming resistors across the input X capacitors

Start-up Timing

A built-in HV start-up circuit in the AP33510 helps simplify the power system design for low standby applications. During the startup transient, the I_{START} current travels through an externally resistive network and HV pin to charge the VCC capacitor. When the VCC is charged to the startup voltage V_{CC_ON}, the current source turns off. The AP33510 will output four switching pulses to detect the I_{DEMAG} current flowing through the DEMAG pin pull-up resistor. Thus, the AC line voltage can be identified. If the input voltage is lower than the brown-in voltage, the IC will enter into restart status. Once the input voltage is higher than the brown-in voltage, the AP33510 will start working and output voltage will ramp up. The auxiliary winding voltage also goes up accordingly. The V_{CC} voltage begins going down from V_{CC_ON} until VCC capacitor charging is taken over by the auxiliary winding voltage.

Operation Mode for High Efficiency

The AP33510 optimizes system efficiency by switching in the valley of the MOSFET drain-source voltage under QR (quasi-resonance) mode with heavy load. When output load decreases, the switching frequency will operate in PFM mode with valley-on switching. The selected valley for turning on is locked until the load changes to the next level. As feedback level continues to decrease, the system will skip more valleys to implement frequency reducing. In this way, higher efficiency can be achieved by reducing switching power loss. In order to avoid an excessive switching loss at very high switching-frequency operations, there is a fixed 150 kHz frequency limitation.

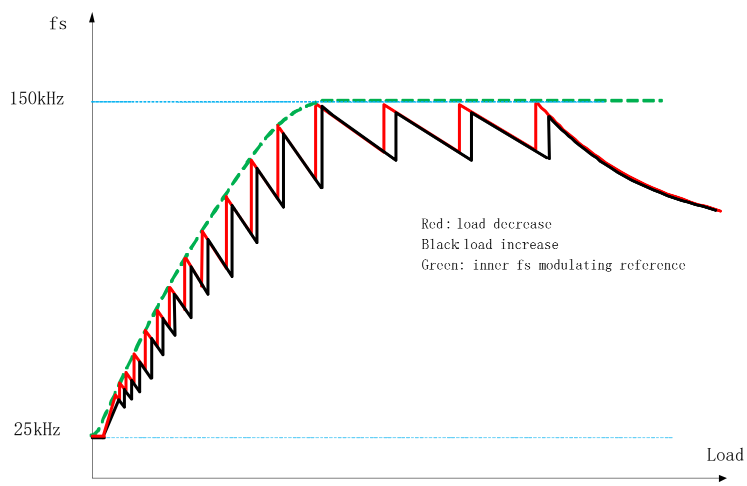

Figure 1. QR Operation Frequency Curve

For valley-on switching, the AP33510 has a built-in internal voltage reference to compare with V_{COMP}. It adjusts the valley number for turn-on, as shown in Figure 1. When the COMP voltage decreases according to an inner modulating reference, the first “valley-on status” is forced to shift to another available “valley-on status”. The maximum valley number for turn-on is the fifteenth. When the valley quantities exceed fifteen, the system will operate at low-frequency hard-switching conditions. A minimum clamp frequency will prevent the switching frequency from dropping below 25kHz to eliminate risk of audible noise.

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Operation Description (continued)

Valley-Switch & Valley-Lock

Quasi-resonant operation is regarded as a soft-switching technology which always turns on the primary GaN FET at the valley status of the Drain-to-Source voltage (V_{DS}). Compared to traditional hard switching, QR switching-on can reduce switching power loss of the GaN FET and achieve good EMI behavior with no additional BOM cost.

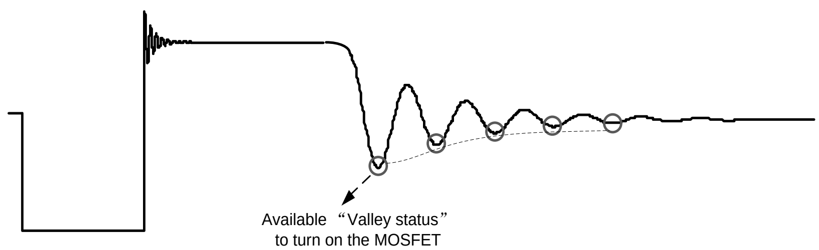

Figure 2. Valley Detection

Figure 2 shows the primary GaN FET V_{DS} waveform. When the secondary-side current flows to zero, the primary inductance L_M and the effective GaN FET output capacitor C_{OSS} begin to resonate. The resonant frequency is approximately $1/2\pi\sqrt{L_M * Coss}$. A QR flyback controller takes advantage of the drain voltage ringing and turns on the power switch at the drain ringing voltage valley to reduce switching loss and EMI. The valley is detected by the DEMAG pin through a pair of voltage dividers. At the primary GaN FET turning-off time and once the voltage on the DEMAG pin is detected below 35mV, one "valley status" is counted. Each "valley status" of the GaN FET V_{DS} will be detected and counted by the DEMAG pin. According to the AP33510's frequency control strategy, one proper "valley status" will be selected to turn on the GaN FET. To prevent a false-trigger of the V_{DS} ring caused by a leakage inductance, the valley-detection function is blanked within the t_{BLK_DEMAG} when the primary GaN FET turns off.

In general, when the turning-on valley changes, the frequency will change. However, if the turning-on position changes back and forth between two neighboring valleys, which causes the frequency to change too fast, this unstable condition will introduce unacceptable audible noise. Through "valley-lock" technology, the turning-on valley is locked and will not switch iteratively when the load is changed.

Frequency Dithering

To improve the EMI performance in valley-lock mode, the AP33510 varies the valley switching moment during the negative half-cycle, and the switching frequency will have a periodic excursion as a triangular wave. As shown in Figure 3, this frequency jittering method helps to spread out energy in a conducted noise frequency domain, and meets stringent EMI requirement. For low-power or middle-power level conditions, the dithering circuit persists in working in frequency-foldback mode because of an innovative implementation of AP33510.

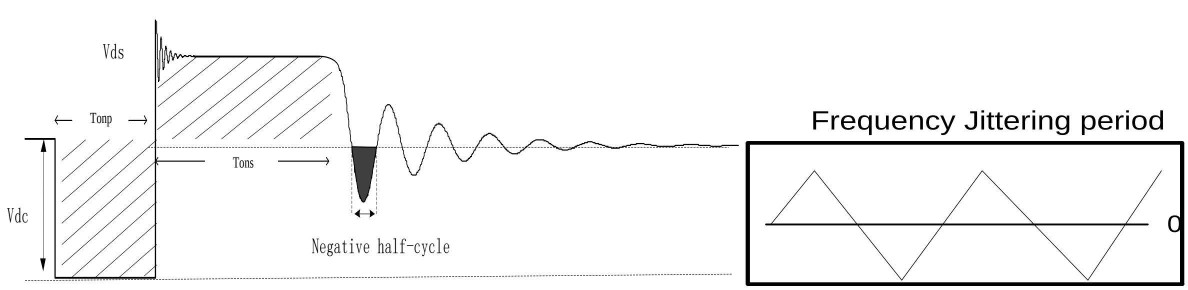

Figure 3. Frequency Dithering

Kelvin Source Connection

The GaN device has lower input capacitance, a lower gate turn-on threshold, and faster switching speeds than silicon MOSFETs—which reduces switching loss but also brings a new challenge to the gate driver as the loop area must be minimized to reduce noise coupling. In addition, the Kelvin connection for the gate driver is necessary to prevent false triggering due to external parasitic inductance from the ground current-sensing resistor.

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Operation Description (continued)

Line Compensation

Pertaining to the general power-supply system at high-line voltage, a higher OCP current with turn-off time delay often occurs in power switching. The AP33510 implements a proprietary line-compensation scheme to add to the offset voltage on the CS pin. This compensation is able to obtain a relative constant OCP current value with universal input voltage.

Built-in V_{CC} LDO

The AP33510 integrates V_{CC} LDO circuitry. The LDO regulates the wide range V_{CC_IN}, which is rectified from auxiliary winding to an acceptable value. This makes the AP33510 a good choice in wide range output voltage applications.

X-CAP Discharge Function

To attenuate differential-mode noise in higher-power applications, an X-CAP is usually used before the rectifier bridge. When the AC line is off, paralleled resistors discharge the X-CAP for safety considerations. These paralleled resistors have large power dissipation and will increase standby power. The AP33510 integrates an X-CAP discharge function to replace the discharge resistors and thus decrease standby power.

This function contains two processes; the first process detects the condition of the AC line through the HV pin. This detected voltage is named V_b. When the system is plugged in, an inner timer of 60ms within the AP33510 begins to work. Meanwhile, a phase-drifted and filtered V_c signal is generated based on V_b and both are compared, as shown in Figure 4.

Whenever signal V_c crosses over with signal V_b, the inner 60ms timer will reset—which represents that the AC line is on. If the system is disconnected from the AC line, the cross-over signal of V_c and V_b will disappear and the 60ms timer will continue to count until it reaches 60ms. Here, the second process (discharge process) will come into effect and a 3mA discharge current will flow through the HV pin to GND, lasting for 60ms. After the AC line is off, the first process and the second process will alternate until the HV pin voltage is discharged below 10V, even when the V_{CC} voltage is lower than $V_{CC\text{-}UVLO}$.

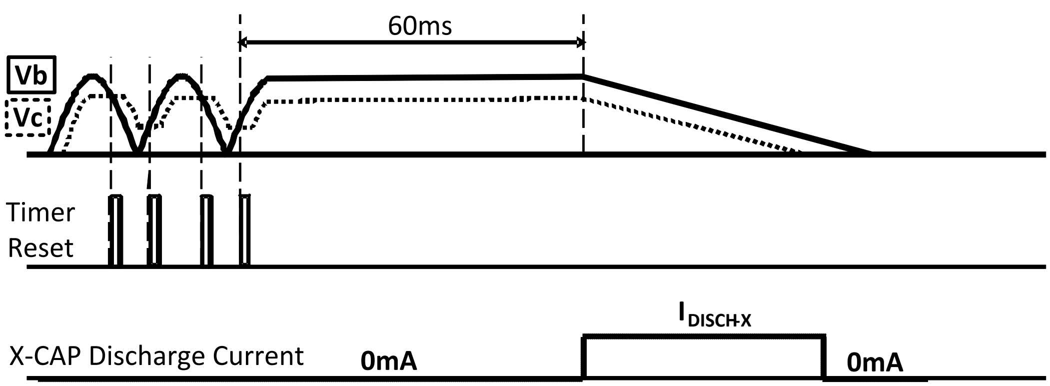

Figure 4. X-CAP Discharge principle

Overpower Protection

An integrated overpower protection circuit provides a relatively constant power limit across different line voltages. The negative voltage of the DEMAG pin can reflect the input voltage, and thus the overpower compensation circuit measures the input voltage via the DEMAG pin. When the output power reaches the OPP limit, the corresponding V_{CS} should touch the overpower reference voltage. When the overpower condition lasts continuously for 80ms, overpower protection is triggered and the switching pulse is disabled. The system will enter into restart mode.

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Operation Description (continued)

VOUT OVP & UVP

The AP33510 provides output OVP and UVP protection functions. The auxiliary winding voltage during secondary rectifier conducting period reflects the output voltage. A divided voltage network is connected to the auxiliary winding and DEMAG pin. The DEMAG pin will detect the equivalent output voltage with a delay of t_{BLK_DEMAG} from the falling edge of the GATE driver signal, as shown in Figure 5. The detected voltage will be compared to the inner SOVP and SUVP threshold voltage. If the SOVP or SUVP threshold is reached continuously by six switching cycles, SOVP or SUVP protection will be triggered, the AP33510 will shut down switching pulses, and the system will restart when the V_{CC} voltage falls below the UVLO voltage.

To prevent a false-trigger of the SUVP during the start-up process, SUVP protection function will be ignored for a blank time of t_{D_UVP}.

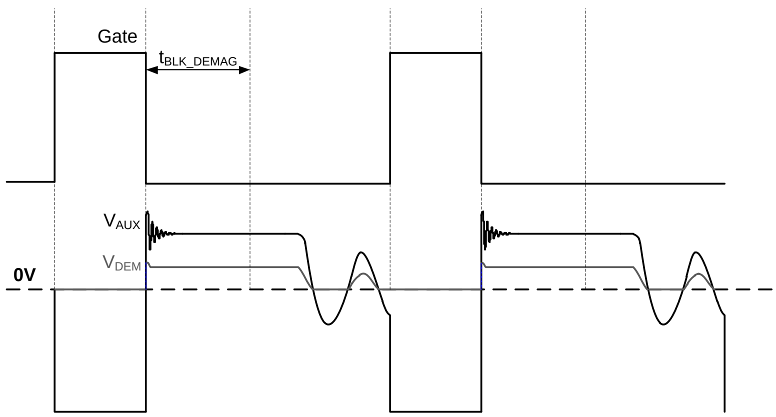

Figure 5. SOVP and SUVP

Overtemperature Protection

The AP33510 integrates internal temperature protection to prevent permanent damage by overtemperature. If the junction temperature exceeds the temperature-protection threshold of +155°C, the IC will trigger the internal OTP and stop switching. Meanwhile, if the VCC drops to the VCC UVLO threshold V_{CC_UVLO}, the controller enters restart mode. A built-in hysteresis ensures that if the internal temperature drops to +140°C, the IC will recover operation.

The controller also can implement external accurate overtemperature protection through pin multiplexing. This is done by connecting an NTC resistor to provide temperature detection.

Other System Protection

V_{BULK_OVP}, FOCP, SSCP, VCC OVP, SCP

The AP33510 provides versatile protections to ensure the reliability of the power system. V_{BULK_OVP} represents line-voltage overvoltage protection. If the detected AC line voltage is higher than V_{BULK_OVP} and sustains for 2.8s, the V_{BULK_OVP} protection will be triggered.

FOCP (fast overcurrent protection) is an ultra-fast short-current protection that helps to avoid catastrophic damage of the system when the secondary rectifier is shorted. The primary peak current will be monitored by the CS pin through a primary sense resistor. Whenever the sampled voltage reaches the threshold of $V_{TH\text{-}FOCP}$ for six switching cycles continuously, the FOCP will be activated to shut down the switching pulse.

SSCP (sensor short-circuit protection) may be triggered when the CS pin is shorted to the ground. The SSCP module senses the voltage across the primary sense resistor with a several microsecond delay time after the rising edge of the primary GATE signal. This sensed signal is compared with $V_{TH\text{-}SSCP}$. If it is lower than $V_{TH\text{-}SSCP}$ for six switching cycles, the SSCP will be triggered and the drive signal will be disabled. To prevent a false-trigger, the SSCP is valid only within the initial 25ms after startup.

VCC overvoltage protection is used to prevent IC damage from overvoltage stress. All these protections described will restart the system when the V_{CC} voltage falls below UVLO.

If the power supply experiences a severe overloading situation or the output of the system is under a short-circuit protection (SCP) test, the driving pulses will stop and V_{CC} will fall down as the auxiliary pulses are missing. When V_{CC} drops below V_{CC_UVLO}, the controller consumption is down to a few µA and V_{CC} slowly rises up again via resistive starting network. When V_{CC} reaches up to V_{CC_ON}, the controller purposely ignores the restart cycle and waits for another VCC cycle. The AP33510 naturally reaches a remarkable low input power by lowering the duty ratio in fault conditions.

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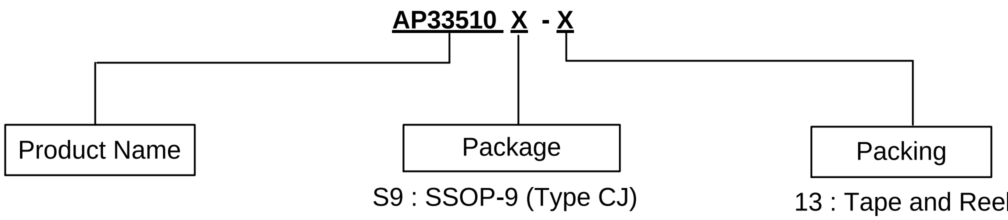
Ordering Information

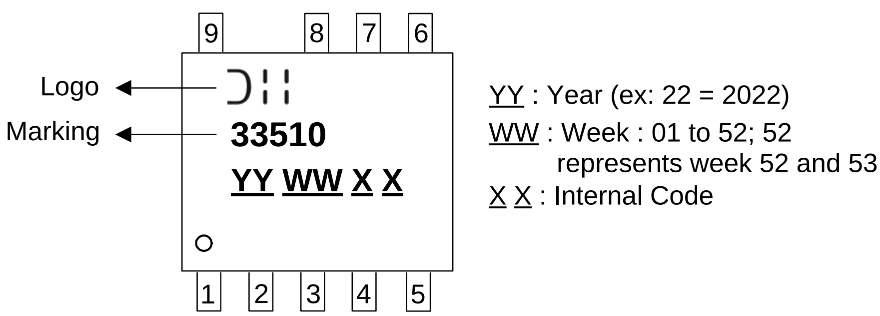


Part Number	Package	Marking	Packing	
			Qty.	Carrier
AP33510S9-13	SSOP-9 (Type CJ)	33510	4,000	Tape and Reel

Marking Information

SSOP-9 (Type CJ)

(Top View)



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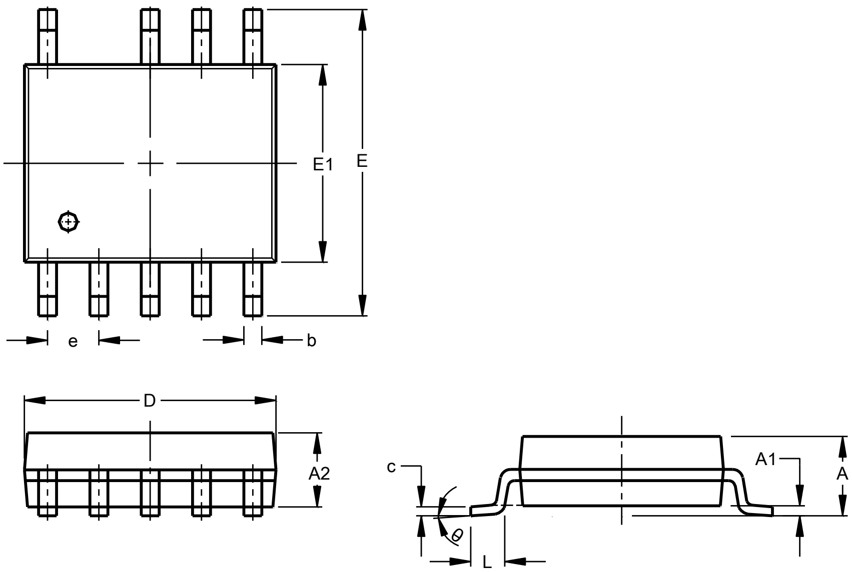
Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SSOP-9 (Type CJ)

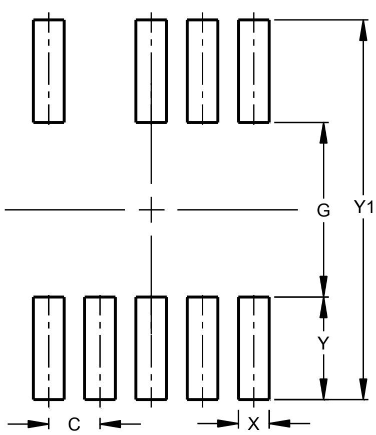


SSOP-9 (Type CJ)			
Dim	**Min**	**Max**	**Typ**
A	1.35	1.75	--
A1	0.10	0.25	--
A2	1.350	1.550	--
b	0.270	0.430	--
c	0.170	0.258	--
D	4.70	5.10	--
E	5.80	6.20	--
E1	3.80	4.00	--
e	--	--	1.00
L	0.40	1.27	--
θ	0°	8°	--
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SSOP-9 (Type CJ)



Dimensions	Value (in mm)
C	1.00
G	3.40
X	0.60
Y	2.00
Y1	7.40

Mechanical Data

- Moisture Sensitivity: Level 3 per JESD22-A113
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 e3
- Weight: 0.08 grams (Approximate)

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