

Si8921/22 Data Sheet

Isolated Amplifier for Current Shunt Measurement

The Si8921/22 is a galvanically isolated analog amplifier. The low-voltage differential input is ideal for measuring voltage across a current shunt resistor or for any place where a sensor must be isolated from the control system. The output is a differential analog signal amplified by either 8.2x or 32.8x.

The very low signal delay of the Si8921/22 allows control systems to respond quickly to fault conditions or changes in load. Low offset and gain drift ensure that accuracy is maintained over the entire operating temperature range. Exceptionally high common-mode transient immunity means that the Si8921/22 delivers accurate measurements even in the presence of high-power switching as is found in motor drive systems and inverters.

The Si8921/22 isolated amplifier utilizes Skyworks' proprietary isolation technology. It supports up to 5.0 kVrms withstand voltage per UL1577. This technology enables higher performance, reduced variation with temperature and age, tighter part-to-part matching, and longer lifetimes compared to other isolation technologies.

Applications:

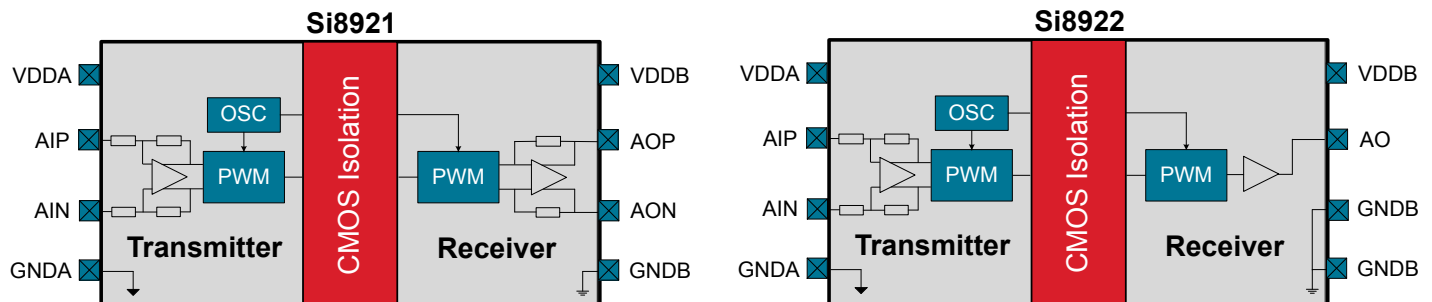
- Industrial, HEV, and renewable energy inverters
- AC, Brushless, and DC motor controls and drives
- Variable speed motor control in consumer white goods
- Isolated switch mode and UPS power supplies
- Automotive on-board chargers, battery management systems, and charging stations

Safety Approvals

- UL 1577 recognized
 - Up to 5000 Vrms for 1 minute
- CSA approval
 - IEC 62368-1 (reinforced insulation)
- VDE certification conformity
 - EN62368-1 (reinforced insulation)
 - Pending IEC60747-17 (basic/reinforced insulation)
- CQC certification approval
 - GB4943.1-2011

KEY FEATURES

- Low-voltage differential input:
 - ± 62.5 mV and ± 250 mV options
- Low signal delay: 0.8 μ s
- Typical input offset: ± 40 μ V
- Typical gain error: $\pm 0.06\%$
- Excellent drift specifications:
 - ± 0.5 μ V/ $^{\circ}$ C typical offset drift
 - -9 ppm/ $^{\circ}$ C typical gain drift
- Typical Nonlinearity: 0.003% full-scale
- Typical SNR: 82 dB over 100 kHz bandwidth
- Typical THD: -88 dB
- High common-mode transient immunity: 75 kV/ μ s
- Automotive-grade OPNs:
 - AIAG compliant PPAP documentation support
 - IMDS and CAMDS listing support
- Compact packages:
 - 8-pin wide body stretched SOIC
 - 8-pin narrow body SOIC
- -40 to 125 $^{\circ}$ C



1. Ordering Guide

| Ordering Part Number ^{1, 2, 3} | Automotive Ordering Part Number ^{1, 2, 3, 4} | Ordering Options | | | |
|---|---|-----------------------|------------------|--------------|---------------------|
| | | Specified Input Range | Isolation Rating | Output | Package Type |
| Si8921AD-IS4 | Si8921AD-AS4 | ±62.5 mV | 5.0 kVrms | Differential | WB Stretched SOIC-8 |
| Si8921BD-IS4 | Si8921BD-AS4 | ±250 mV | 5.0 kVrms | Differential | WB Stretched SOIC-8 |
| Si8921AB-IS | Si8921AB-AS | ±62.5 mV | 2.5 kVrms | Differential | NB SOIC-8 |
| Si8921BB-IS | Si8921BB-AS | ±250 mV | 2.5 kVrms | Differential | NB SOIC-8 |
| Si8922AD-IS4 | Si8922AD-AS4 | 8 to 62.5 mV | 5.0 kVrms | Single-ended | WB Stretched SOIC-8 |
| Si8922BD-IS4 | Si8922BD-AS4 | 30 to 250 mV | 5.0 kVrms | Single-ended | WB Stretched SOIC-8 |
| Si8922AB-IS | Si8922AB-AS | 8 to 62.5 mV | 2.5 kVrms | Single-ended | NB SOIC-8 |
| Si8922BB-IS | Si8922BB-AS | 30 to 250 mV | 2.5 kVrms | Single-ended | NB SOIC-8 |

Note:

1. All packages are RoHS-compliant.
2. "Si" and "SI" are used interchangeably.
3. AEC-Q100 pending qualification.
4. Automotive-Grade devices ("-A" suffix) are identical in construction materials, topside marking, and electrical parameters to their Industrial Grade ("-I suffix") version counterparts. Automotive-Grade products are produced utilizing full automotive process flows and additional statistical process controls throughout the manufacturing flow. The Automotive-Grade part number is included on shipping labels.

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2. System Overview

The input to the Si8921/22 is designed for low-voltage, differential signals. This is ideal for connection to low resistance current shunt measurement resistors. The Si8921A has a specified full scale input range of ± 62.5 mV, and the Si8921B has a specified full scale input range of ± 250 mV. In both cases, the internal gain is set so that the full scale output is 2.05 V. The Si8921 provides a differential output voltage while the Si8922 provides a single-ended output voltage.

The Si8921/22 modulates the analog signal in a unique way for transmission across the semiconductor based isolation barrier. The input signal is first converted to a pulse-width modulated digital signal. On the other side of the isolation barrier, the signal is demodulated. The resulting PWM signal is then used to faithfully reproduce the analog signal. This solution provides exceptional signal bandwidth and accuracy.

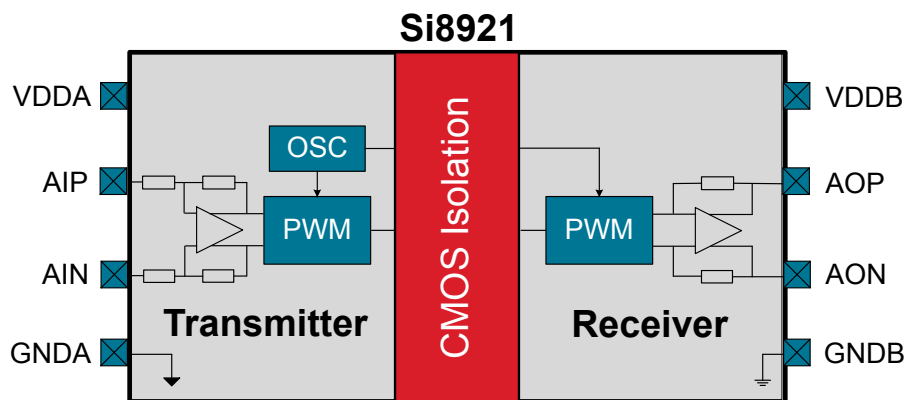


Figure 2.1. Si8921 Functional Block Diagram

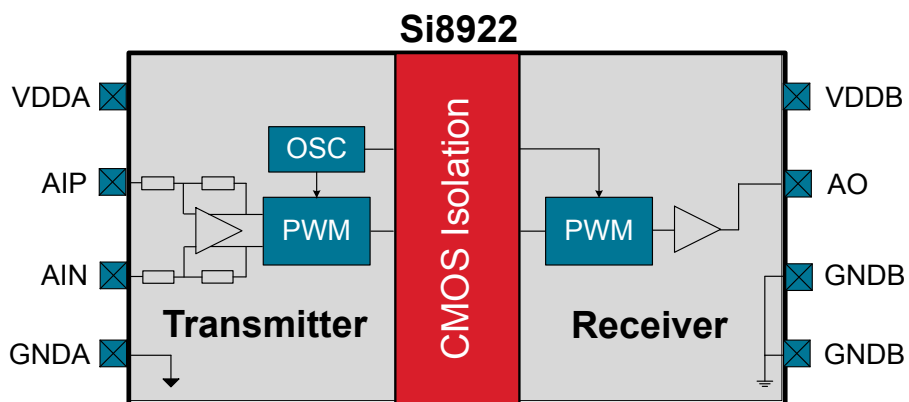


Figure 2.2. Si8922 Functional Block Diagram

2.1 Fail-Safe and Low-Power Modes

The Si8921/22 implements a fail-safe output when the high-side supply voltage VDDA goes away. This is important for safe operation in systems with high safety requirements. The fail-safe output is nominally 2.8 V (Si8922) or -2.8 V (Si8921) which can be differentiated from the maximum clipping output voltage of 2.6 V to simplify diagnostics on the system level.

| Device | Output Voltage (VDDA Normal) | Output Voltage (VDDA Removed) |
|--------|------------------------------|-------------------------------|
| Si8921 | $\sim \pm 2.6$ V | ~ -2.8 V |
| Si8922 | 0 to ~ 2.6 V | $\sim +2.8$ V |

In addition to the fail-safe output, when a loss of VDDA supply occurs, the part will automatically move into a lower power mode that reduces IDDB current to approximately 1 mA. Similarly, a loss of VDD B supply will reduce IDDA current to approximately 1 mA. When the supply voltage is returned, normal operation begins in approximately 250 μ s.

3. Current Sense Application

In the driver circuit presented below, the Si8921 is used to amplify the voltage across the sense resistor, RSENSE, and transmit the analog signal to the low-voltage domain across an isolation barrier. Isolation is needed because the voltage of RSENSE with respect to ground will swing between 0 V and the high voltage rail connected to the drain of Q1.

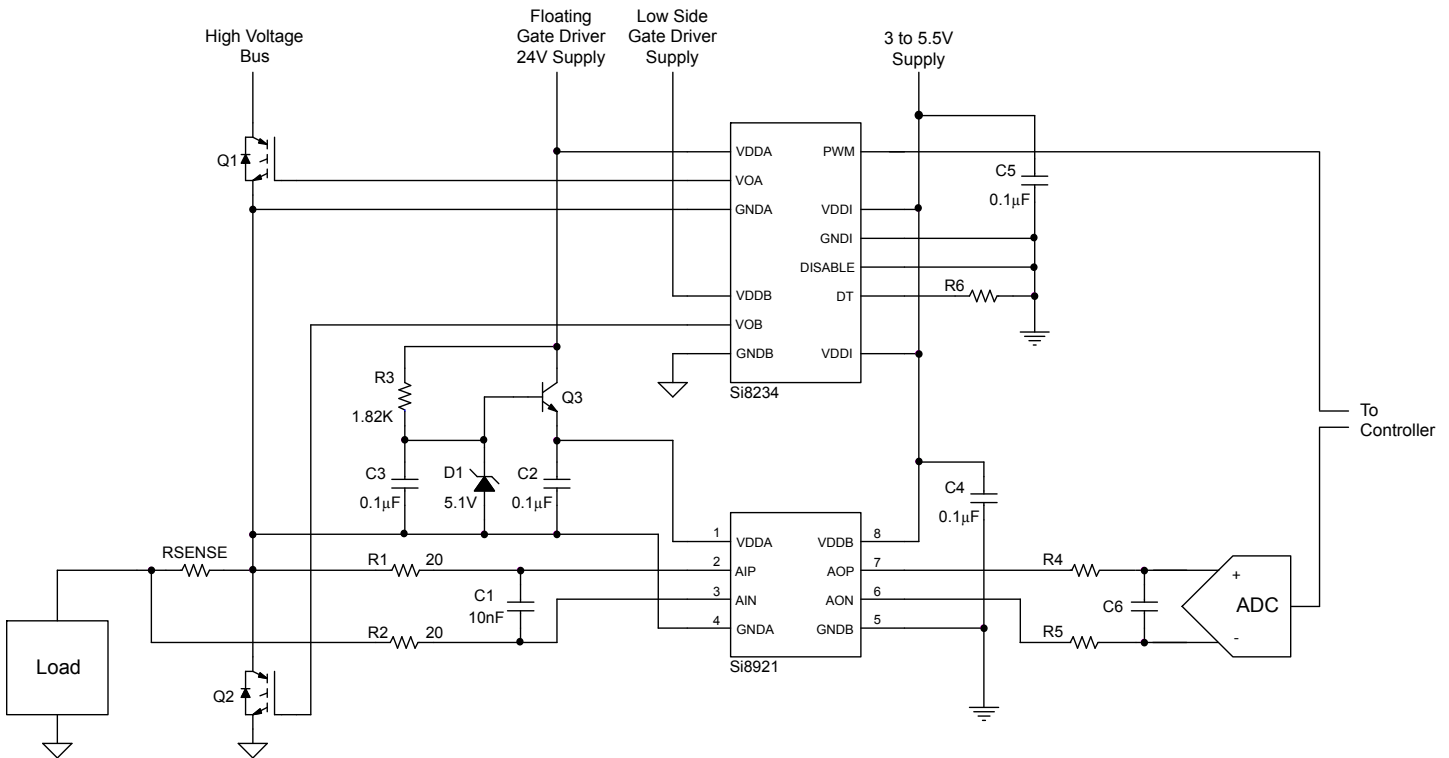


Figure 3.1. Current Sense Application

The load in this application can be a motor winding or a similar inductive winding. In a three-phase motor drive application, this circuit would be repeated three times, one for each phase. RSENSE should be a small resistor value to reduce power loss. However, an excessively low resistance will reduce the signal-to-noise ratio of the measurement. Si8921/22 offers two specified full-scale input options, ± 62.5 mV (Si8921A/22A) and ± 250 mV (Si8921B/22B), for optimizing the value of RSENSE.

AIP and AIN connections to the RSENSE resistor should be made as close as possible to each end of the RSENSE resistor as trace resistance will add error to the measurement. The input to the Si8921/22 is differential, and the PCB traces back to the input pins should run in parallel. This ensures that any large noise transients that occur on the high-voltage side are coupled equally to the AIP and AIN pins and will be rejected by the Si8921/22 as a common-mode signal.

The amplifier bandwidth of the Si8921/22 is approximately 600 kHz. If further input filtering is required, a passive, differential RC low-pass filter can be placed between RSENSE and the input pins. Values of $R1 = R2 = 20 \Omega$ and $C1 = 10$ nF, as shown in [Figure 3.1 Current Sense Application on page 5](#), provides a cutoff at approximately 400 kHz. For the lowest gain error, R1 and R2 should always be less than 33Ω to keep the source impedance sufficiently low compared to the Si8921/22 input impedance.

The common-mode voltage of AIN and AIP must be greater than -0.2 V but less than 1 V with respect to GNDA. To meet this requirement, connect GNDA of the Si8921/22 to one side of the RSENSE resistor. In this example, GNDA, RSENSE, the source of Q1, and the drain of Q2 are connected. The ground of the gate driver (Skyworks' Si8234 in this circuit) is also commonly connected to the same node.

The Q1 gate driver has a floating supply, 24 V in this example. Since the input and output of the Si8921/22 are galvanically isolated from each other, separate power supplies are necessary on each side. Q3, R3, C3, and D1 make a regulator circuit for powering the input side of the Si8921/22 from this floating supply. D1 establishes a voltage of 5.6 V at the base of Q3. R3 is selected to provide a Zener current of 10 mA for D1. C3 provides filtering at the base of Q3, and the emitter output of Q3 provides approximately 5 V to VDDA. C2 is a bypass capacitor for the supply and should be placed at the VDDA pin with its return trace connecting to the GNDA connection at RSENSE.

C4, the local bypass capacitor for the B-side of Si8921/22, should be placed close to VDDB supply pin with its return close to GNDB. The output signal at AOP and AON is differential with a nominal gain of 8.2 (Si8921B) or 34.8 (Si8921A) and common mode of 1.4 V. The outputs are sampled by a differential input ADC. Depending on the sample rate of the ADC, an anti-aliasing filter may be required. A simple anti-aliasing filter can be made from the passive components, R4, C6, and R5. The characteristics of this filter are dictated by the input topology and sampling frequency of the ADC. However, to ensure the Si8921 outputs are not overloaded, $R4 = R5 > 5 \text{ k}\Omega$ and C6 can be calculated by the following equation:

$$C6 = \frac{1}{2 \times \pi \times (R4 + R5) \times f_{3dB}}$$

For the Si8922, Pin 6 and C6 are both grounded, and R5 is removed.

4. Electrical Specifications

Table 4.1. Electrical Specifications
 $T_A = -40$ to $+125$ °C, $A_{IN} = G_{NDA}$; typical specs at 25 °C with $V_{DDA} = V_{DDB} = 5$ V unless specified differently under Test Condition

| Parameter | | Symbol | Test Condition | Min | Typ | Max | Units |
|---------------------------------------|-------------|-------------------|--------------------------------------|-------|-------|------|--------|
| Input Side Supply Voltage | | VDDA | | 3.0 | | 5.5 | V |
| Input Supply Current | Si8921A/21B | IDDA | $V_{DDA} = 3.3$ V | 3.3 | 4.6 | 6 | mA |
| | Si8922A/22B | IDDA | $V_{DDA} = 3.3$ V | 2.1 | 4.5 | 6.1 | mA |
| Output Side Supply Voltage | | VDDB | | 3.0 | | 5.5 | V |
| Output Supply Current | Si8921A/21B | IDDB | $V_{DDB} = 3.3$ V | 2.6 | 3.5 | 4.5 | mA |
| | Si8922A/22B | IDDB | $V_{DDB} = 3.3$ V | 2.0 | 4.3 | 5.6 | mA |
| Amplifier Bandwidth | | | | | 600 | | kHz |
| Amplifier Input | | | | | | | |
| Specified Linear Input Range | Si8921A | VAIP – VAIN | | -62.5 | | 62.5 | mV |
| | Si8921B | | | -250 | | 250 | mV |
| | Si8922A | VAIP – VAIN | | 8 | | 62.5 | mV |
| | Si8922B | | | 30 | | 250 | mV |
| Maximum Input Voltage Before Clipping | Si8921A | VAIP – VAIN | | | ±77 | | mV |
| | Si8921B | | | | ±310 | | mV |
| | Si8922A | | | 0 | 77 | | mV |
| | Si8922B | | | 0 | 310 | | mV |
| Common-Mode Operating Range | | VCM | $A_{IN} \neq G_{NDA}$ | -0.2 | | 1 | V |
| Input Referred Offset | Si8921A/21B | VOS | $T_A = 25$ °C, $A_{IP} = A_{IN} = 0$ | -0.15 | ±0.04 | 0.15 | mV |
| | Si8922A/22B | VOS | $T_A = 25$ °C, $A_O = 0.25$ V | -0.35 | ±0.07 | 0.35 | mV |
| Input Offset Drift | | VOS_T | | -0.3 | 0.5 | 3 | μV/°C |
| Differential Input impedance | Si8921A/22A | RIN | | | 6.3 | | kΩ |
| | Si8921B/22B | | | | 21.4 | | kΩ |
| Differential Input Impedance Drift | | RIN_T | | | 850 | | ppm/°C |
| Amplifier Output | | | | | | | |
| Full-Scale Output | | VAOP – VAON | | | 2.5 | | Vpk |
| Gain | Si8921A/22A | | | | 32.8 | | |
| | Si8921B/22B | | | | 8.2 | | |
| Gain Error | | | $T_A = 25$ °C | -0.2 | ±0.06 | 0.2 | % |
| Gain Error Drift | | | | -24 | -9 | 0 | ppm/°C |
| Output Common Mode Voltage (Si8921) | | $(VAOP + VAON)/2$ | | 1.34 | 1.39 | 1.49 | V |

| Parameter | | Symbol | Test Condition | Min | Typ | Max | Units |
|---|---------|---------------|---|-------|-------|------|-----------------------|
| Nonlinearity | Si8921A | | $T_A = 25\text{ }^\circ\text{C}$ | -0.04 | 0.01 | 0.04 | % |
| | Si8921B | | $T_A = 25\text{ }^\circ\text{C}$ | -0.02 | 0.003 | 0.02 | % |
| | Si8922A | | $T_A = 25\text{ }^\circ\text{C}$ | -0.08 | 0.02 | 0.08 | % |
| | Si8922B | | $T_A = 25\text{ }^\circ\text{C}$ | -0.04 | 0.01 | 0.04 | % |
| Nonlinearity Drift | | | | -16 | | 16 | ppm/ $^\circ\text{C}$ |
| Signal-to-Noise Ratio | Si8921A | SNR | $F_{IN} = 10\text{ kHz, BW} = 100\text{ kHz}$ | 70 | 77 | | dB |
| | Si8921B | | | 75 | 82 | | dB |
| | Si8922A | | | 64 | 71 | | dB |
| | Si8922B | | | 69 | 76 | | dB |
| Signal-to-Noise Ratio | Si8921A | SNR | $F_{IN} = 1\text{ kHz, BW} = 10\text{ kHz}$ | | 86 | | dB |
| | Si8921B | | | | 91 | | dB |
| | Si8922A | | | | 79 | | dB |
| | Si8922B | | | | 83 | | dB |
| Total Harmonic Distortion | Si8921A | THD | $F_{IN} = 1\text{ kHz}$ | | -85 | -74 | dB |
| | Si8921B | THD | $F_{IN} = 1\text{ kHz}$ | | -88 | -77 | dB |
| | Si8922A | THD | $F_{IN} = 1\text{ kHz}$ | | -82 | -63 | dB |
| | Si8922B | THD | $F_{IN} = 1\text{ kHz}$ | | -85 | -66 | dB |
| Power-Supply Rejection Ratio | | PSRR | VDDA at DC | | -100 | | dB |
| | | | VDDA at 100 mV and 10 kHz ripple | | -100 | | dB |
| | | | VDDB at DC | | -100 | | dB |
| | | | VDDB at 100 mV and 10 kHz ripple | | -100 | | dB |
| Output Resistive Load | Si8921 | RLOAD | Between AON and AOP | 5 | | | k Ω |
| | Si8922 | | Between AO and GND | 5 | | | k Ω |
| Output Capacitive Load | | CLOAD | Each pin to ground | | | 100 | pF |
| Timing | | | | | | | |
| Signal Delay (Si8921) | | t_{PD} | 50% to 50% | | 0.8 | | μs |
| Signal Delay (Si8922) | | t_{PD} | 50% to 50% | | 1 | | μs |
| Rise Time | | t_R | 10% to 90% | | 0.8 | | μs |
| Startup Time | | $t_{STARTUP}$ | | | 250 | | μs |
| Common-Mode Transient Immunity ¹ | | CMTI | AIP = AIN = AGND, VCM = 1500 V | 50 | 75 | | kV/ μs |
| Note: | | | | | | | |
| 1. An analog CMTI failure is defined as an output error of more than 100 mV persisting for at least 1 μs . | | | | | | | |

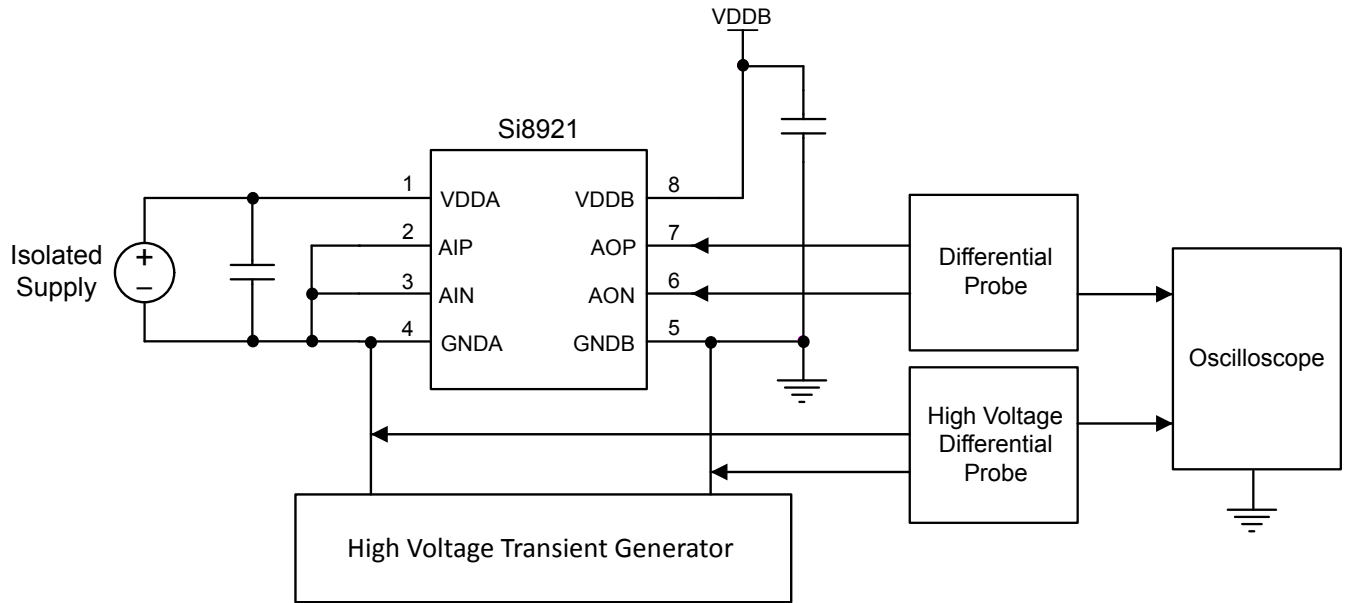


Figure 4.1. Common-Mode Transient Immunity Characterization Circuit

Table 4.2. IEC 60747-17 Safety Limiting Values¹

| Parameter | Symbol | Test Condition | Characteristic | Unit |
|---|--------|---|----------------|------|
| Safety Temperature | T_S | | 150 | °C |
| Safety Input Current (WB Stretched SOIC-8) | I_S | $\theta_{JA} = 90 \text{ }^\circ\text{C/W}$ $V_{DD} = 5.5 \text{ V}$ $T_J = 150 \text{ }^\circ\text{C}$ $T_A = 25 \text{ }^\circ\text{C}$ | 253 | mA |
| | | $\theta_{JA} = 90 \text{ }^\circ\text{C/W}$ $V_{DD} = 3.6 \text{ V}$ $T_J = 150 \text{ }^\circ\text{C}$ $T_A = 25 \text{ }^\circ\text{C}$ | 386 | mA |
| Safety Input Current (NB SOIC-8) | I_S | $\theta_{JA} = 112 \text{ }^\circ\text{C/W}$ $V_{DD} = 5.5 \text{ V}$ $T_J = 150 \text{ }^\circ\text{C}$ $T_A = 25 \text{ }^\circ\text{C}$ | 203 | mA |
| | | $\theta_{JA} = 112 \text{ }^\circ\text{C/W}$ $V_{DD} = 3.6 \text{ V}$ $T_J = 150 \text{ }^\circ\text{C}$ $T_A = 25 \text{ }^\circ\text{C}$ | 310 | mA |
| Safety Input Power (WB Stretched SOIC-8) | P_S | $\theta_{JA} = 90 \text{ }^\circ\text{C/W}$ $T_J = 150 \text{ }^\circ\text{C}$ $T_A = 25 \text{ }^\circ\text{C}$ | 1389 | mW |
| Safety Input Power (NB SOIC-8) | P_S | $\theta_{JA} = 112 \text{ }^\circ\text{C/W}$ $T_J = 150 \text{ }^\circ\text{C}$ $T_A = 25 \text{ }^\circ\text{C}$ | 1116 | mW |
| Note: | | | | |
| 1. Maximum value allowed in the event of a failure. Refer to the thermal derating curves below. | | | | |

Table 4.3. Thermal Characteristics

| Parameter | Symbol | WB Stretched SOIC-8 | NB SOIC-8 | Unit |
|---------------------------------------|---------------|---------------------|-----------|------|
| IC Junction-to-Air Thermal Resistance | θ_{JA} | 90 | 112 | °C/W |

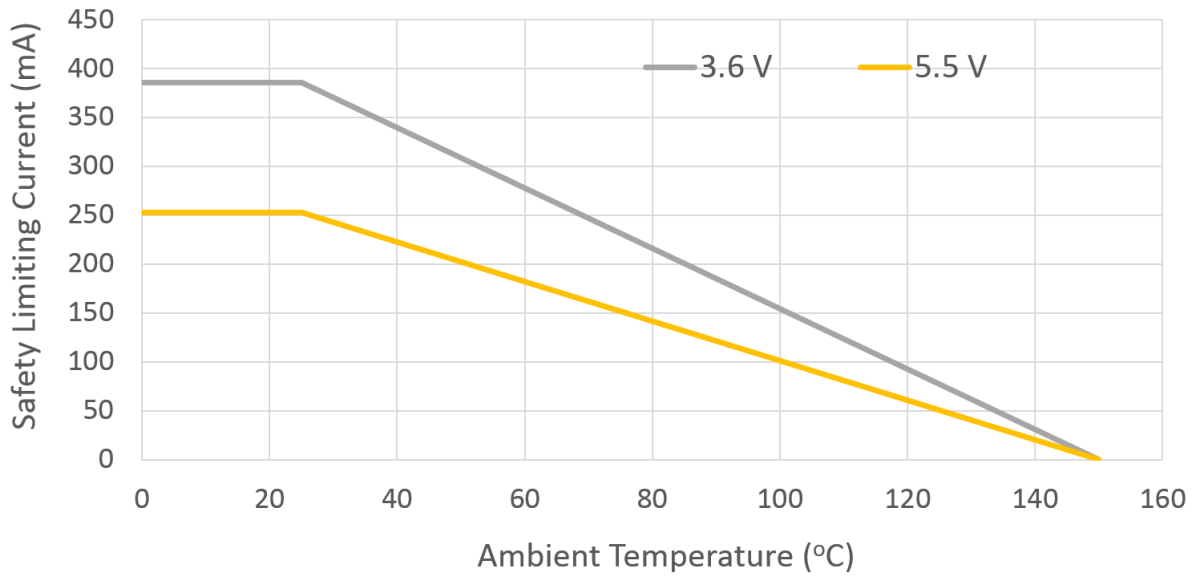


Figure 4.2. WB Stretched SOIC-8 Thermal Derating Curve for Safety Limiting Current

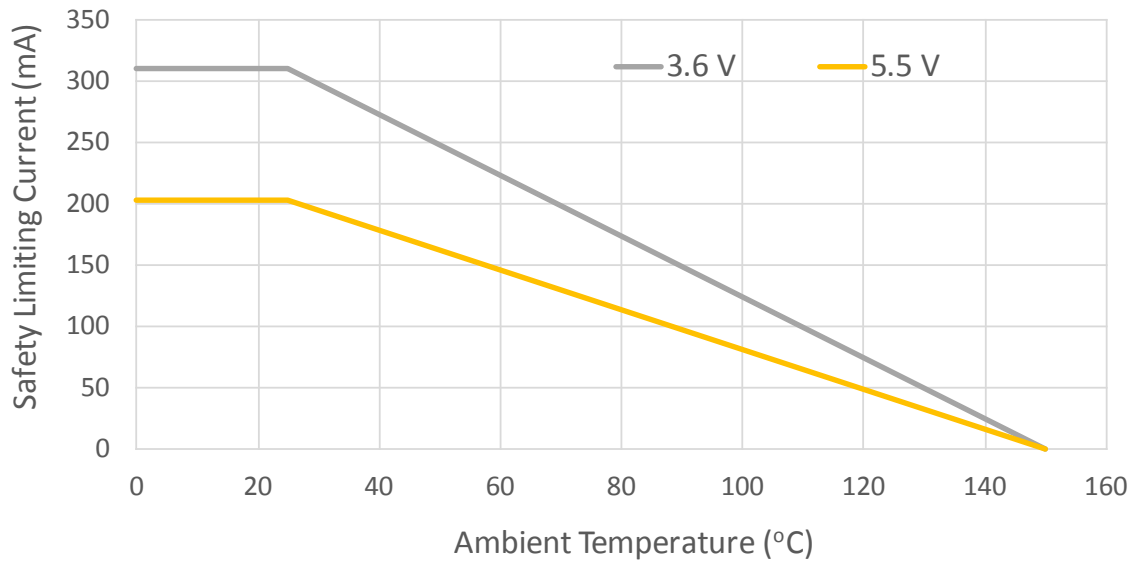


Figure 4.3. NB SOIC-8 Thermal Derating Curve for Safety Limiting Current

Table 4.4. Absolute Maximum Ratings¹

| Parameter | Symbol | Min | Max | Unit |
|---------------------------------------|----------------|------|------------|------|
| Storage Temperature | T_{STG} | -65 | 150 | °C |
| Ambient Temperature Under Bias | T_A | -40 | 125 | °C |
| Junction Temperature | T_J | — | 150 | °C |
| Supply Voltage | VDDA, VDDB | -0.5 | 6.0 | V |
| Input Voltage respect to GNDA | VAIP, VAIN | -0.5 | VDDx + 0.5 | V |
| Output Sink or Source Current | I _o | — | 5 | mA |
| Total Power Dissipation | P_T | — | 212 | mW |
| Lead Solder Temperature (10 s) | | — | 260 | °C |
| Human Body Model ESD Rating | | 6000 | — | V |
| Capacitive Discharge Model ESD Rating | | 2000 | — | V |

Note:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of the data sheet.

4.1 Regulatory Information

Table 4.5. Regulatory Information^{1, 2}

| |
|--|
| CSA |
| The Si8921 is certified under CSA. For more details, see Master Contract Number 232873. |
| 62368-1: Up to 600 V _{RMS} reinforced insulation working voltage; up to 1000 V _{RMS} basic insulation working voltage. |
| VDE |
| The Si8921 is pending certification under VDE. For more details, see File 5028467. |
| IEC60747-17: Up to 2121 V _{peak} for reinforced insulation working voltage. |
| EN62368-1: Up to 600 V _{RMS} reinforced insulation working voltage; up to 1000 V _{RMS} basic insulation working voltage. |
| UL |
| The Si8921 is certified under UL1577 component recognition program. For more details, see File E257455. |
| Rated up to 5000 V _{RMS} isolation voltage for basic protection. |
| CQC |
| The Si8921 is certified under GB4943.1-2011. |
| Rated up to 250 V _{RMS} reinforced insulation working voltage at 5000 meters. |
| Note: |
| 1. Regulatory Certifications apply to 5 kV _{RMS} rated devices which are production tested to 6.0 kV _{RMS} for 1 s. |
| 2. Regulatory Certifications apply to 2.5 kV _{RMS} rated devices which are production tested to 3.0 kV _{RMS} for 1 s. |

Table 4.6. Insulation and Safety-Related Specifications

| Parameter | Symbol | Test Condition | Value | | Unit |
|---|-----------------|----------------|--------------------|------------------|------|
| | | | WB Stretched SOIC8 | NB SOIC8 | |
| Nominal External Air Gap (Clearance) | CLR | | 8 | 4 | mm |
| Nominal External Tracking (Creepage) | CRP | | 8 | 4 | mm |
| Minimum Internal Gap (Internal Clearance) | DTI | | 36 | 36 | μm |
| Tracking Resistance | PTI or CTI | IEC60112 | 600 | 600 | V |
| Erosion Depth | ED | | 0.019 | 0.04 | mm |
| Resistance (Input-Output) ¹ | R _{IO} | | 10 ¹² | 10 ¹² | Ω |
| Capacitance (Input-Output) ¹ | C _{IO} | f = 1 MHz | 1 | 1 | pF |
| Note: | | | | | |
| 1. To determine resistance and capacitance, the Si8921/22 is converted into a 2-terminal device. Pins 1–4 are shorted together to form the first terminal, and pins 5–8 are shorted together to form the second terminal. The parameters are then measured between these two terminals. | | | | | |

Table 4.7. IEC 60664-1 Ratings

| Parameter | Test Conditions | Specification | |
|-----------------------------|---|--------------------|----------|
| | | WB Stretched SOIC8 | NB SOIC8 |
| Basic Isolation Group | Material Group | I | I |
| Installation Classification | Rated Mains Voltages $\leq 150 V_{RMS}$ | I-IV | I-IV |
| | Rated Mains Voltages $\leq 300 V_{RMS}$ | I-IV | I-IV |
| | Rated Mains Voltages $\leq 600 V_{RMS}$ | I-IV | I-III |

Table 4.8. IEC 60747-17 Insulation Characteristics¹

| Parameter | Symbol | Test Condition | Characteristic | | Unit |
|--------------------------------------|------------|--|--------------------|----------|------------|
| | | | WB Stretched SOIC8 | NB SOIC8 | |
| Maximum Working Isolation Voltage | V_{IORM} | | 1500 | 1500 | V_{RMS} |
| Maximum Repetitive Isolation Voltage | V_{IORM} | | 2121 | 2121 | V_{peak} |
| Input to Output Test Voltage | V_{PR} | Method b1 ($V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test, $t_m = 1$ s, Partial Discharge < 5 pC) | 3976 | 3976 | V_{peak} |
| Maximum Transient Isolation Voltage | V_{IOTM} | $t = 60$ s | 8000 | 4000 | V_{peak} |
| Maximum Surge Isolation Voltage | V_{IOSM} | Test voltage is $\geq 1.3 \times V_{IMP}$, minimum 10000 V_{peak} and 1.2 $\mu s/50 \mu s$ | 10400 | 10400 | V_{peak} |
| Maximum Impulse Voltage | V_{IMP} | | 8000 | 5656 | V_{peak} |
| Pollution Degree | | DIN VDE 0110 | 2 | 2 | |
| Insulation Resistance | R_S | $T_{AMB} = T_S$, $V_{IO} = 500$ V | $>10^9$ | $>10^9$ | Ω |

Note:

1. This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si8921/22 provides a climate classification of 40/125/21.

4.2 Typical Operating Characteristics

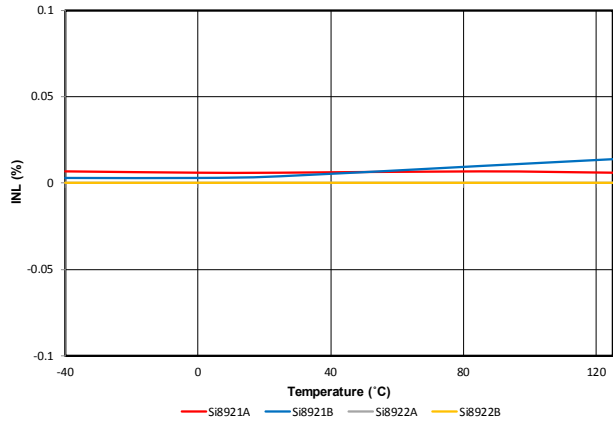


Figure 4.4. Nonlinearity (%) vs. Temperature (°C)

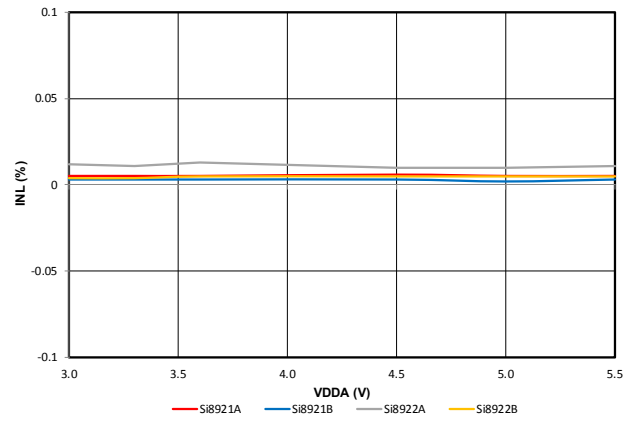


Figure 4.5. Nonlinearity (%) vs. VDDA Supply (V)

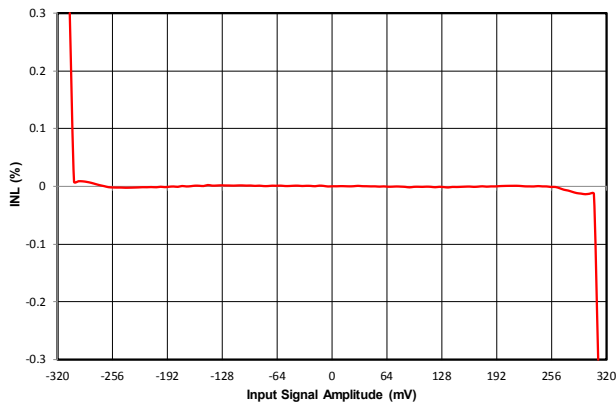


Figure 4.6. Si8921B Nonlinearity (%) vs. Input Signal Amplitude (mV)

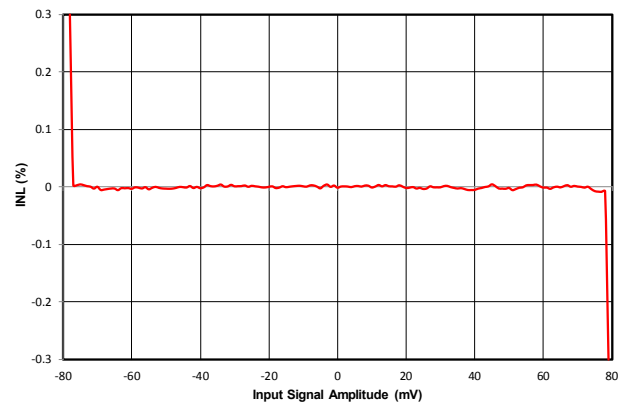


Figure 4.7. Si8921A Nonlinearity (%) vs. Input Signal Amplitude (mV)

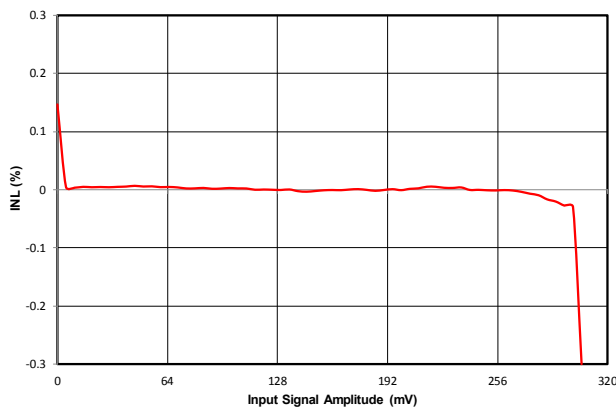


Figure 4.8. Si8922B Nonlinearity (%) vs. Input Signal Amplitude (mV)

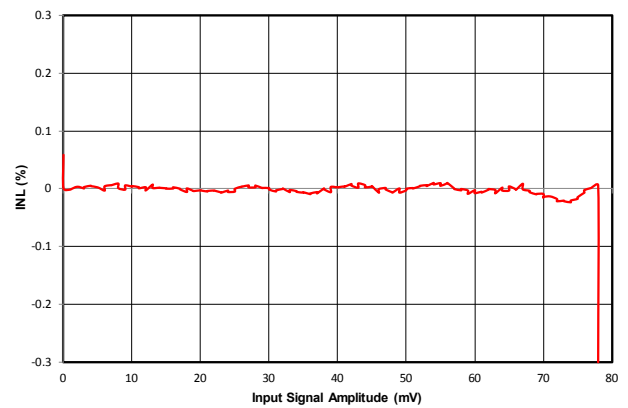


Figure 4.9. Si8922A Nonlinearity (%) vs. Input Signal Amplitude (mV)

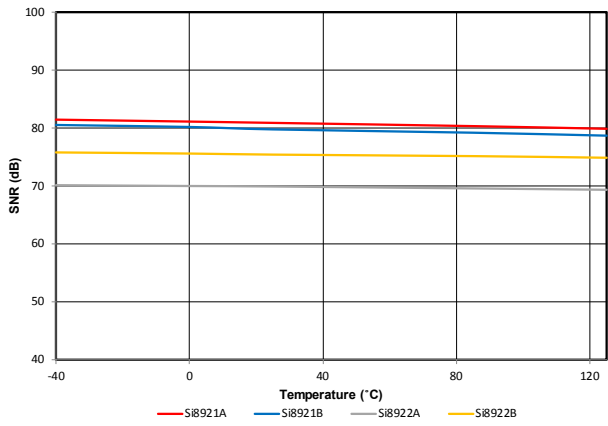


Figure 4.10. Signal-to-Noise Ratio (dB) vs. Temperature (°C)

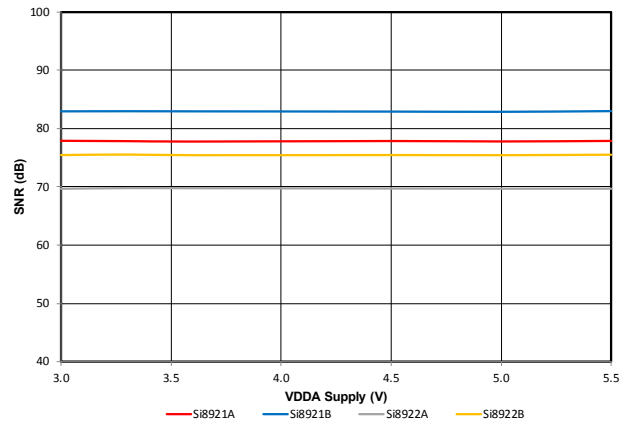


Figure 4.11. Signal-to-Noise Ratio (dB) vs. VDDA Supply (V)

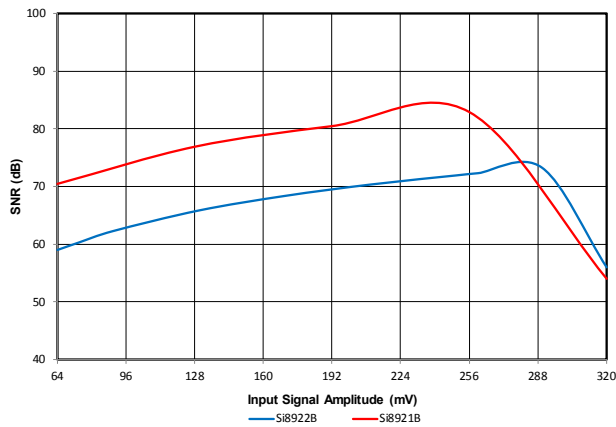


Figure 4.12. Si892xB Signal-to-Noise Ratio (dB) vs. Input Signal Amplitude (mV)

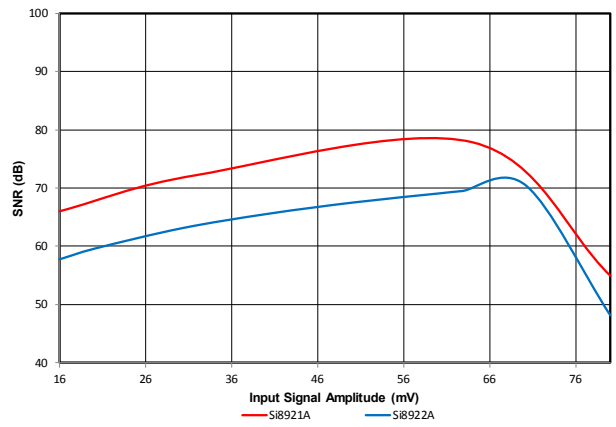


Figure 4.13. Si892xA Signal-to-Noise Ratio (dB) vs. Input Signal Amplitude (mV)

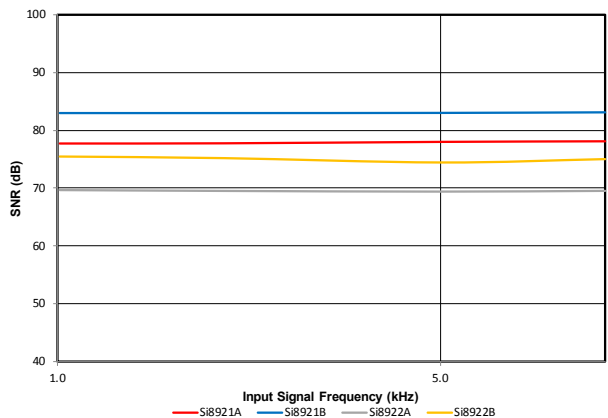


Figure 4.14. Signal-to-Noise Ratio (dB) vs. Input Signal Frequency (kHz)

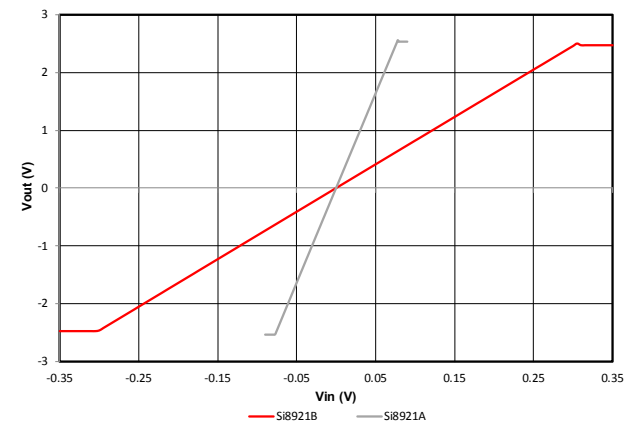


Figure 4.15. Si8921 Output Voltage (V) vs. Input Voltage (V)

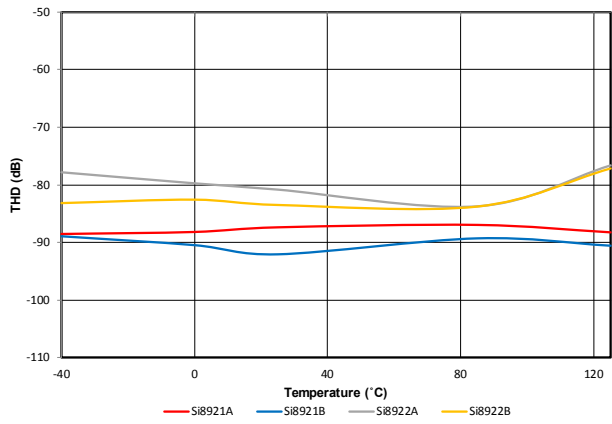


Figure 4.16. Total Harmonic Distortion (dB) vs. Temperature (°C)

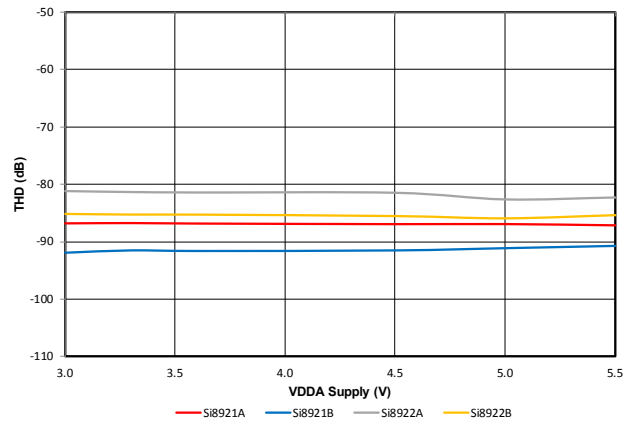


Figure 4.17. Total Harmonic Distortion (dB) vs. VDDA Supply (V)

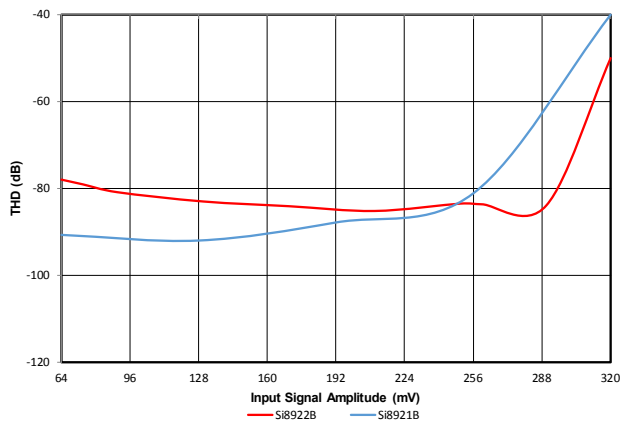


Figure 4.18. Si892xB Total Harmonic Distortion (dB) vs. Input Signal Amplitude (mV)

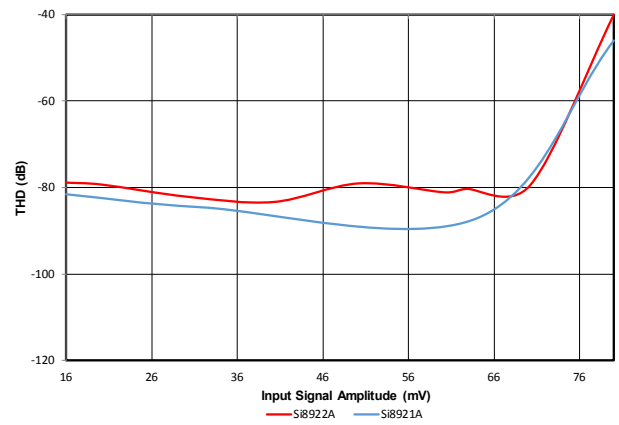


Figure 4.19. Si892xA Total Harmonic Distortion (dB) vs. Input Signal Amplitude (mV)

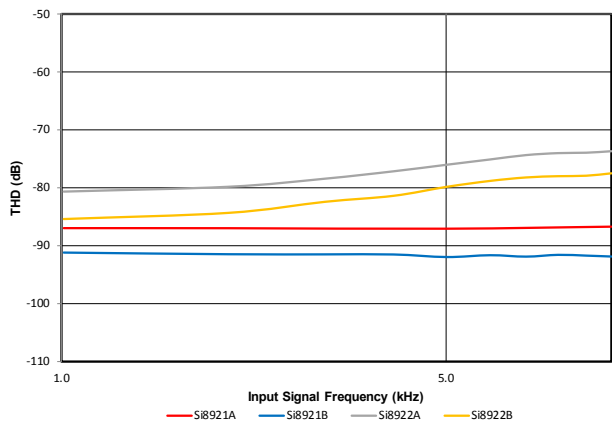


Figure 4.20. Total Harmonic Distortion (dB) vs. Input Signal Frequency (kHz)

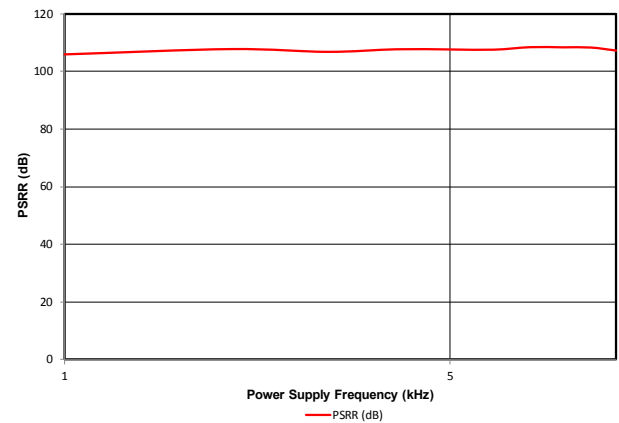


Figure 4.21. Power Supply Rejection Ratio vs. Power Supply Frequency (kHz)

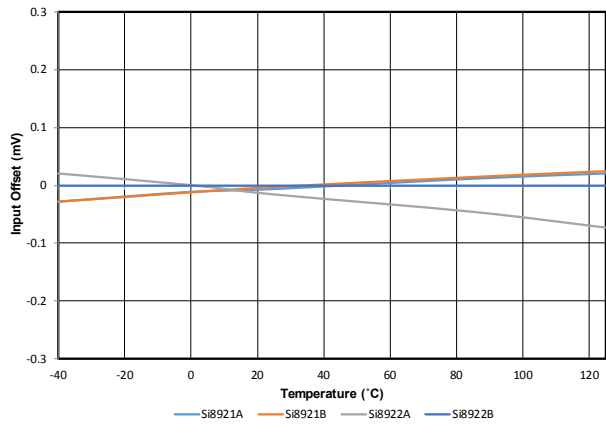


Figure 4.22. Input Offset (mV) vs. Temperature (°C)

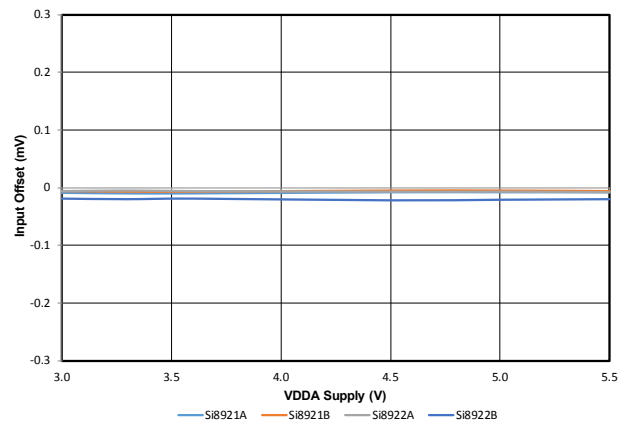


Figure 4.23. Input Offset (mV) vs. VDDA Supply (V)

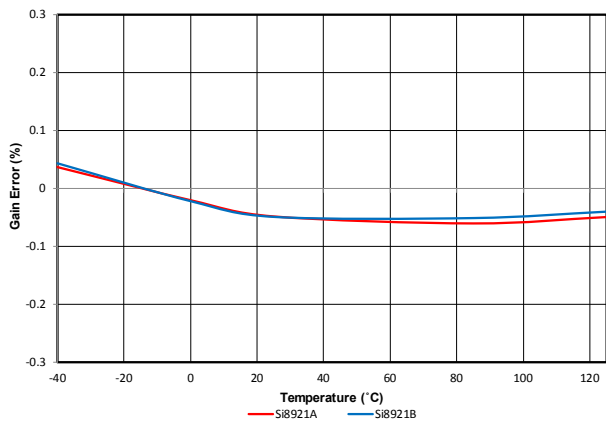


Figure 4.24. Gain Error (%) vs. Temperature (°C)

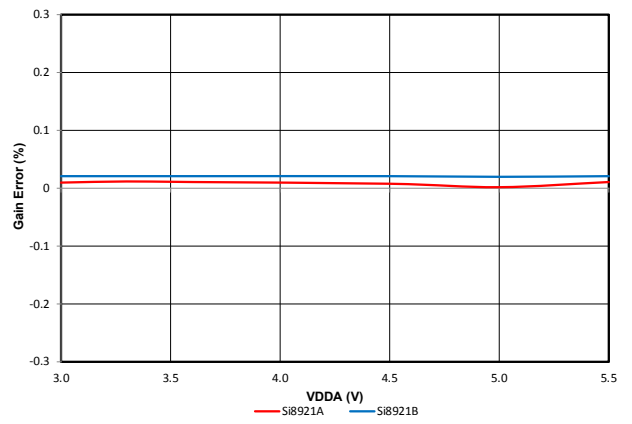


Figure 4.25. Gain Error (%) vs. VDDA Supply (V)

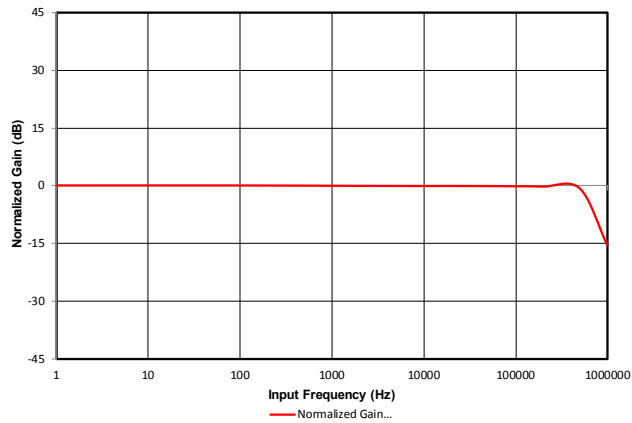


Figure 4.26. Amplifier Bandwidth

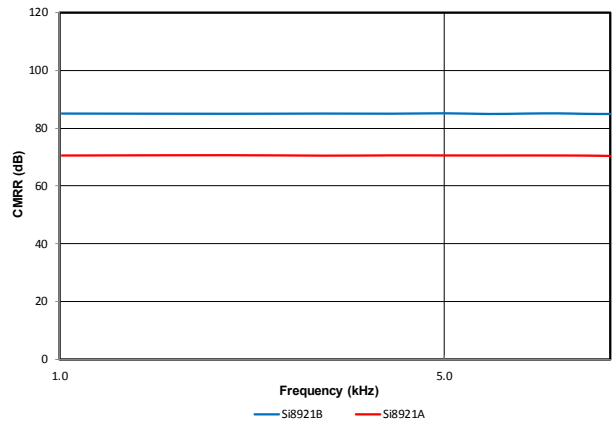


Figure 4.27. Common-Mode Rejection Ratio (dB) vs. Input Frequency (kHz)

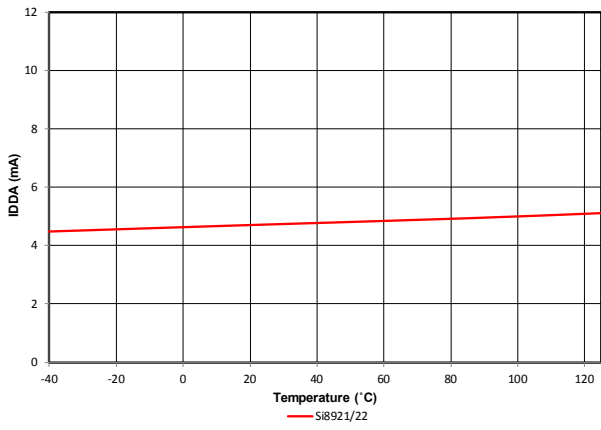


Figure 4.28. IDDA (mA) vs. Temperature (°C)

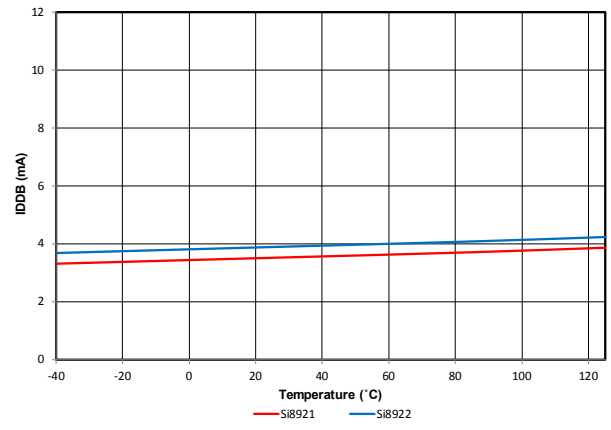


Figure 4.29. IDDB (mA) vs. Temperature (°C)

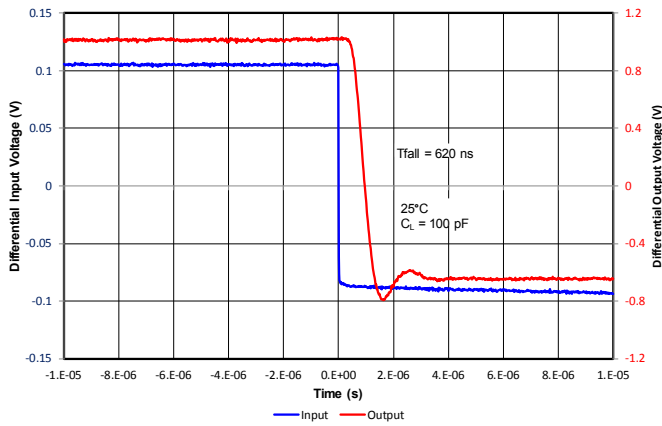


Figure 4.30. Si8921B High-to-Low Step Response

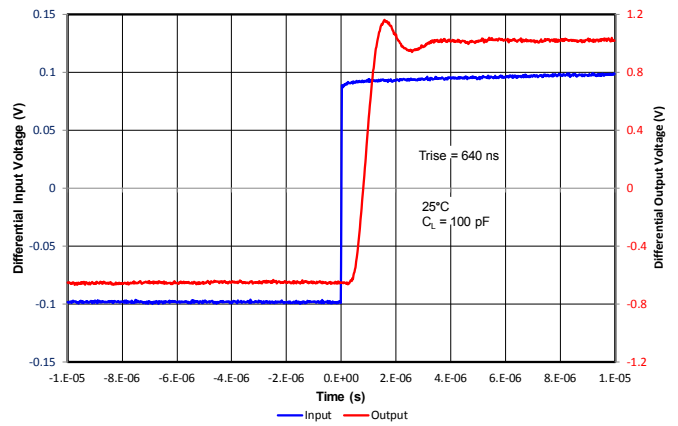


Figure 4.31. Si8921B Low-to-High Step Response

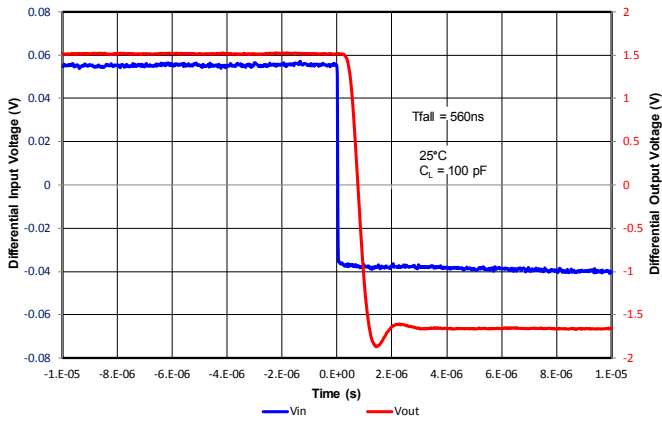


Figure 4.32. Si8921A High-to-Low Step Response

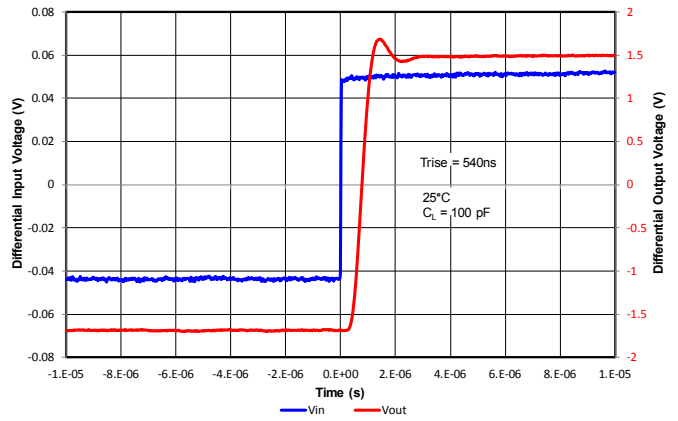


Figure 4.33. Si8921A Low-to-High Step Response

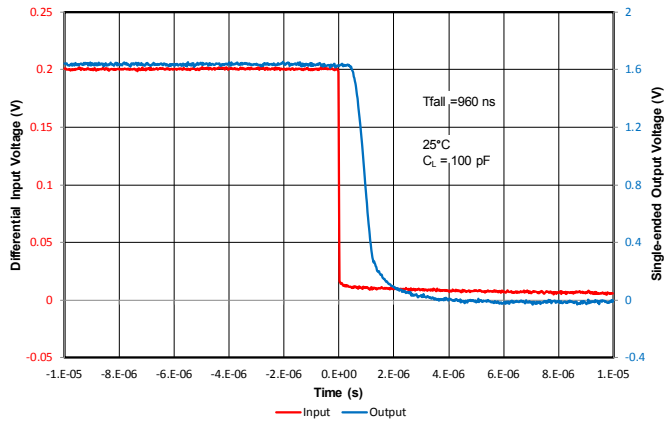


Figure 4.34. Si8922B High-to-Low Step Response

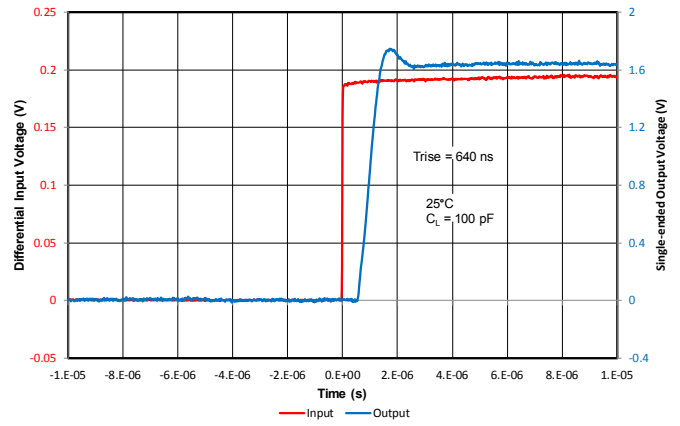


Figure 4.35. Si8922B Low-to-High Step Response

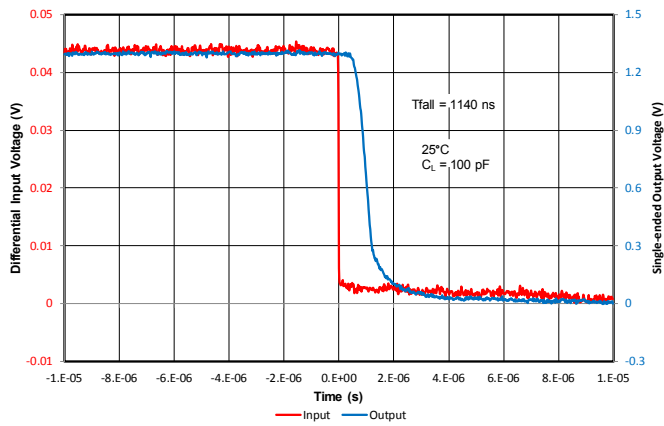


Figure 4.36. Si8922A High-to-Low Step Response

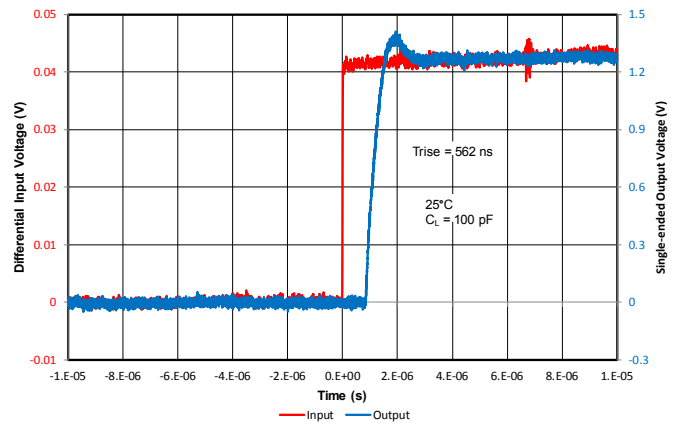


Figure 4.37. Si8922A Low-to-High Step Response

5. Pin Descriptions

5.1 Si8921 Pin Descriptions

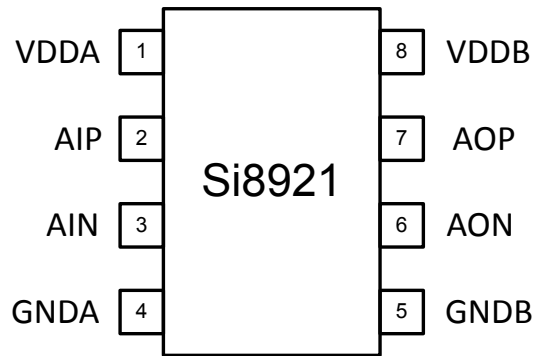


Table 5.1. Si8921 Pin Descriptions

| Name | Pin Number | Description |
|------|------------|--------------------------|
| VDDA | 1 | Input side power supply |
| AIP | 2 | Analog input high |
| AIN | 3 | Analog input low |
| GNDA | 4 | Input side ground |
| GNDB | 5 | Output side ground |
| AON | 6 | Analog output low |
| AOP | 7 | Analog output high |
| VDDB | 8 | Output side power supply |

5.2 Si8922 Pin Descriptions

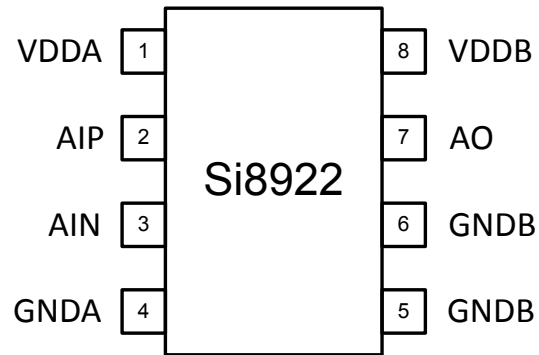


Table 5.2. Si8922 Pin Descriptions

| Name | Pin Number | Description |
|------|------------|--------------------------|
| VDDA | 1 | Input side power supply |
| AIP | 2 | Analog input high |
| AIN | 3 | Analog input low |
| GNDA | 4 | Input side ground |
| GNDB | 5 | Output side ground |
| GNDB | 6 | Output side ground |
| AO | 7 | Analog output |
| VDDB | 8 | Output side power supply |

6. Packaging

6.1 Package Outline: 8-Pin Wide Body Stretched SOIC

The figure below illustrates the package details for the Si8921/22 in a 8-Pin Wide Body Stretched SOIC package. The table lists the values for the dimensions shown in the illustration.

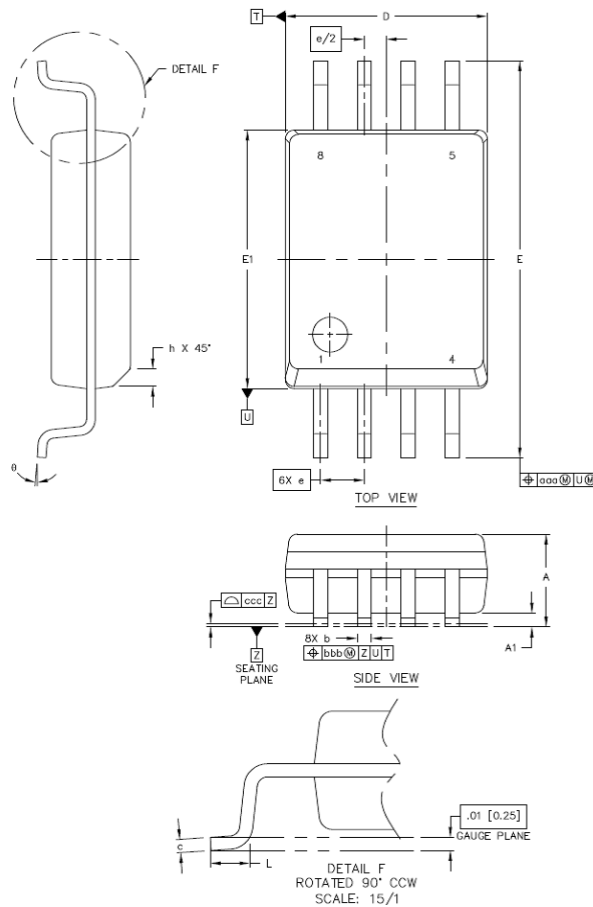


Figure 6.1. 8-Pin Wide Body Stretched SOIC Package

Table 6.1. 8-Pin Wide Body Stretched SOIC Package Diagram Dimensions

| Dimension | MIN | MAX |
|-----------|----------|-------|
| A | 2.49 | 2.79 |
| A1 | 0.36 | 0.46 |
| b | 0.30 | 0.51 |
| c | 0.20 | 0.33 |
| D | 5.74 | 5.94 |
| E | 11.25 | 11.76 |
| E1 | 7.39 | 7.59 |
| e | 1.27 BSC | |
| L | 0.51 | 1.02 |
| h | 0.25 | 0.76 |
| θ | 0° | 8° |

| Dimension | MIN | MAX |
|-----------|-----|------|
| aaa | -- | 0.25 |
| bbb | -- | 0.25 |
| ccc | -- | 0.10 |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

6.2 Package Outline: 8-Pin Narrow Body SOIC

The figure below illustrates the package details for the Si8921/22 in an 8-Pin Narrow Body SOIC package. The table lists the values for the dimensions shown in the illustration.

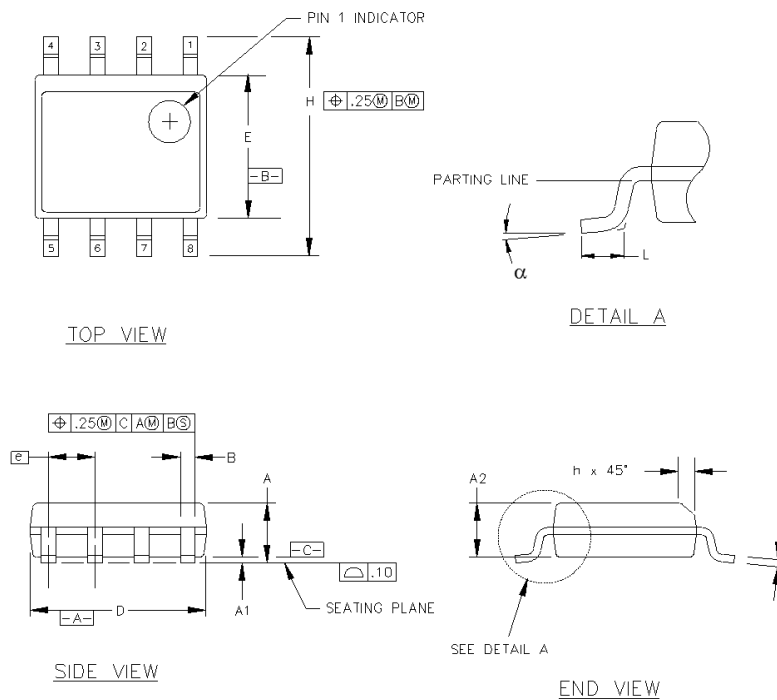


Figure 6.2. 8-Pin Narrow Body SOIC Package

Table 6.2. 8-Pin Narrow Body SOIC Package Diagram Dimensions

| Dimension | Min | Max |
|-----------|----------|----------|
| A | 1.35 | 1.75 |
| A1 | 0.10 | 0.25 |
| A2 | 1.40 REF | 1.55 REF |
| B | 0.33 | 0.51 |
| C | 0.19 | 0.25 |
| D | 4.80 | 5.00 |
| E | 3.80 | 4.00 |
| e | 1.27 BSC | |
| H | 5.80 | 6.20 |
| h | 0.25 | 0.50 |
| L | 0.40 | 1.27 |
| α | 0° | 8° |

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. This drawing conforms to JEDEC Outline MS-102.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020B specification for Small Body Components.

6.3 Land Pattern: 8-Pin Wide Body Stretched SOIC

The figure below illustrates the recommended land pattern details for the Si8921/22 in a 8-Pin Wide Body Stretched SOIC package. The table lists the values for the dimensions shown in the illustration.

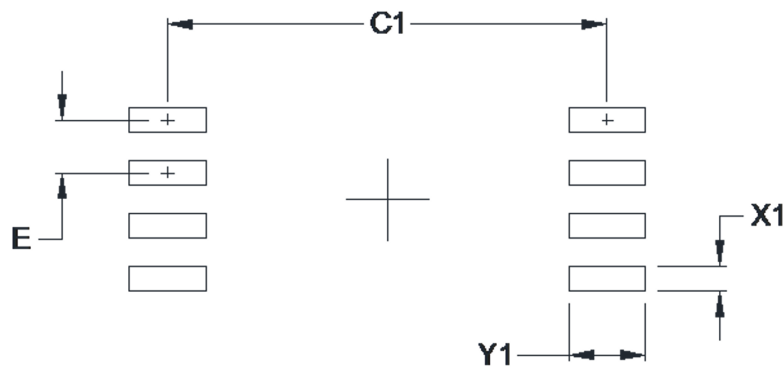


Figure 6.3. 8-Pin Wide Body Stretched SOIC Land Pattern

Table 6.3. 8-Pin Wide Body Stretched SOIC Land Pattern Dimensions

| Symbol | mm |
|--------|-------|
| C1 | 10.60 |
| E | 1.27 |
| X1 | 0.60 |
| Y1 | 1.85 |

Note:

General

1. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pins.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.4 Land Pattern: 8-Pin Narrow Body SOIC

The figure below illustrates the recommended land pattern details for the Si8921/22 in a 8-Pin Narrow Body SOIC package. The table lists the values for the dimensions shown in the illustration.

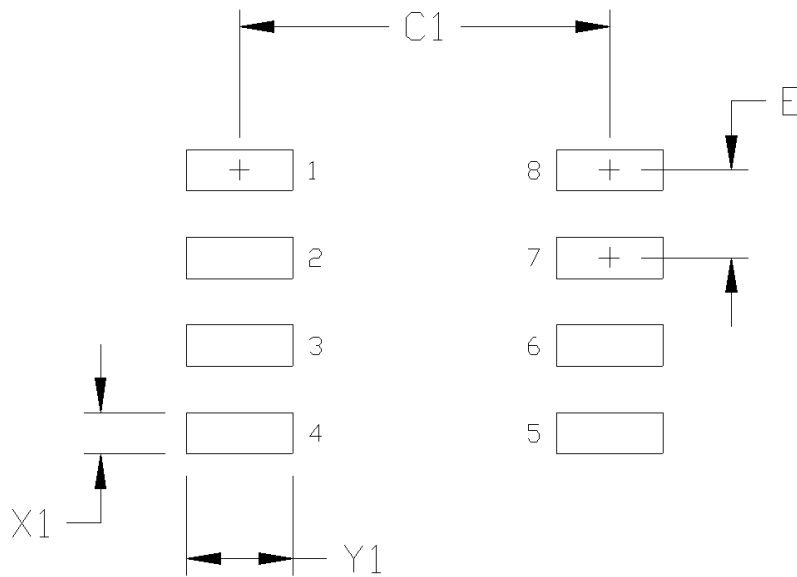


Figure 6.4. 8-Pin Narrow Body SOIC Land Pattern

Table 6.4. 8-Pin Narrow Body SOIC Land Pattern Dimensions

| Symbol | mm |
|--------|------|
| C1 | 5.40 |
| E | 1.27 |
| X1 | 0.60 |
| Y1 | 1.55 |

Note:

1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X173-8N for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

6.5 Top Marking: 8-Pin Wide Body Stretched SOIC

The figure below illustrates the top markings for the Si8921/22 in a 8-Pin Wide Body Stretched SOIC package. The table explains the top marks shown in the illustration.

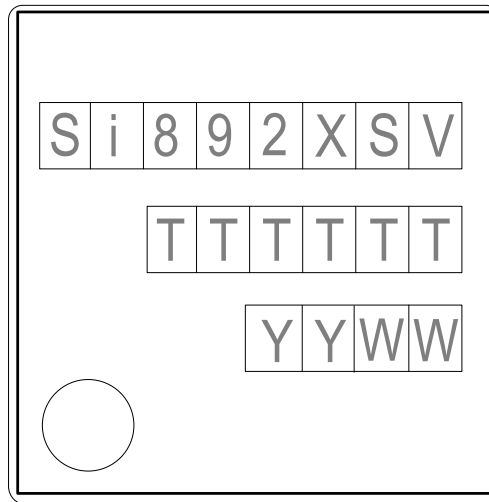


Figure 6.5. Si8921 8-Pin Wide Body Stretched SOIC Top Marking

Table 6.5. 8-Pin Wide Body Stretched SOIC Top Mark Explanation

| | | |
|------------------------|--|---|
| Line 1 Marking: | Customer Part Number | Si892X = Isolator Amplifier Series X = Base part number <ul style="list-style-type: none"> • 1 = Differential output • 2 = Single-ended output S = Input Range: <ul style="list-style-type: none"> • A = ± 62.5 mV • B = ± 250 mV V = Insulation rating: <ul style="list-style-type: none"> • D = 5.0 kVrms |
| Line 2 Marking: | TTTTTT = Mfg Code | Manufacturing Code from the Assembly Purchase Order form. |
| Line 3 Marking: | YY = Year WW = Work Week Circle = 43 mils Diameter Left-Justified | Assigned by the Assembly House. Corresponds to the year and work week of the mold date. |

6.6 Top Marking: 8-Pin Narrow Body SOIC

The figure below illustrates the top markings for the Si8921/22 in a 8-Pin Narrow Body SOIC package. The table explains the top marks shown in the illustration.

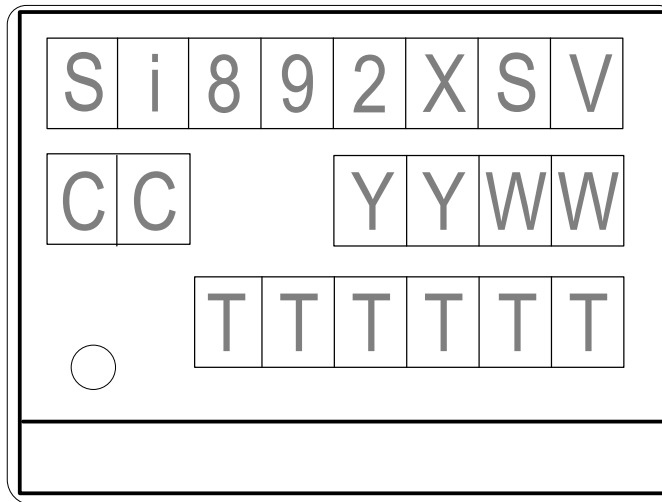


Figure 6.6. 8-Pin Narrow Body SOIC Top Marking

Table 6.6. 8-Pin Narrow Body SOIC Top Marking Explanation

| | | |
|------------------------|--|--|
| Line 1 Marking: | Customer Part Number | <p>Si892X = Isolator Amplifier Series</p> <p>X = Base part number</p> <ul style="list-style-type: none"> • 1 = Differential output • 2 = Single-ended output <p>S = Input Range:</p> <ul style="list-style-type: none"> • A = ± 62.5 mV • B = ± 250 mV <p>V = Insulation rating:</p> <ul style="list-style-type: none"> • B = 2.5 kVrms |
| Line 2 Marking: | <p>CC = Country of Origin ISO Code Abbreviation</p> <p>YY = Year</p> <p>WW = Work Week</p> | Assigned by the Assembly House. Corresponds to the year and work week of the mold date. |
| Line 3 Marking: | <p>TTTTTT = Mfg Code</p> <p>Circle = 19.7 mils Diameter</p> <p>Left-Justified</p> | Manufacturing Code from the Assembly Purchase Order form. |

7. Revision History

Revision 206437A

December, 2022

- Updated decimal-based revision number to alphanumeric code.

Revision 0.9

September, 2022

- Updated Safety Approvals on front page.
- Updated minimum supply currents in [4. Electrical Specifications](#).
- Updated [4.1 Regulatory Information](#).

Revision 0.8

June, 2021

- Added Automotive OPNs and updated specified input range in [1. Ordering Guide](#).
- Updated [Figure 3.1 Current Sense Application on page 5](#).
- Added linearity minimum specification to [Table 4.1 Electrical Specifications on page 7](#).

Revision 0.7

April, 2020

- Numerous clarifications throughout.
- Updated [4. Electrical Specifications](#) after full characterization.
- Changed Si8922 Pin 6 from NC to GND.

Revision 0.51

June, 2019

- Added section for Automotive Grade OPNs.
- Corrected error in Specified Linear Input Range on page 6.
- Changed DTI Specification on page 11.
- Corrected [Si8922 Pin Diagram](#) on page 20.
- Updated supply currents on page 6.

Revision 0.5

March, 2019

- Updated specifications.
- Added narrow body SOIC-8 package.

Revision 0.1

February, 2018

- Initial release.

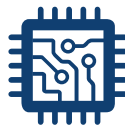


**Connecting Everyone
and Everything,
All the Time**



Portfolio

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Quality

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Support & Resources

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