VSC8522-02 Datasheet
12-Port 10/100/1000BASE-T PHY with QSGMII MAC

Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Learn more at www.microsemi.com.

Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.2

Revision 4.2 of this datasheet was published in February 2019. In revision 4.2, VeriPHY descriptions were updated and VeriPHY register information was deleted. For functional details of the VeriPHY suite and operating instructions, see the ENT-AN0125 PHY, Integrated PHY-Switch VeriPHY - Cable Diagnostics application note.

1.2 Revision 4.1

Revision 4.1 of this datasheet was published in May 2014. The following is a summary of the changes made to the datasheet:

- Information about the device SerDes MAC and the device media interface was updated. Neither the integrated SerDes media access controller (MAC) or the enhanced SerDes media interface of the device include internal AC-decoupling capacitors; external capacitors must be used.
- The functional block diagram of the device was changed to show the correct direction of the SERDES_E(3:1)_TXN, the SERDES_E(3:1)_RXP, and the SERDES_E(3:1)_RXN signals.
- Information about AC-coupling, which is required when using a differential reference clock (REFCLK) input, was added.
- Information about the typical input impedance for a differential REFCLK signal (R_I) was added.
- The order of the information in the Pins by Function section was changed to match the alphabetical sort in the Pins spreadsheet attached to this document.
- References to SFP functionality, Basic Serial LED functionality, and Parallel LED signal detection (part of the Enhanced LED Control) were removed from this document. These functions are not supported in this device. The Functional Group of pins 40, 41, 42, 43, 44, 45, 47, 49, 50, A14, and A15 were changed from Multipurpose to Miscellaneous.

1.3 Revision 4.0

Revision 4.0 of this datasheet was published in December 2012. In revision 4.0 of the document, errata items, which were previously published in the VSC8522-02 Errata revision 1.0 as open issues, are now reconciled in the datasheet. Now that the information is available in the datasheet, the previously published errata document no longer applies, and it has been removed from the Microsemi Web site.

1.4 Revision 2.0

- Revision 2.0 of this datasheet was published in September 2012. This was the first publication of the document.

2 Introduction

This document consists of descriptions and specifications for both functional and physical aspects of the VSC8522-02 12-port 10/100/1000BASE-T PHY device for the Ethernet market segment.

In addition to datasheets, the Microsemi Web site offers an extensive library of documentation, support files, and application materials specific to each device. The address of the Microsemi Web site is www.microsemi.com.

2.1 Register and Bit Conventions

This document refers to registers by their address and bit number in decimal notation. A range of bits is indicated with a colon. For example, a reference to address 26, bits 15 through 14 is shown as 26.15:14.

A register with an E and a number attached (example 27E1) means it is a register contained within extended register page number 1. A register with a G attached (example 13G) means it is a GPIO page register.

Bit numbering follows the IEEE standard with bit 15 being the most significant bit and bit 0 being the least significant bit.

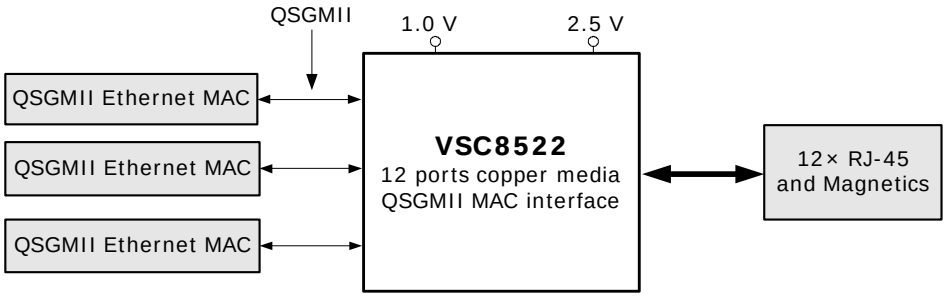
3 Overview

The VSC8522-02 is a low-power 12-port Gigabit Ethernet transceiver. It has a low electromagnetic interference (EMI) line driver and integrated line side termination resistors that conserve both power and printed circuit board (PCB) space.

Microsemi's mixed signal and digital signal processing (DSP) architecture is a key operational feature of the VSC8522-02, assuring robust performance even under less-than-favorable environmental conditions. It supports both half-duplex and full duplex 10BASE-T, 100BASE-TX, and 1000BASE-T communication speeds over Category 5 (Cat5) unshielded twisted pair (UTP) cable at distances greater than 100 m, displaying excellent tolerance to NEXT, FEXT, echo, and other types of ambient environmental and system electronic noise.

The following illustration shows a high-level, general view of a typical VSC8522-02 application.

Figure 1 • **QSGMII Application Diagram**



3.1 Key Features

This section lists the main features and benefits of the VSC8522-02 device.

Low Power

- Low power consumption of approximately 425 mW per port in 1000BASE-T mode, 200 mW per port in 100BASE-TX mode, and 225 mW per port in 10BASE-T mode
- ActiPHY™ link down power savings
- PerfectReach™ smart cable reach algorithm
- IEEE 802.3az Energy Efficient Ethernet idle power savings

Wide Range of Support

- Compliant with IEEE 802.3 (10BASE-T, 100BASE-TX, and 1000BASE-T) specifications
- Support for >16 kB jumbo frames in all speeds with programmable synchronization FIFOs
- Supports Cisco QSGMII v1.3, IEEE 1149.1 JTAG boundary scan, and IEEE 1149.6 AC-JTAG
- Support for applications that need to meet 2 kV CDE, IEC 61000-4-2 at 8 kV
- Available in a low-cost, 302-pin TQFP package with a 24 mm × 24 mm body size for low-power, fanless applications

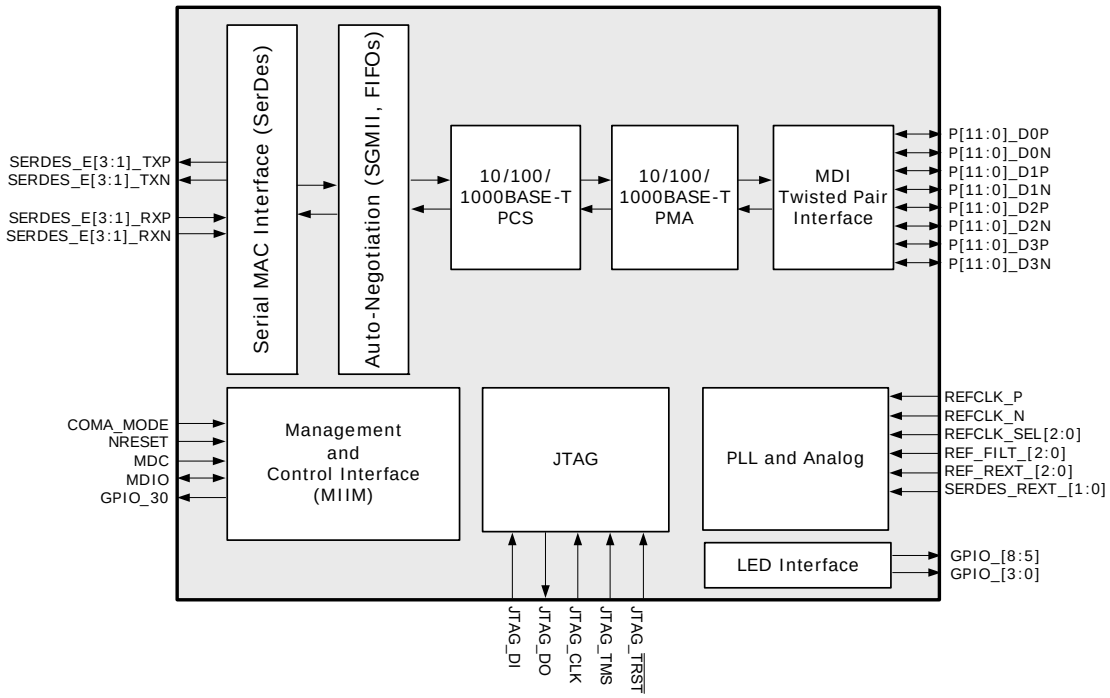
Flexibility

- VeriPHY® cable diagnostics suite provides extensive network cable operating conditions and status
- Patented, low EMI line driver with integrated line side termination resistors
- Serial LED interface option
- Extensive test features including near end, far end, copper media connector, SerDes MAC loopback, and Ethernet packet generator with CRC error counter to decrease time-to-market

3.2 Block Diagram

The following illustration shows the primary functional blocks of the VSC8522-02 device.

Figure 2 • **Block Diagram**



4 Functional Descriptions

This section provides detailed information about the functionality of the VSC8522-02 device, available configurations, operational features, and testing functionality. It includes descriptions of the various device interfaces and their configuration. With the information in this section, the device setup parameters can be determined for configuring the VSC8522-02 part for use in a particular application.

4.1 Operating Mode

The VSC8522-02 supports 10/100/1000BASE-T media through the QSGMII MAC-to-Cat5 Link Partner operating mode (ports 8-11). For more information, see Figure 1, page 3.

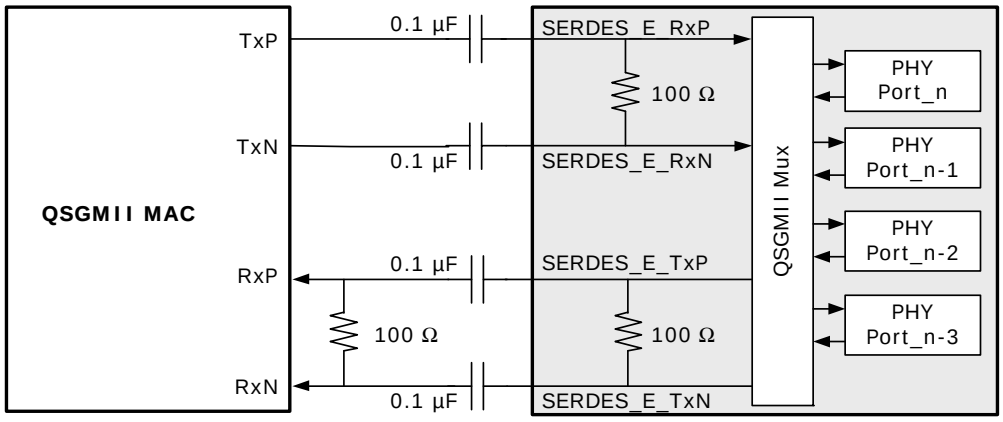
4.2 SerDes MAC Interface

The VSC8522-02 SerDes MAC interface performs data serialization and deserialization functions using an integrated SerDes block. The interface operates in QSGMII mode. The Enhanced SerDes block includes an integrated termination resistor. Register 19G is a global register and only needs to be set once to configure the device. The other register bits are configured on a per-port basis and the operation either needs to be repeated for each port, or a broadcast write needs to be used by setting register 22, bit 0 to configure all the ports simultaneously.

4.2.1 QSGMII MAC

The VSC8522-02 device supports a QSGMII MAC to convey four ports of network data and port speed between 10BASE-T, 100BASE-T, and 1000BASE-T data rates and operates in both half-duplex and full-duplex at all port speeds. To configure the device for QSGMII MAC mode, set register 19G, bits 15:14 = 00 or 10. This device also supports SGMII MAC-side autonegotiation on each individual port and is enabled through register 16E3, bit 7, of that port.

Figure 3 • **QSGMII MAC Interface**



4.3 PHY Addressing and Port Mapping

This section contains information about PHY addressing and port mapping.

4.3.1 PHY Addressing

The VSC8522-02 includes two external PHY address pins to allow control of multiple PHY devices on a system board that are sharing a common management bus. Based on the settings of these two address

control pins, the internal PHYs in the VSC8522-02 device take on the address ranges as shown in the following table.

Table 1 • **PHY Address Range Selection**

PHYADD4	PHYADD3	Internal PHY Addresses
0	0	0–11
0	1	12–23
1	0	4–15
1	1	20–31

4.3.2 SerDes Port Mapping

The VSC8522-02 includes three 5 GHz enhanced SerDes macros. The following table shows the SerDes port mapping in QSGMII to CAT5 mode of operation.

Table 2 • **SerDes Port Mapping**

Interface Pins	Mode
SERDES_E1_TXP, SERDES_E1_TXN	QSGMII0
SERDES_E1_RXP, SERDES_E1_RXN	QSGMII0
SERDES_E2_TXP, SERDES_E2_TXN	QSGMII1
SERDES_E2_RXP, SERDES_E2_RXN	QSGMII1
SERDES_E3_TXP, SERDES_E3_TXN	QSGMII2
SERDES_E3_RXP, SERDES_E3_RXN	QSGMII2

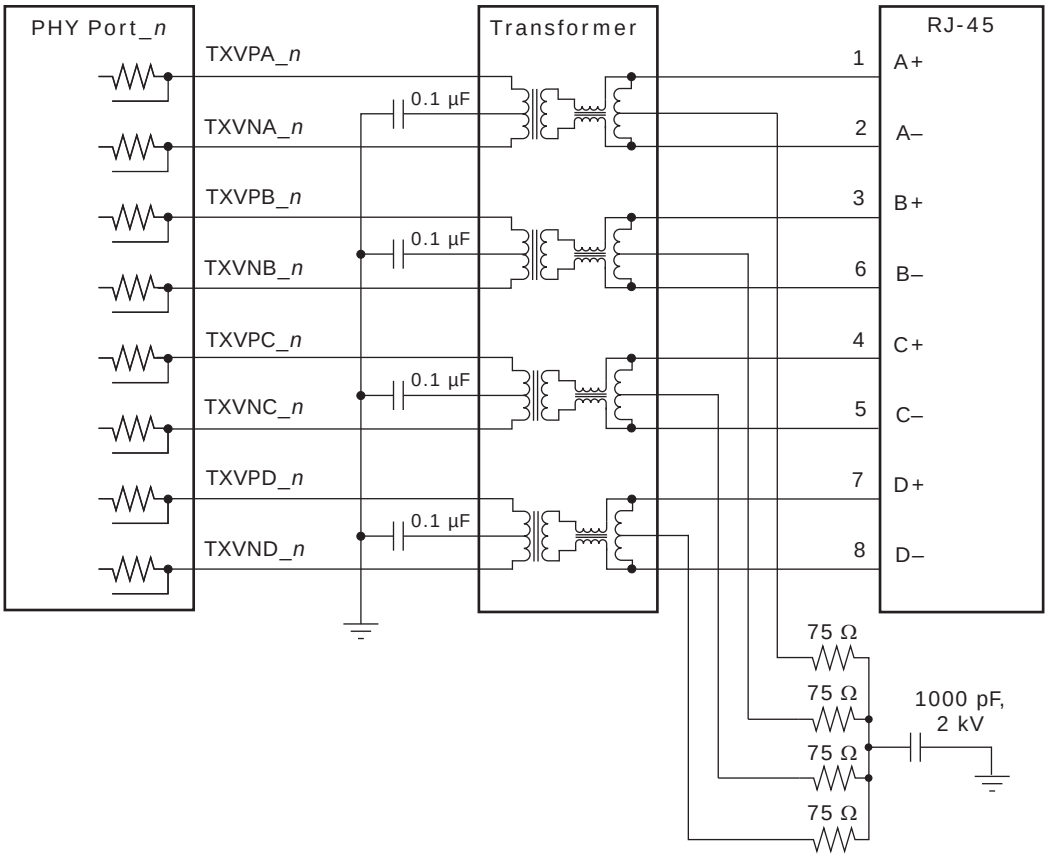
4.4 Cat5 Twisted Pair Media Interface

The VSC8522-02 twisted pair interface is compliant with IEEE 802.3-2008 and the IEEE 802.3az standard for Energy Efficient Ethernet.

4.4.1 Voltage-Mode Line Driver

Unlike many other gigabit PHYs, the VSC8522-02 uses a patented voltage-mode line driver that allows it to fully integrate the series termination resistors, which are required to connect the PHY's Cat5 interface to an external 1:1 transformer. Also, the interface does not require the user to place an external voltage on the center tap of the magnetic. The following illustration shows the connections.

Figure 4 • **Cat5 Media Interface**



4.4.2 Cat5 Autonegotiation and Parallel Detection

The VSC8522-02 supports twisted pair autonegotiation, as defined by IEEE 802.3-2008 Clause 28 and IEEE 802.3az. The autonegotiation process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, autonegotiation can determine speed, duplex configuration, and master or slave operating modes for 1000BASE-TX. Autonegotiation also enables a connected MAC to communicate with its link partner MAC through the VSC8522-02 using optional next pages, which set attributes that may not otherwise be defined by the IEEE standard.

If the Cat5 link partner does not support autonegotiation, the VSC8522-02 automatically uses parallel detection to select the appropriate link speed.

Autonegotiation is disabled by clearing register 0, bit 12. If autonegotiation is disabled, the state of register bits 0.6, 0.13, and 0.8 determine the device operating speed and duplex mode. Note that while 10BASE-T and 100BASE-T do not require autonegotiation, Clause 40 has defined 1000BASE-T to require autonegotiation.

4.4.3 1000BASE-T Forced Mode Support

VSC8522-02 provides support for a 1000BASE-T forced test mode. In this mode, the PHY can be forced into 1000BASE-T mode and does not require manual setting of master/slave at the two ends of the link. This mode is for test purposes only, and should not be used in normal operation. To configure a PHY in this mode, set register 17E2, bit 5 = 1 and register 0, bits 6 and 13 = 10.

4.4.4 Automatic Crossover and Polarity Detection

For trouble-free configuration and management of Ethernet links, the VSC8522-02 includes a robust automatic crossover detection feature for all three speeds on the twisted-pair interface (10BASE-T, 100BASE-T, and 1000BASE-T). Known as HP Auto-MDIX, the function is fully compliant with Clause 40 of IEEE 802.3-2008.

Additionally, the device detects and corrects polarity errors on all MDI pairs — a useful capability that exceeds the requirements of the standard.

Both HP Auto-MDIX detection and polarity correction are enabled in the device by default. Default settings can be changed using device register bits 18.5:4. Status bits for each of these functions are located in register 28.

Note: The VSC8522-02 can be configured to perform HP Auto-MDIX, even when autonegotiation is disabled and the link is forced into 10/100 speeds. To enable this feature, set register 18.7 to 0. To disable the feature, set register 0.12 to 0.

The HP Auto-MDIX algorithm successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in the following table.

Table 3 • **Supported MDI Pair Combinations**

1, 2	3, 6	4, 5	7, 8	Mode
A	B	C	D	Normal MDI
B	A	D	C	Normal MDI-X
A	B	D	C	Normal MDI with pair swap on C and D pair
B	A	C	D	Normal MDI-X with pair swap on C and D pair

4.4.5 Manual HP Auto-MDIX Setting

As an alternative to HP Auto-MDIX detection, the PHY can be forced to be MDI or MDI-X using register 19E1, bits 3:2. Setting these bits to 10 forces MDI and setting 11 forces MDI-X. Leaving the bits 00 enables the HP Auto-MDIX setting to be based on register 18, bits 7 and 5.

4.4.6 Link Speed Downshift

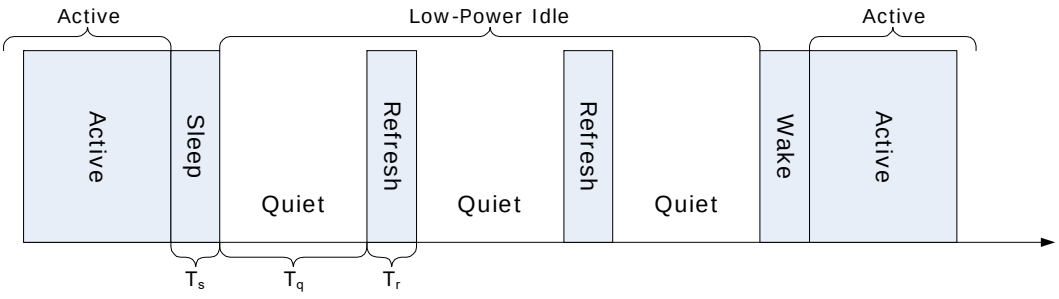
For operation in cabling environments that are incompatible with 1000BASE-T, the VSC8522-02 provides an automatic link speed downshift option. When enabled, the device automatically changes its 1000BASE-T autonegotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T. No reset is required to get out of this state if a subsequent link partner with 1000BASE-T support is connected. This feature is useful in setting up in networks using older cable installations that include only pairs A and B, and not pairs C and D.

To configure and monitor link speed downshifting, set register 20E1, bits 4:1. For more information, see Table 43, page 43.

4.4.7 Energy Efficient Ethernet

The VSC8522-02 supports the IEEE 802.3az Energy Efficient Ethernet standard that is currently in development. This new standard provides a method for reducing power consumption on an Ethernet link during times of low utilization. It uses low power idles (LPI) to achieve this objective.

Figure 5 • **Low Power Idle Operation**



Using LPI, the usage model for the link is to transmit data as fast as possible and then return to a low power idle state. Energy is saved on the link by cycling between active and low power idle states. During

LPI, power is reduced by turning off unused circuits and using this method, energy use scales with bandwidth utilization.

The VSC8522-02 uses LPI to optimize power dissipation in 100BASE-TX and 1000BASE-T modes of operation. In addition, the IEEE 802.3az standard defines a 10BASE-Te mode that reduces transmit signal amplitude from 5 V_{p-p} to ~3.3 V_{p-p}. This mode reduces power consumption in 10 Mbps link speed and fully interoperates with legacy 10BASE-T compliant PHYs over 100 m Cat5 cable or better.

To configure the VSC8522-02 in 10BASE-Te mode, set register 17E2.15 to 1 for each port. Additional Energy Efficient Ethernet features are controlled through Clause 45 registers. For more information, see Clause 45 Registers to Support Energy Efficient Ethernet, page 54.

4.5 Reference Clock

The device reference clock can be a 25 MHz, 125 MHz, or 156.25 MHz clock signal. It can be either a differential reference clock or a single-ended clock. However, 25 MHz single-ended operation is not recommended when using QSGMII due to the jitter specification requirements of this interface. For more information, see Reference Clock, page 58.

4.5.1 Configuring the REFCLK

There are three REFCLK_SEL pins to configure the REFCLK speed. The following table shows the functionality and associated REFCLK frequency.

Table 4 • **REFCLK Frequency Selection**

REFCLK_SEL2	REFCLK_SEL1	REFCLK_SEL0	REFCLK Frequency
0	0	0	125 MHz
0	0	1	156.25 MHz
1	0	0	25 MHz

4.5.2 Single-Ended REFCLK Input

To use a single-ended REFCLK, an external resistor network is required. The purpose of the network is to limit the amplitude and to adjust the center of the swing. The configurations for a single-ended REFCLK are shown in the following illustrations.

Figure 6 • **2.5 V CMOS Single-Ended REFCLK Input Resistor Network**

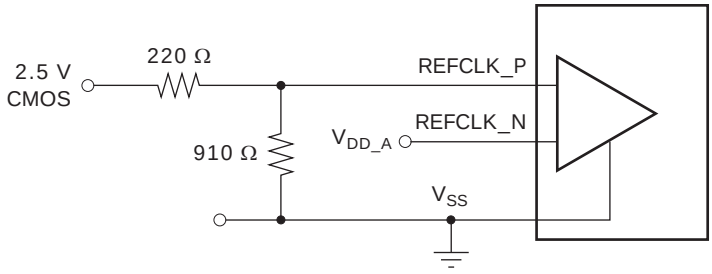
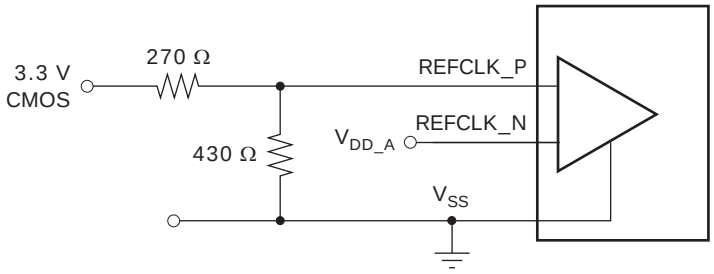


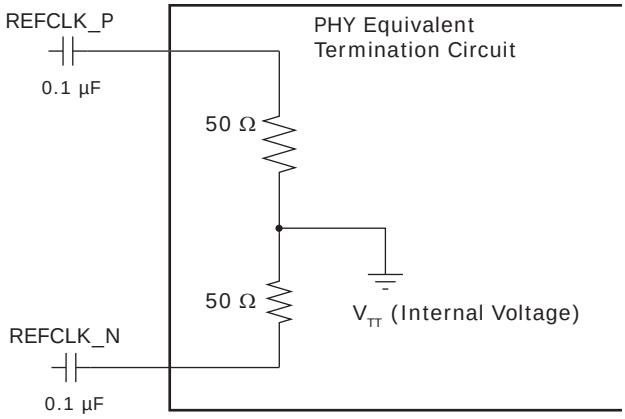
Figure 7 • **3.3 V CMOS Single-Ended REFCLK Input Resistor Network**



4.5.3 Differential REFCLK Input

AC-coupling is required when using a differential REFCLK. Differential clocks must be capacitively coupled and LVDS-compliant. The following illustration shows the configuration.

Figure 8 • **AC-Coupling Required for REFCLK Input**

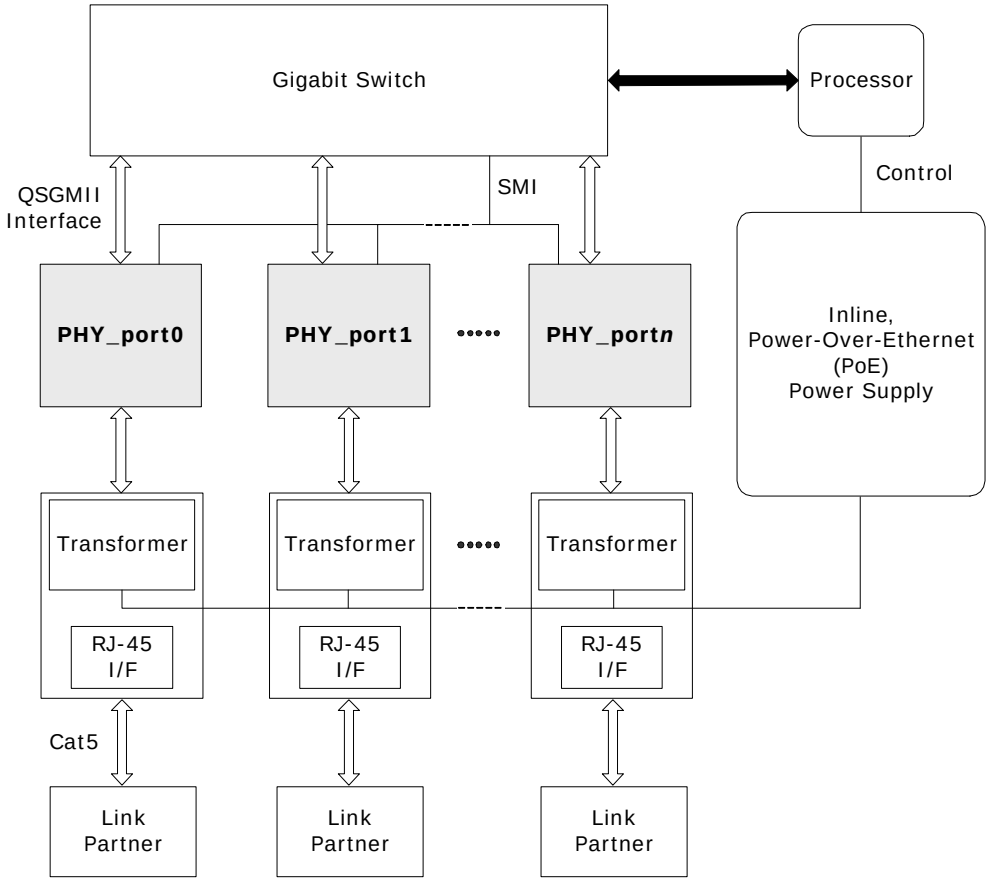


4.6 Ethernet Inline Powered Devices

The VSC8522-02 can detect legacy inline powered devices in Ethernet network applications. Inline powered detection capability is useful in systems that enable IP phones and other devices (such as wireless access points) to receive power directly from their Ethernet cable, similar to office digital phones receiving power from a private branch exchange (PBX) office switch over telephone cabling. This type of setup eliminates the need for an external power supply and enables the inline powered device to remain active during a power outage, assuming that the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, or other uninterruptable power source.

For more information about legacy inline powered device detection, visit the Cisco Web site at www.cisco.com. The following illustration shows an example of an inline powered Ethernet switch application.

Figure 9 • **Inline Powered Ethernet Switch Diagram**



The following procedure describes the process that an Ethernet switch must perform to process inline power requests made by a link partner (LP) that is, in turn, capable of receiving inline power:

1. Enable the inline powered device detection mode on each VSC8522-02 PHY using its serial management interface. Set register bit 23E1.10 to 1.
2. Ensure that the VSC8522-02 autonegotiation enable bit (register 0.12) is also set to 1. In the application, the device sends a special fast link pulse (FLP) signal to the LP. Reading register bit 23E1.9:8 returns 00 during the search for devices that require power over Ethernet (PoE).
3. The VSC8522-02 PHY monitors its inputs for the FLP signal looped back by the LP. An LP capable of receiving PoE loops back the FLP pulses when the LP is in a powered down state. This is reported when VSC8522-02 register bit 23E1.9:8 reads back 01. It can also be verified as an inline power detection interrupt by reading VSC8522-02 register bit 26.9, which should be a 1, and which is subsequently cleared and the interrupt de-asserted after the read. If an LP device does not loop back the FLP after a specific time, VSC8522-02 register bit 23E1.9:8 automatically resets to 10.
4. If the VSC8522-02 PHY reports that the LP requires PoE, the Ethernet switch must enable inline power on this port, externally of the PHY.
5. The PHY automatically disables inline powered device detection if the VSC8522-02 register bits 23E1.9:8 automatically resets to 10, and then automatically changes to its normal autonegotiation process. A link is then auto-negotiated and established when the link status bit is set (register bit 1.2 is set to 1).
6. In the event of a link failure (indicated when VSC8522-02 register bit 1.2 reads 0), the inline power should be disabled to the inline powered device external to the PHY. The VSC8522-02 PHY disables its normal autonegotiation process and re-enables its inline powered device detection mode.

4.7 IEEE 802.3af PoE Support

The VSC8522-02 is compatible with switch designs that are intended for use in systems that supply power to data terminal equipment (DTE) by means of the MDI or twisted pair cable, as described in IEEE 802.3af Clause 33.

4.8 ActiPHY Power Management

In addition to the IEEE-specified power-down control bit (device register bit 0.11), the device also includes an ActiPHY power management mode for each PHY. This mode enables support for power-sensitive applications. It utilizes a signal-detect function that monitors the media interface for the presence of a link to determine when to automatically power-down the PHY. The PHY wakes up at a programmable interval and attempts to wake up the link partner PHY by sending a burst of FLP over copper media.

The ActiPHY power management mode in the VSC8522-02 is enabled on a per-port basis during normal operation at any time by setting register bit 28.6 to 1.

The following operating states are possible when ActiPHY mode is enabled:

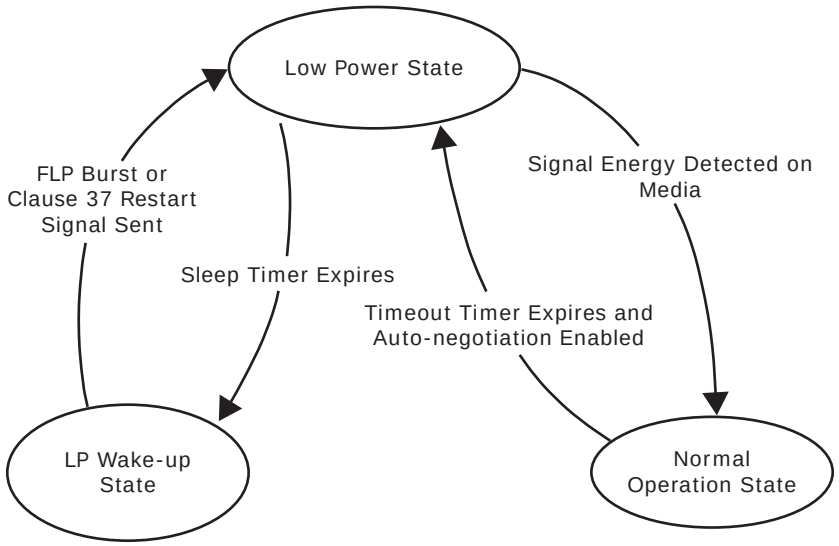
- Low power state
- LP wake-up state
- Normal operating state (link-up state)

The VSC8522-02 switches between the low power state and LP wake-up state at a programmable rate (the default is two seconds) until signal energy has been detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. If the PHY is in its normal operating state and the link fails, the PHY returns to the low power state after the expiration of the link status time-out timer. After reset, the PHY enters the low power state.

When autonegotiation is enabled in the PHY, the ActiPHY state machine operates as described. If autonegotiation is disabled and the link is forced to use 10BASE-T or 100BASE-TX modes while the PHY is in its low power state, the PHY continues to transition between the low power and LP wake-up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped. If autonegotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low power state.

The following illustration shows the relationship between ActiPHY states and timers.

Figure 10 • **ActiPHY State Diagram**



4.8.1 Low Power State

In the low power state, all major digital blocks are powered down. However, the following functionality is provided:

- SMI interface (MDC, MDIO, and MDINT pins)
- CLKOUT

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low power state and transitions to the normal operating state when signal energy is detected on the media. This happens when the PHY is connected to one of the following:

- Autonegotiation-capable link partner
- Another PHY in enhanced ActiPHY LP wake-up state

In the absence of signal energy on the media pins, the PHY periodically transitions from low-power state to LP wake-up state, based on the programmable sleep timer (register bits 20E1.14:13). The actual sleep time duration is randomized from –80 ms to 60 ms to avoid two linked PHYs in ActiPHY mode entering a lock-up state during operation.

4.8.2 Link Partner Wake-Up State

In the link partner wake-up state, the PHY attempts to wake up the link partner. Up to three complete FLP bursts are sent on alternating pairs A and B of the Cat5 media for a duration based on the wake-up timer, which is set using register bits 20E1.12:11.

In this state, the following functionality is provided:

- SMI interface (MDC, MDIO, and MDINT pins)
- CLKOUT

After sending signal energy on the relevant media, the PHY returns to the low power state.

4.8.3 Normal Operating State

In the normal operating state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration of the programmable link status time-out timer, which is set using register bit 28.7 and bit 28.2. It then enters the low power state.

4.9 Serial Management Interface

The VSC8522-02 device includes an IEEE 802.3-compliant serial management interface (SMI) that is affected by use of its MDC and MDIO pins. The SMI provides access to device control and status registers. The register set that controls the SMI consists of 32 16-bit registers, including all required IEEE-specified registers. Also, there are additional pages of registers accessible using device register 31.

Energy Efficient Ethernet control registers are available through the SMI using Clause 45 registers and Clause 22 register access in registers 13 through 14. For more information, see Table 22, page 32 and Table 67, page 54.

The SMI is a synchronous serial interface with input data to the VSC8522-02 on the MDIO pin that is clocked on the rising edge of the MDC pin. The output data is sent on the MDIO pin on the rising edge of the MDC signal. The interface can be clocked at a rate from 0 MHz to 12.5 MHz, depending on the total load on MDIO. An external 2-kΩ pull-up resistor is required on the MDIO pin.

4.9.1 SMI Frames

Data is transferred over the SMI using 32-bit frames with an optional, arbitrary-length preamble. Before the first frame can be sent, at least two clock pulses on MDC must be provided with the MDIO signal at logic one to initialize the SMI state machine. The following illustrations show the SMI frame format for read and write operations.

Figure 11 • **SMI Read Frame**

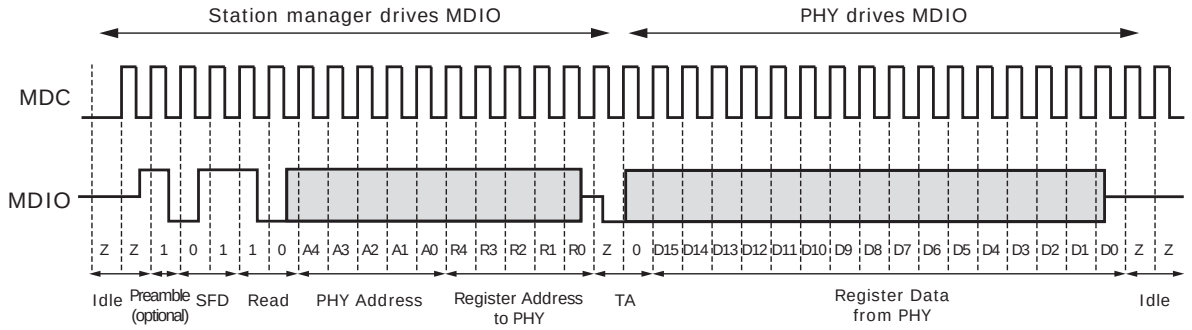
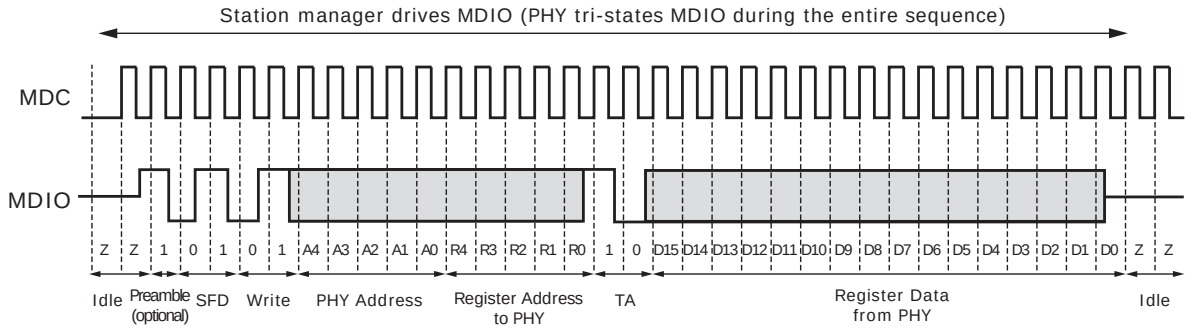


Figure 12 • **SMI Write Frame**



The following list provides additional information about the terms used in the SMI read and write timing diagrams.

4.9.1.1 Idle

During idle, the MDIO node goes to a high-impedance state. This allows an external pull-up resistor to pull the MDIO node up to a logical 1 state. Because the idle mode should not contain any transitions on MDIO, the number of bits is undefined during idle.

4.9.1.2 Preamble

By default, preambles are not expected or required. The preamble is a string of ones. If it exists, the preamble must be at least one bit; otherwise, it can be of an arbitrary length.

4.9.1.3 Start of Frame (SFD)

A pattern of 01 indicates the start of frame. If the pattern is not 01, all following bits are ignored until the next preamble pattern is detected.

4.9.1.4 Read or Write Opcode

A pattern of 10 indicates a read. A 01 pattern indicates a write. If the bits are not either 01 or 10, all following bits are ignored until the next preamble pattern is detected.

4.9.1.5 PHY Address

The particular VSC8522-02 responds to a message frame only when the received PHY address matches its physical address. The physical address is 5 bits long (4:0).

4.9.1.6 Register Address

The next five bits are the register address.

4.9.1.7 Turnaround

The two bits used to avoid signal contention when a read operation is performed on the MDIO are called the turnaround (TA) bits. During read operations, the VSC8522-02 drives the second TA bit, a logical 0.

4.9.1.8 Data

The 16-bits read from or written to the device are considered the data or data stream. When data is read from a PHY, it is valid at the output from one rising edge of MDC to the next rising edge of MDC. When data is written to the PHY, it must be valid around the rising edge of MDC.

4.9.1.9 Idle

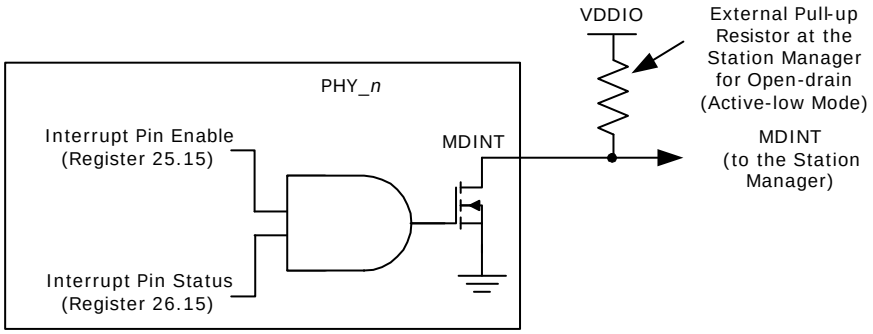
The sequence is repeated.

4.9.2 SMI Interrupt

The SMI includes an output interrupt signal, MDINT, for signaling the station manager when certain events occur in the VSC8522-02.

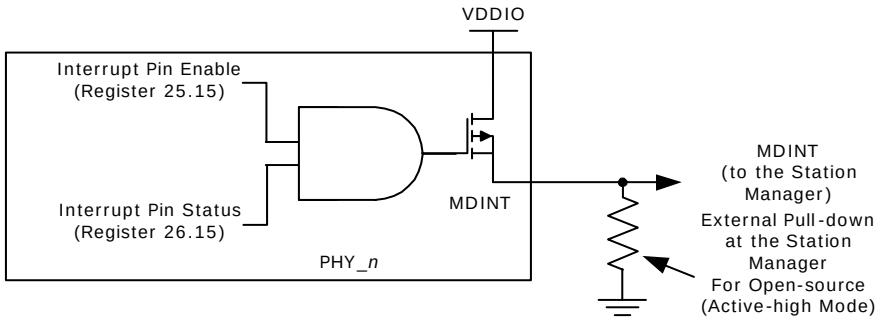
The MDINT pin can be configured for open-drain (active-low) by tying the pin to a pull-up resistor and to VDDIO. The following illustration shows this configuration.

Figure 13 • **MDINT Configured as an Open-Drain (Active-Low) Pin**



Alternatively, the MDINT pin can be configured for open-source (active-high) by tying the pin to a pull-down resistor and to VSS. The following illustration shows this configuration.

Figure 14 • **MDINT Configured as an Open-Source (Active-High) Pin**



When a PHY generates an interrupt, the MDINT pin is asserted (driven high or low, depending on resistor connection) if the interrupt pin enable bit (MII register 25.15) is set.

4.10 LED Interface

The VSC8522-02 outputs four LED signals per port (LED0, LED1, LED2, and LED3) through an enhanced serial LED mode. For more information, see Enhanced Serial LED Mode, page 17. The polarity of the LED outputs is programmable and can be changed through register 17E2.13:10. The default polarity is active low.

4.10.1 LED Modes

Each LED pin can be configured to display different status information that can be selected by setting the LED mode in register 29. The modes listed in the following table are equivalent to the setting used in register 29 to configure each LED pin. The default LED state is active low and can be changed by

modifying the value in register 17E2, bits 13:10. The blink/pulse-stretch is dependent on the LED behavior setting in register 30.

Table 5 • **LED Mode and Function Summary**

Mode	Function Name	LED State and Description
0	Link/Activity	1 = No link in any speed on any media interface. 0 = Valid link at any speed on any media interface. Blink or pulse-stretch = Valid link at any speed on any media interface with activity present.
1	Link1000/Activity	1 = No link in 1000BASE-T. 0 = Valid 1000BASE-T. Blink or pulse-stretch = Valid 1000BASE-T link with activity present.
2	Link100/Activity	1 = No link in 100BASE-TX. 0 = Valid 100BASE-TX. Blink or pulse-stretch = Valid 100BASE-TX link with activity present.
3	Link10/Activity	1 = No link in 10BASE-T. 0 = Valid 10BASE-T link. Blink or pulse-stretch = Valid 10BASE-T link with activity present.
4	Link100/1000/Activity	1 = No link in 100BASE-TX or 1000BASE-T. 0 = Valid 100BASE-TX or 1000BASE-T link. Blink or pulse-stretch = Valid 100BASE-TX or 1000BASE-T link with activity present.
5	Link10/1000/Activity	1 = No link in 10BASE-T or 1000BASE-T. 0 = Valid 10BASE-T or 1000BASE-T link. Blink or pulse-stretch = Valid 10BASE-T or 1000BASE-T link with activity present.
6	Link10/100/Activity	1 = No link in 10BASE-T, or 100BASE-TX. 0 = Valid 10BASE-T or 100BASE-TX, link. Blink or pulse-stretch = Valid 10BASE-T, or 100BASE-TX link with activity present.
7	Duplex/Collision	1 = Link established in half-duplex mode, or no link established. 0 = Link established in full-duplex mode. Blink or pulse-stretch = Link established in half-duplex mode but collisions are present.
8	Collision	1 = No collision detected. Blink or pulse-stretch = Collision detected.
9	Activity	1 = No activity present. Blink or pulse-stretch = Activity present (becomes TX activity present if register bit 30.14 is set to 1).
10	Autonegotiation Fault	1 = No autonegotiation fault present. 0 = Autonegotiation fault occurred.
11	Reserved	Reserved.
12	Force LED Off	1 = De-asserts the LED(1).
13	Force LED On	0 = Asserts the LED(1).

1. Setting this mode suppresses LED blinking after reset.

4.10.2 LED Behavior

Several LED behaviors can be programmed into the VSC8522-02. Use the settings in register 30 to program LED behavior, which includes the following:

4.10.2.1 LED Combine

Enables an LED to display the status for a combination of primary and secondary modes. This can be enabled or disabled for each LED pin. For example, a copper link running in 1000BASE-T mode and activity present can be displayed with one LED by configuring an LED pin to Link1000/Activity mode. The LED asserts when linked to a 1000BASE-T partner and also blinks or performs pulse-stretch when activity is either transmitted by the PHY or received by the Link Partner. When disabled, the combine feature only provides status of the selected primary function. In this example, only Link1000 asserts the LED, and the secondary mode, activity, does not display if the combine feature is disabled.

4.10.2.2 LED Blink or Pulse-Stretch

This behavior is used for activity and collision indication. This can be uniquely configured for each LED pin. Activity and collision events can occur randomly and intermittently throughout the link-up period. Blink is a 50% duty cycle oscillation of asserting and de-asserting an LED pin. Pulse-stretch guarantees that an LED is asserted and de-asserted for a specific period of time when activity is either present or not present. These rates can also be configured using a register setting.

4.10.2.3 Rate of LED Blink or Pulse-Stretch

This behavior controls the LED blink rate or pulse-stretch length when blink/pulse-stretch is enabled on an LED pin. The blink rate, which alternates between a high and low voltage level at a 50% duty cycle, can be set to 2.5 Hz, 5 Hz, 10 Hz, or 20 Hz. For pulse-stretch, the rate can be set to 50 ms, 100 ms, 200 ms, or 400 ms. The blink rate selection for PHY0 globally sets the rate used for all LED pins on all PHY ports.

4.10.2.4 LED Pulsing Enable

To provide additional power savings, the LEDs (when asserted) can be pulsed at 5 kHz, 20% duty cycle.

4.10.2.5 LED Blink After Reset

The LEDs will blink for one second after power-up and after any time all resets have been de-asserted. This can be disabled through register 19E1, bit 11 = 0.

4.10.2.6 Pulse Programmable Control

These bits add the ability to width and frequency of LED pulses. This feature facilities power reduction options.

4.10.3 Enhanced Serial LED Mode

VSC8522-02 can be configured to output up to four LED signals per port on a serial stream that can be de-serialized externally to drive LEDs on the system board. This functionality is controlled by setting register 25G, bits 7:1. In this mode, the serial LED_DATA is shifted out on the falling edge of LED_CLK and is latched in the external serial to parallel converter on the rising edge of LED_CLK. The falling edge of LED_LD signal can be used to shift the data from the shift register in the converter to the parallel output drive register. If a separate parallel output drive register is not used in the external serial to parallel converter, then the LEDs will blink at a high frequency as the data bits are being shifted through which may be undesirable. The LED_PULSE signal provides a 5 kHz pulse stream whose duty cycle can be modulated to turn on/off LEDs at a high rate. This signal can be tied to the output enable signal of the serial to parallel converter to provide the LED dimming functionality to save energy.

4.11 GPIO Pins

The VSC8522-02 provides nine multiplexed multipurpose pins. For more information about the available GPIO pins, see LED and Multi/General Purpose Input and Output Pins, page 99, and for information about configuring them, see General Purpose Registers, page 50.

4.12 Testing Features

The VSC8522-02 device includes several testing features designed to facilitate performing system-level debugging and in-system production testing. This section describes the available features.

4.12.1 Ethernet Packet Generator

The Ethernet packet generator (EPG) can be used at each of the 10/100/1000BASE-T speed settings for copper Cat5 media to isolate problems between the MAC and the VSC8522-02, or between a locally connected PHY and its remote link partner. Enabling the EPG feature effectively disables all MAC interface transmit pins and selects the EPG as the source for all data transmitted onto the twisted pair interface.

Important The EPG is intended for use with laboratory or in-system testing equipment only. Do not use the EPG testing feature when the VSC8522-02 is connected to a live network.

To enable the VSC8522-02 EPG feature, set the device register bit 29E1.15 to 1.

When the EPG is enabled, packet loss occurs during transmission of packets from the MAC to the PHY. However, the PHY receive output pins to the MAC are still active when the EPG is enabled. If it is necessary to disable the MAC receive pins as well, set the register bit 0.10 to 1.

When the device register bit 29E1.14 is set to 1, the PHY begins transmitting Ethernet packets based on the settings in registers 29E1 and 30E1. These registers set:

- Source and destination addresses for each packet
- Packet size
- Inter-packet gap
- FCS state
- Transmit duration
- Payload pattern

If register bit 29E1.13 is set to 0, register bit 29E1.14 is cleared automatically after 30,000,000 packets are transmitted.

4.12.2 CRC Counters

A set of cyclical redundancy check (CRC) counters is available in all PHYs in VSC8522-02 to monitor traffic on the copper interface.

The device CRC counters operate in 10/100/1000BASE-T mode as follows:

- After receiving a packet on the media interface, register bit 15 in register 18E1 or register 28E3 is set and cleared after being read.
- The packet then is counted by either the good CRC counter or the bad CRC counter.
- Both CRC counters are also automatically cleared when read.

The good CRC counter's highest value is 9,999 packets. After this value is reached, the counter clears on the 10,000th packet and continues to count additional packets beyond that value. The bad CRC counter stops counting when it reaches its maximum counter limit of 255 packets.

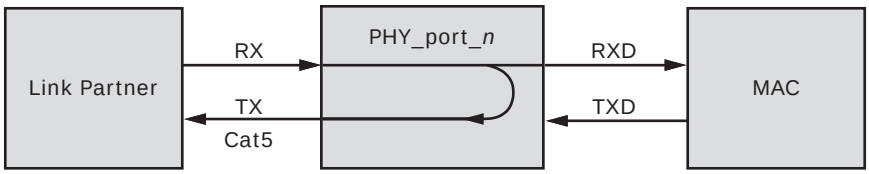
4.12.2.1 Copper Interface CRC Counters

Two separate CRC counters are available and reside between the copper interface PCSs and SerDes MAC interface. There is a 14-bit good CRC counter available through register bits 18E1.13:0 and a separate 8-bit bad CRC counter available in register bits 23E1.7:0.

4.12.3 Far-End Loopback

The far-end loopback testing feature is enabled by setting register bit 23.3 to 1. When enabled, it forces incoming data from a link partner on the current media interface, into the MAC interface of the PHY, to be retransmitted back to the link partner on the media interface as shown in the following illustration. In addition, the incoming data also appears on the receive data pins of the MAC interface. Data present on the transmit data pins of the MAC interface is ignored when using this testing feature.

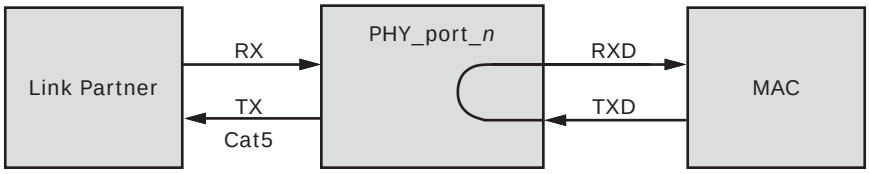
Figure 15 • **Far-End Loopback Diagram**



4.12.4 Near-End Loopback

When the near-end loopback testing feature is enabled, transmitted data (TXD) is looped back in the PCS block onto the receive data signals (RXD), as shown in the following illustration. When using this testing feature, no data is transmitted over the network. To enable near-end loopback, set the device register bit 0.14 to 1.

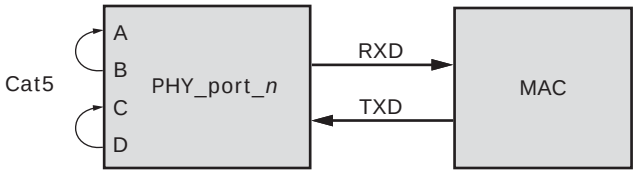
Figure 16 • **Near-End Loopback Diagram**



4.12.5 Connector Loopback

The connector loopback testing feature allows the twisted pair interface to be looped back externally. When using this feature, the PHY must be connected to a loopback connector or a loopback cable. Pair A should be connected to pair B, and pair C to pair D, as shown in the following illustration. The connector loopback feature functions at all available interface speeds.

Figure 17 • **Connector Loopback Diagram**



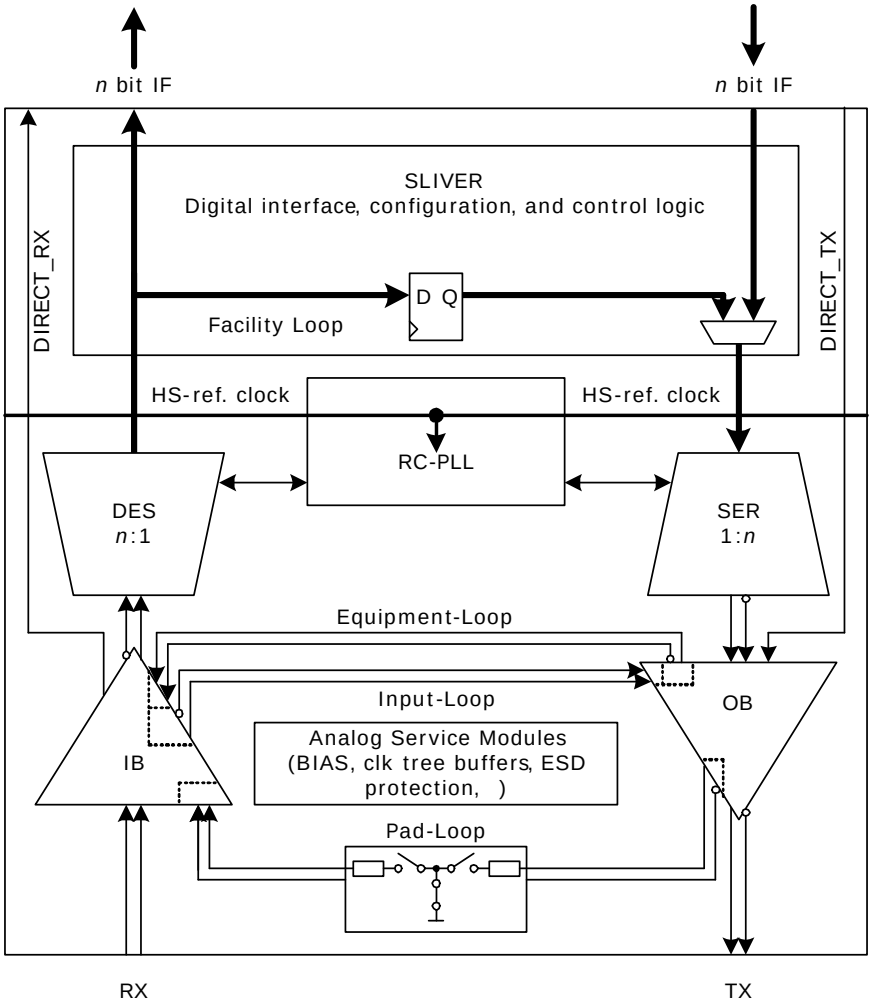
When using the connector loopback testing feature, the device autonegotiation, speed, and duplex configuration is set using device registers 0, 4, and 9. For 1000BASE-T connector loopback, the following additional writes are required. Execute the additional writes in the following order:

1. Enable the 1000BASE-T connector loopback. Set register bit 24.0 to 1.
2. Disable pair swap correction. Set register bit 18.5 to 1.

4.12.6 SerDes Loopbacks

For test purposes, the enhanced SerDes macro interfaces provide several data loops. The following illustration shows the SerDes loopbacks.

Figure 18 • **Data Loops of the SerDes Macro**



4.12.6.1 QSGMII Mode

When the MAC interface is configured in QSGMII mode, write the following 16-bit value to register 18G:

Bits 15:12 0x9

Bits 11:8: Port address (0xC to 0xE)

Bits 7:4: Loopback type

Bits 3:0: 0x2

where loopback type is:

0x0: No loopback

0x1: Pad loopback

0x2: Input loopback

0x4: Facility loopback

0x8: Equipment loopback

and port addresses (bits 11:8) are:

0xC: Enhanced SerDes macro for ports 0–3

0xD: Enhanced SerDes macro for ports 4–7

0xE: Enhanced SerDes macro for ports 8-11

Note: Loopback configuration affects all four ports associated with a QSGMII. Individual port loopback within a QSGMII is not possible.

4.12.6.2 Facility Loop

The recovered and de-multiplexer deserializer data output is looped back to the serializer data input and replaces the data delivered by the digital core. This test loop provides the possibility to test the complete analog macro data path from outside including input buffer, clock and data recovery, serialization and output buffer. The data received by the input buffer must be transmitted by the output buffer after some delay.

Additional configuration of the Enhanced SerDes macro is required for facility loopback mode. When entering facility loopback mode, the set = 1 option should be run; when exiting facility loopback mode, the set = 0 option should be run. The following software script must be executed after running the command to enable/disable facility loopback mode.

```
PhyWrite(PhyBaseAddr, 31, 0x0010);
PhyWrite(PhyBaseAddr, 18, 0x8s13);
// where "s" is the physical address of the SerDes macro
PhyWrite(PhyBaseAddr, 18, 0xd7d3);
PhyWrite(PhyBaseAddr, 18, 0x8007);
tmp1 = PhyRead(PhyBaseAddr, 18);
tmp2 = tmp1 & 0x0ff0;
if (set)
    tmp3 = tmp2 | 0x0100;
else
    tmp3 = tmp2 & 0x0ef0;
tmp4 = tmp3 | 0x8006;
PhyWrite(PhyBaseAddr, 18, tmp4);
PhyWrite(PhyBaseAddr, 18, 0x9p40);
// where "p" is the logical address of the SGMII or QSGMII interface
```

PhyBaseAddr is the base address of the internal PHYs and is equal to 0, 12, 4, or 20 based on the value of the PHYADD4 and PHYADD3 pins. For more information, see Table 1, page 6.

The value of *s* is 1–3 and corresponds to the physical address of the enhanced SerDes macro. The value of *p* is 0–2 and is the logical address of the QSGMII lane that corresponds to the enhanced SerDes macro with physical address *s*. For more information about address mapping, see Table 2, page 6.

4.12.6.2.1 Equipment Loop

The 1-bit data stream at the serializer output is looped back to the deserializer and replaces the received data stream from the input buffer. This test loop provides the possibility to verify the digital data path internally. The transmit data goes through the serialization, the clock and data recovery and deserialization before the data is fed back to the digital core.

4.12.6.2.2 Input Loop

The received 1-bit data stream of the input buffer is looped back asynchronously to the output buffer. This test loop provides the possibility to the test only the analog parts of the QSGMII interface because only the input and output buffer are part of this loop.

4.12.6.2.3 Pad Loop

The 1-bit data stream at the output buffer output is looped back to the input buffer input and added to the differential pad signal. Therefore, the input pad should not be driven when the output loop is activated. The test loop provides a means to test the complete QSGMII macro data path, including the input and output buffers.

4.12.7 VeriPHY Cable Diagnostics

The VSC8522-02 includes a comprehensive suite of cable diagnostic functions that are available using SMI reads and writes. These functions enable a variety of cable operating conditions and status to be accessed and checked. The VeriPHY suite has the ability to identify the cable length and operating conditions and to isolate a variety of common faults that can occur on Cat5 twisted pair cabling.

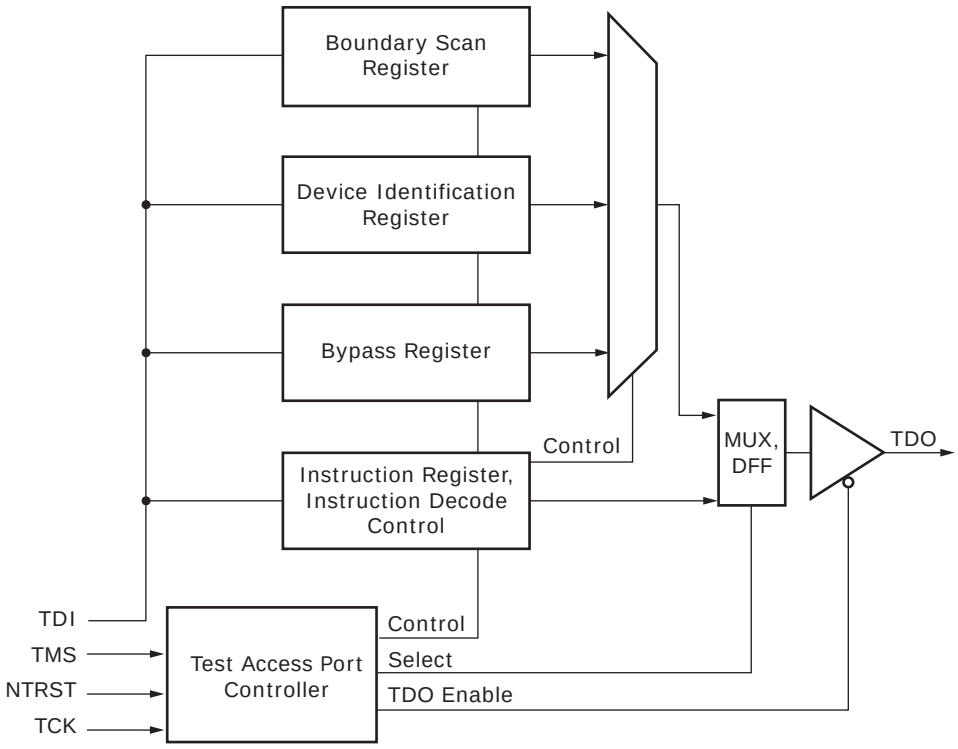
For functional details of the VeriPHY suite and the operating instructions, see the ENT-AN0125 PHY, Integrated PHY-Switch VeriPHY - Cable Diagnostics application note.

4.12.8 JTAG Boundary Scan

The VSC8522-02 supports the test access port (TAP) and boundary scan architecture described in IEEE 1149.1. The device includes an IEEE 1149.1-compliant test interface, referred to as a JTAG TAP interface.

The JTAG boundary scan logic on the VSC8522-02, accessed using its TAP interface, consists of a boundary scan register and other logic control blocks. The TAP controller includes all IEEE-required signals (TMS, TCK, TDI, and TDO), in addition to the optional asynchronous reset signal NTRST. The following illustration shows the TAP and boundary scan architecture.

Figure 19 • **Test Access Port and Boundary Scan Architecture**



After a TAP reset, the device identification register is serially connected between TDI and TDO by default. The TAP instruction register is loaded either from a shift register when a new instruction is shifted in, or, if there is no new instruction in the shift register, a default value of 6'b100100 (IDCODE) is loaded. Using this method, there is always a valid code in the instruction register, and the problem of toggling instruction bits during a shift is avoided. Unused codes are mapped to the BYPASS instruction.

4.12.9 JTAG Instruction Codes

The VSC8522-02 supports the following instruction codes:

4.12.9.1 EXTEST

Allows tests of the off-chip circuitry and board-level interconnections by sampling input pins and loading data onto output pins. Outputs are driven by the contents of the boundary-scan cells, which have to be updated with valid values, with the PRELOAD instruction, prior to the EXTEST instruction.

4.12.9.2 SAMPLE/PRELOAD

Allows a snapshot of inputs and outputs during normal system operation to be taken and examined. It also allows data values to be loaded into the boundary-scan cells prior to the selection of other boundary-scan test instructions.

4.12.9.3 IDCODE

Provides the version number (bits 31:28), device family ID (bits 27:12), and the manufacturer identity (bits 11:1) to be serially read from the device.

The following table provides information about the meaning of IDCODE binary values stored in the device JTAG registers.

Table 6 • **IDCODE JTAG Device Identification Register Descriptions**

Description	Device Version	Family ID	Manufacturing Identity	LSB
Bit field	31–28	27–12	11–1	0
Binary value	0000	1011 0000 0000 0001	000 0111 0100	1

4.12.9.4 USERCODE

Provides the version number (bits 31:28), part number (bits 27:12), and the manufacturer identity (bits 11:1) to be serially read from the device. The following table provides information about the meaning of USERCODE binary values stored in the device JTAG registers.

Table 7 • **USERCODE JTAG Device Identification Register Descriptions**

Description	Device Version	Model Number	Manufacturing Identity	LSB
Bit field	31–28	27–12	11–1	0
Binary value	0010	1000 0101 0010 0010	000 0111 0100	1

4.12.9.5 CLAMP

Allows the state of the signals driven from the component pins to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. While the CLAMP instruction is selected, the signals driven from the component pins do not change.

4.12.9.6 HIGHZ

Places the component in a state in which all of its system logic outputs are placed in a high-impedance state. In this state, an in-circuit test system can drive signals onto the connections normally driven by a component output without incurring a risk of damage to the component. This makes it possible to use a board where not all of the components are compatible with the IEEE 1149.1 standard.

4.12.9.7 BYPASS

The bypass register contains a single shift-register stage and is used to provide a minimum-length serial path (one TCK clock period) between TDI and TDO to bypass the device when no test operation is required.

The following table provides information about the location and IEEE compliance of the JTAG instruction codes used in the VSC8522-02. Instructions not explicitly listed in the table are reserved. For more information about these IEEE specifications, visit the IEEE Web site at www.IEEE.org.

Table 8 • **JTAG Interface Instruction Codes**

Instruction	Code	Selected Register	Register Width	IEEE 1149.1	IEEE 1149.6
EXTEST	6'b000000	Boundary-Scan	161	Mandatory	
SAMPLE/PRELOAD	6'b000001	Boundary-Scan	161	Mandatory	
IDCODE	6'b100100	Device Identification	32	Optional	
USERCODE	6'b100101	Device Identification	32	Optional	
CLAMP	6'b000010	Bypass Register	1	Optional	
HIGHZ	6'b000101	Bypass Register	1	Optional	
BYPASS	6'b111111	Bypass Register	1	Mandatory	
EXTEST_PULSE	6'b000011	Boundary-Scan Register	161		Mandatory
EXTEST_TRAIN	6'b000100	Boundary-Scan Register	161		Mandatory

4.12.10 Boundary Scan Register Cell Order

All inputs and outputs are observed in the boundary scan register cells. All outputs are additionally driven by the contents of boundary scan register cells. Bidirectional pins have all three related boundary scan register cells: input, output, and control.

The complete boundary scan cell order is available as a BSDL file format on the Microsemi Web site at www.microsemi.com.

4.12.11 JTAG Boundary Scan Interface

The IEEE 1149.6 AC-JTAG solution integrated on all SerDes ports of the VSC8522-02 extends the capability of IEEE 1149.1 boundary scan for robust board-level testing. This interface is backward-compatible to the IEEE 1149.1 standard.

4.13 Configuration

The VSC8522-02 can be configured by setting internal memory registers using the management interface.

5 Registers

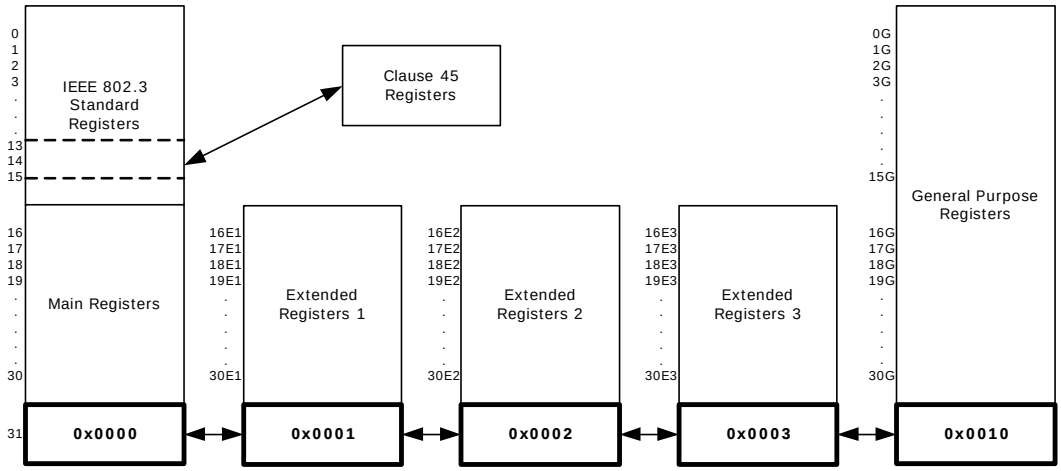
This section provides information about how to configure the VSC8522-02 using its internal memory registers and the management interface.

The VSC8522-02 uses several different types of registers:

- IEEE Clause 22 device registers with addresses from 0 to 31
- Three pages of extended registers with addresses from 16E1–30E1, 16E2–30E2, and 16E3–30E3
- General-purpose registers with addresses from 0G to 30G
- IEEE Clause 45 devices registers accessible through the Clause 22 registers 13 and 14 to support IEEE 802.3az Energy Efficient Ethernet registers

The following illustration shows the relationship between the device registers and their address spaces.

Figure 20 • **Register Space Diagram**



- Reserved Registers—For main registers 16–31, extended registers 16E1–30E1, 16E2–30E2, 16E3–30E3, and general purpose registers 0G–30G, any bits marked as Reserved should be processed as read-only and their states as undefined.
- Reserved Bits—In writing to registers with reserved bits, use a read-modify-then-write technique, where the entire register is read but only the intended bits to be changed are modified. Reserved bits cannot be changed and their read state cannot be considered static or unchanging.

5.1 IEEE Standard and Main Registers

In the VSC8522-02, the page space of the standard registers consists of the IEEE standard registers and the Microsemi standard registers. The following table lists the names of the registers associated with the addresses as dictated by the IEEE standard.

Table 9 • **IEEE 802.3 Standard Registers**

Address	Name
0	Mode Control
1	Mode Status
2	PHY Identifier 1
3	PHY Identifier 2
4	Autonegotiation Advertisement
5	Autonegotiation Link Partner Ability
6	Autonegotiation Expansion

Table 9 • **IEEE 802.3 Standard Registers *(continued)***

Address	Name
7	Autonegotiation Next-Page Transmit
8	Autonegotiation Link Partner Next-Page Receive
9	1000BASE-T Control
10	1000BASE-T Status
11–12	Reserved
13	Clause 45 access registers from IEEE 802.3 Table 22-6 and 22.24.3.11-12 and Annex 22D
14	Clause 45 access registers from IEEE 802.3 Table 22-6 and 22.24.3.11-12 and Annex 22D
15	1000BASE-T Status Extension 1

The following table lists the names of the registers in the main page space of the device. These registers are accessible only when register address 31 is set to 0x0000.

Table 10 • **Main Registers**

Address	Name
16	100BASE-TX Status Extension 1
17	1000BASE-T Status Extension 2
18	Bypass Control
19	Error Counter 1
20	Error Counter 2
21	Error Counter 3
22	Extended Control and Status
23	Extended PHY Control 1
24	Extended PHY Control 2
25	Interrupt Mask
26	Interrupt Status
27	Reserved
28	Auxiliary Control and Status
29	LED Mode Select
30	LED Behavior
31	Extended Register Page Access

5.1.1 Mode Control

The device register at memory address 0 controls several aspects of VSC8522-02 functionality. The following table shows the available bit settings in this register and what they control.

Table 11 • **Mode Control, Address 0 (0x00)**

Bit	Name	Access	Description	Default
15	Software reset	R/W	Self-clearing. Restores all serial management interface (SMI) registers to default state, except for sticky and super-sticky bits. 1: Reset asserted. 0: Reset de-asserted. Wait [X] after setting this bit to initiate another SMI register access.	0
14	Loopback	R/W	1: Loopback enabled. 0: Loopback disabled. When loop back is enabled, the device functions at the current speed setting and with the current duplex mode setting (bits 6, 8, and 13 of this register).	0
13	Forced speed selection LSB	R/W	Least significant bit. MSB is bit 6. 00: 10 Mbps. 01: 100 Mbps. 10: 1000 Mbps. 11: Reserved.	0
12	Autonegotiation enable	R/W	1: Autonegotiation enabled. 0: Autonegotiation disabled.	1
11	Power-down	R/W	1: Power-down enabled.	0
10	Isolate	R/W	1: Disable MAC interface outputs and ignore MAC interface inputs.	0
9	Restart autonegotiation	R/W	Self-clearing bit. 1: Restart autonegotiation on media interface.	0
8	Duplex	R/W	1: Full-duplex. 0: Half-duplex.	0
7	Collision test enable	R/W	1: Collision test enabled.	0
6	Forced speed selection MSB	R/W	Most significant bit. LSB is bit 13. 00: 10 Mbps. 01: 100 Mbps. 10: 1000 Mbps. 11: Reserved.	10
5:0	Reserved	RO	Reserved.	All zeros

5.1.2 Mode Status

The register at address 1 in the device main registers space allows you to read the currently enabled mode setting. The following table shows possible readouts of this register.

Table 12 • **Mode Status, Address 1 (0x01)**

Bit	Name	Access	Description	Default
15	100BASE-T4 capability	RO	1: 100BASE-T4 capable.	0
14	100BASE-TX FDX capability	RO	1: 100BASE-TX FDX capable.	1
13	100BASE-TX HDX capability	RO	1: 100BASE-TX HDX capable.	1
12	10BASE-T FDX capability	RO	1: 10BASE-T FDX capable.	1
11	10BASE-T HDX capability	RO	1: 10BASE-T HDX capable.	1
10	100BASE-T2 FDX capability	RO	1: 100BASE-T2 FDX capable.	0
9	100BASE-T2 HDX capability	RO	1: 100BASE-T2 HDX capable.	0
8	Extended status enable	RO	1: Extended status information present in register 15.	1
7	Reserved	RO	**Note:** Reserved.	1
6	Preamble suppression capability	RO	1: MF preamble can be suppressed. 0: MF required.	1
5	Autonegotiation complete	RO	1: Autonegotiation complete.	0
4	Remote fault	RO	Latches high. 1: Far-end fault detected.	0
3	Autonegotiation capability	RO	1: Autonegotiation capable.	1
2	Link status	RO	Latches low. 1: Link is up.	0
1	Jabber detect	RO	Latches high. 1: Jabber condition detected.	0
0	Extended capability	RO	1: Extended register capable.	1

5.1.3 Device Identification

All 16 bits in both register 2 and register 3 in the VSC8522-02 are used to provide information associated with aspects of the device identification. The following tables list the expected readouts.

Table 13 • **Identifier 1, Address 2 (0x02)**

Bit	Name	Access	Description	Default
15:0	Organizationally unique identifier (OUI)	RO	OUI most significant bits (3:18)	0×0007

Table 14 • **Identifier 2, Address 3 (0x03)**

Bit	Name	Access	Description	Default
15:10	OUI	RO	OUI least significant bits (19:24)	000001
9:4	Microsemi model number	RO	VSC8522-02 (0x2f)	101111
3:0	Device revision number	RO		0011

5.1.4 Autonegotiation Advertisement

The bits in address 4 in the main registers space control the VSC8522-02 ability to notify other devices of the status of its autonegotiation feature. The following table shows the available settings and readouts.

Table 15 • **Device Autonegotiation Advertisement, Address 4 (0x04)**

Bit	Name	Access	Description	Default
15	Next page transmission request	R/W	1: Request enabled	0
14	Reserved	RO	Reserved	0
13	Transmit remote fault	R/W	1: Enabled	0
12	Reserved	R/W	Reserved	0
11	Advertise asymmetric pause	R/W	1: Advertises asymmetric pause	0
10	Advertise symmetric pause	R/W	1: Advertises symmetric pause	0
9	Advertise100BASE-T4	R/W	1: Advertises 100BASE-T4	0
8	Advertise100BASE-TX FDX	R/W	1: Advertise 100BASE-TX FDX	1
7	Advertise100BASE-TX HDX	R/W	1: Advertises 100BASE-TX HDX	1
6	Advertise10BASE-T FDX	R/W	1: Advertises 10BASE-T FDX	1
5	Advertise10BASE-T HDX	R/W	1: Advertises 10BASE-T HDX	1
4:0	Advertise selector	R/W		00001

5.1.5 Link Partner Autonegotiation Capability

The bits in main register 5 can be used to determine if the Cat5 link partner (LP) used with the VSC8522-02 is compatible with the autonegotiation functionality.

Table 16 • **Autonegotiation Link Partner Ability, Address 5 (0x05)**

Bit	Name	Access	Description	Default
15	LP next page transmission request	RO	1: Requested	0
14	LP acknowledge	RO	1: Acknowledge	0
13	LP remote fault	RO	1: Remote fault	0
12	Reserved	RO	Reserved	0
11	LP advertise asymmetric pause	RO	1: Capable of asymmetric pause	0
10	LP advertise symmetric pause	RO	1: Capable of symmetric pause	0
9	LP advertise 100BASE-T4	RO	1: Capable of 100BASE-T4	0
8	LP advertise 100BASE-TX FDX	RO	1: Capable of 100BASE-TX FDX	0
7	LP advertise 100BASE-TX HDX	RO	1: Capable of 100BASE-TX HDX	0
6	LP advertise 10BASE-T FDX	RO	1: Capable of 10BASE-T FDX	0
5	LP advertise 10BASE-T HDX	RO	1: Capable of 10BASE-T HDX	0
4:0	LP advertise selector	RO		00000

5.1.6 Autonegotiation Expansion

The bits in main register 6 work together with those in register 5 to indicate the status of the LP autonegotiation functioning. The following table shows the available settings and readouts.

Table 17 • **Autonegotiation Expansion, Address 6 (0x06)**

Bit	Name	Access	Description	Default
15:5	Reserved	RO	Reserved.	All zeros
4	Parallel detection fault	RO	This bit latches high. 1: Parallel detection fault.	0
3	LP next page capable	RO	1: LP is next page capable.	0
2	Local PHY next page capable	RO	1: Local PHY is next page capable.	1
1	Page received	RO	This bit latches low. 1: New page is received.	0
0	LP is autonegotiation capable	RO	1: LP is capable of autonegotiation.	0

5.1.7 Transmit Autonegotiation Next Page

The settings in register 7 in the main registers space provide information about the number of pages in an autonegotiation sequence. The following table shows the settings available.

Table 18 • **Autonegotiation Next Page Transmit, Address 7 (0x07)**

Bit	Name	Access	Description	Default
15	Next page	R/W	1: More pages follow	0
14	Reserved	RO	Reserved	0
13	Message page	R/W	1: Message page 0: Unformatted page	1
12	Acknowledge 2	R/W	1: Complies with request 0: Cannot comply with request	0
11	Toggle	RO	1: Previous transmitted LCW = 0 0: Previous transmitted LCW = 1	0
10:0	Message/unformatted code	R/W		00000000001

5.1.8 Autonegotiation Link Partner Next Page Receive

The bits in register 8 of the main register space work together with register 7 to determine certain aspects of the LP autonegotiation. The following table shows the possible readouts.

Table 19 • **Autonegotiation LP Next Page Receive, Address 8 (0x08)**

Bit	Name	Access	Description	Default
15	LP next page	RO	1: More pages follow	0
14	Acknowledge	RO	1: LP acknowledge	0
13	LP message page	RO	1: Message page 0: Unformatted page	0
12	LP acknowledge 2	RO	1: LP complies with request	0
11	LP toggle	RO	1: Previous transmitted LCW = 0 0: Previous transmitted LCW = 1	0
10:0	LP message/unformatted code	RO		All zeros

5.1.9 1000BASE-T Control

The VSC8522-02's 1000BASE-T functionality is controlled by the bits in register 9 of the main register space. The following table shows the settings and readouts available.

Table 20 • **1000BASE-T Control, Address 9 (0x09)**

Bit	Name	Access	Description	Default
15:13	Transmitter test mode	R/W	000: Normal. 001: Mode 1: Transmit waveform test. 010: Mode 2: Transmit jitter test as master. 011: Mode 3: Transmit jitter test as slave. 100: Mode 4: Transmitter distortion test. 101–111: Reserved	000
12	Master/slave manual configuration	R/W	1: Master/slave manual configuration enabled.	0
11	Master/slave value	R/W	This register is only valid when bit 9.12 is set to 1. 1: Configure PHY as master during negotiation. 0: Configure PHY as slave during negotiation.	0
10	Port type	R/W	1: Multi-port device. 0: Single-port device.	1
9	1000BASE-T FDX capability	R/W	1: PHY is 1000BASE-T FDX capable.	1
8	1000BASE-T HDX capability	R/W	1: PHY is 1000BASE-T HDX capable.	1
7:0	Reserved	R/W	Reserved.	0x00

Note: Transmitter test mode (bits 15:13) operates in the manner described in IEEE 802.3 section 40.6.1.1.2. When using any of the transmitter test modes, the automatic media-sense feature must be disabled. For more information, see Extended PHY Control 2, page 37.

5.1.10 1000BASE-T Status

The bits in register 10 of the main register space can be read to obtain the status of the 1000BASE-T communications enabled in the device. The following table shows the readouts.

Table 21 • **1000BASE-T Status, Address 10 (0x0A)**

Bit	Name	Access	Description	Default
15	Master/slave configuration fault	RO	This bit latches high. 1: Master/slave configuration fault detected. 0: No master/slave configuration fault detected.	0
14	Master/slave configuration resolution	RO	1: Local PHY configuration resolved to master. 0: Local PHY configuration resolved to slave.	1
13	Local receiver status	RO	1: Local receiver is operating normally.	0
12	Remote receiver status	RO	1: Remote receiver OK.	0
11	LP 1000BASE-T FDX capability	RO	1: LP 1000BASE-T FDX capable.	0
10	LP 1000BASE-T HDX capability	RO	1: LP 1000BASE-T HDX capable.	0

Table 21 • **1000BASE-T Status, Address 10 (0x0A) *(continued)***

Bit	Name	Access	Description	Default
9:8	Reserved	RO	Reserved.	00
7:0	Idle error count	RO	Self-clearing register.	0x00

5.1.11 MMD Access Control Register

The bits in register 13 of the main register space are a window to the EEE registers as defined in IEEE 802.3az Clause 45.

Table 22 • **MMD EEE Access, Address 13 (0x0D)**

Bit	Name	Access	Description
15:14	Function	R/W	00: Address 01: Data, no post increment 10: Data, post increment for read and write 11: Data, post increment for write only
13:5	Reserved	R/W	Reserved
4:0	DVAD	R/W	Device address as defined in IEEE 802.3az table 45-1

5.1.12 MMD Address or Data Register

The bits in register 14 of the main register space are a window to the EEE registers as defined in IEEE 802.3az Clause 45.

Table 23 • **MMD Address or Data Register, Address 14 (0x0E)**

Bit	Name	Access	Description
15:0	Register Address/Data	R/W	If register 13.15:14 = 2'b00, address of register of the device that is specified by 13.4:0. Otherwise, the data to be written to or read from the register.

5.1.13 1000BASE-T Status Extension 1

Register 15 provides additional information about the operation of the device 1000BASE-T communications. The following table shows the readouts available.

Table 24 • **1000BASE-T Status Extension 1, Address 15 (0x0F)**

Bit	Name	Access	Description	Default
15	1000BASE-X FDX capability	RO	1: PHY is 1000BASE-X FDX capable	0
14	1000BASE-X HDX capability	RO	1: PHY is 1000BASE-X HDX capable	0
13	1000BASE-T FDX capability	RO	1: PHY is 1000BASE-T FDX capable	1
12	1000BASE-T HDX capability	RO	1: PHY is 1000BASE-T HDX capable	1
11:0	Reserved	RO	Reserved	0x000

5.1.14 100BASE-TX Status Extension

Register 16 in the main registers page space of the VSC8522-02 provides additional information about the status of the device's 100BASE-TX operation.

Table 25 • **100BASE-TX Status Extension, Address 16 (0x10)**

Bit	Name	Access	Description	Default
15	100BASE-TX Descrambler	RO	1: Descrambler locked.	0
14	100BASE-TX lock error	RO	Self-clearing bit. 1: Lock error detected.	0
13	100BASE-TX disconnect state	RO	Self-clearing bit. 1: PHY 100BASE-TX link disconnect detected.	0
12	100BASE-TX current link status	RO	1: PHY 100BASE-TX link active.	0
11	100BASE-TX receive error	RO	Self-clearing bit. 1: Receive error detected.	0
10	100BASE-TX transmit error	RO	Self-clearing bit. 1: Transmit error detected.	0
9	100BASE-TX SSD error	RO	Self-clearing bit. 1: Start-of-stream delimiter error detected.	0
8	100BASE-TX ESD error	RO	Self-clearing bit. 1: End-of-stream delimiter error detected.	0
7:0	Reserved	RO	Reserved	

5.1.15 1000BASE-T Status Extension 2

The second status extension register is at address 17 in the device main registers space. It provides information about another set of parameters associated with 1000BASE-T communications. For information about the first status extension register, see Table 24, page 32.

Table 26 • **1000BASE-T Status Extension 2, Address 17 (0x11)**

Bit	Name	Access	Description	Default
15	1000BASE-T descrambler	RO	1: Descrambler locked.	0
14	1000BASE-T lock error	RO	Self-clearing bit. 1: Lock error detected.	0
13	1000BASE-T disconnect state	RO	Self-clearing bit. 1: PHY 1000BASE-T link disconnect detected.	0
12	1000BASE-T current link status	RO	1: PHY 1000BASE-T link active.	0
11	1000BASE-T receive error	RO	Self-clearing bit. 1: Receive error detected.	0
10	1000BASE-T transmit error	RO	Self-clearing bit. 1: Transmit error detected.	0
9	1000BASE-T SSD error	RO	Self-clearing bit. 1: Start-of-stream delimiter error detected.	0

Table 26 • **1000BASE-T Status Extension 2, Address 17 (0x11) *(continued)***

Bit	Name	Access	Description	Default
8	1000BASE-T ESD error	RO	Self-clearing bit. 1: End-of-stream delimiter error detected.	0
7	1000BASE-T carrier extension error	RO	Self-clearing bit. 1: Carrier extension error detected.	0
6	Non-compliant BCM5400 detected	RO	1: Non-compliant BCM5400 link partner detected.	0
5	MDI crossover error	RO	1: MDI crossover error was detected.	0
4:0	Reserved	RO	Reserved	

5.1.16 Bypass Control

The bits in this register control aspects of functionality in effect when the device is disabled for the purpose of traffic bypass. The following table shows the settings available.

Table 27 • **Bypass Control, Address 18 (0x12)**

Bit	Name	Access	Description	Default
15	Transmit disable	R/W	1: PHY transmitter disabled.	0
14	4B5B encoder/decoder	R/W	1: Bypass 4B/5B encoder/decoder.	0
13	Scrambler	R/W	1: Bypass scrambler.	0
12	De-scrambler	R/W	1: Bypass de-scrambler.	0
11	PCS receive	R/W	1: Bypass PCS receiver.	0
10	PCS transmit	R/W	1: Bypass PSC transmit.	0
9	LFI timer	R/W	1: Bypass Link Fail Inhibit (LFI) timer.	0
8	Reserved	RO	Reserved.	
7	HP Auto-MDIX at forced 10/100	R/W	Sticky bit. 1: Disable HP Auto-MDIX at forced 10/100 speeds.	1
6	Non-compliant BCM5400 detect disable	R/W	Sticky bit. 1: Disable non-compliant BCM5400 detection.	0
5	Disable pair swap correction (HP Auto-MDIX when autonegotiation enabled)	R/W	Sticky bit. 1: Disable the automatic pair swap correction.	0
4	Disable polarity correction	R/W	Sticky bit. 1: Disable polarity inversion correction on each subchannel.	0
3	Parallel detect control	R/W	Sticky bit. 1: Do not ignore advertised ability. 0: Ignore advertised ability.	1
2	Pulse shaping filter	R/W	1: Disable pulse shaping filter	0
1	Disable automatic 1000BASE-T next page exchange	R/W	Sticky bit. 1: Disable automatic 1000BASE-T next page exchanges.	0

Table 27 • **Bypass Control, Address 18 (0x12) *(continued)***

Bit	Name	Access	Description	Default
0	Reserved	RO	Reserved.	

Note: If bit 18.1 is set to 1 in this register, automatic exchange of next pages is disabled, and control is returned to the user through the SMI after the base page is exchanged. The user then must send the correct sequence of next pages to the link partner, determine the common capabilities, and force the device into the correct configuration following the successful exchange of pages.

5.1.17 Error Counter 1

The bits in register 19 provide an error counter. The following table shows the settings available.

Table 28 • **Extended Control and Status, Address 19 (0x13)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	
7:0	100/1000BASE-TX receive error counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

5.1.18 Error Counter 2

The bits in register 20 provide an error counter. The following table shows the settings available.

Table 29 • **Extended Control and Status, Address 20 (0x14)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	
7:0	100/1000BASE-TX false carrier counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

5.1.19 Error Counter 3

The bits in register 21 provide an error counter. The following table shows the settings available.

Table 30 • **Extended Control and Status, Address 21 (0x15)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	
7:0	Copper media link disconnect counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

5.1.20 Extended Control and Status

The bits in register 22 provide additional device control and readouts. The following table shows the settings available.

Table 31 • **Extended Control and Status, Address 22 (0x16)**

Bit	Name	Access	Description	Default
15	Force 10BASE-T link high	R/W	Sticky bit. 1: Bypass link integrity test. 0: Enable link integrity test.	0
14	Jabber detect disable	R/W	Sticky bit. 1: Disable jabber detect.	0

Table 31 • **Extended Control and Status, Address 22 (0x16) *(continued)***

Bit	Name	Access	Description	Default
13	Disable 10BASE-T echo	R/W	Sticky bit. 1: Disable 10BASE-T echo.	1
12	Disable SQE mode	R/W	Sticky bit. 1: Disable SQE mode.	1
11:10	10BASE-T squelch control	R/W	Sticky bit. 00: Normal squelch. 01: Low squelch. 10: High squelch. 11: Reserved.	00
9	Sticky reset enable	R/W	Super-sticky bit. 1: Enabled.	1
8	EOF Error	RO	This bit is self-clearing. 1: EOF error detected.	0
7	10BASE-T disconnect state	RO	This bit is self-clearing. 1: 10BASE-T link disconnect detected.	0
6	10BASE-T link status	RO	1: 10BASE-T link active.	0
5:1	Reserved	RO	Reserved.	
0	SMI broadcast write	R/W	Sticky bit. 1: Enabled.	0

The following information applies to the extended control and status bits:

- When bit 22.15 is set, the link integrity state machine is bypassed and the PHY is forced into a link pass status.
- When bits 22.11:10 are set to 00, the squelch threshold levels are based on the IEEE standard for 10BASE-T. When set to 01, the squelch level is decreased, which can improve the bit error rate performance on long loops. When set to 10, the squelch level is increased and can improve the bit error rate in high-noise environments.
- When bit 22.9 is set, all sticky register bits retain their values during a software reset. Clearing this bit causes all sticky register bits to change to their default values upon software reset. Super-sticky bits retain their values upon software reset regardless of the setting of bit 22.9.
- When bit 22.0 is set, if a write to any PHY register (registers 0–31, including extended registers), the same write is broadcast to all PHYs. For example, if bit 22.0 is set to 1 and a write to PHY0 is executed (register 0 is set to 0x1040), all PHYs' register 0s are set to 0x1040. Disabling this bit restores normal PHY write operation. Reads are still possible when this bit is set, but the value that is read corresponds only to the particular PHY being addressed.

5.2 Extended PHY Control 1

The following table shows the settings available.

Table 32 • **Extended PHY Control 1, Address 23 (0x17)**

Bit	Name	Access	Description	Default
15:13	Reserved	RO	Reserved.	110
12	Reserved	R/W	Reserved.	0
11:4	Reserved	RO	Reserved.	0
3	Far-end loopback mode	R/W	1: Enabled.	0
2:0	Reserved	RO	Reserved.	

5.2.1 Extended PHY Control 2

The second set of extended controls is located in register 24 in the main register space for the device. The following table shows the settings and readouts available.

Table 33 • **Extended PHY Control 2, Address 24 (0x18)**

Bit	Name	Access	Description	Default
15:13	100BASE-TX edge rate control	R/W	Sticky bit. 011: +5 Edge rate (slowest). 010: +4 Edge rate. 001: +3 Edge rate. 000: +2 Edge rate. 111: +1 Edge rate. 110: Default edge rate. 101: –1 Edge rate. 100: –2 Edge rate (fastest).	000
12	PICMG 2.16 reduced power mode	R/W	Sticky bit. 1: Enabled.	0
11:6	Reserved	RO	Reserved.	
5:4	Jumbo packet mode	R/W	Sticky bit. 00: Normal IEEE 1.5 kB packet length. 01: 9 kB jumbo packet length (12 kB with 60 ppm or better reference clock). 10: 12 kB jumbo packet length (16 kB with 70 ppm or better reference clock). 11: Reserved.	00
3:1	Reserved	RO	Reserved.	
0	1000BASE-T connector loopback	R/W	1: Enabled.	0

Note: When bits 5:4 are set to jumbo packet mode, the default maximum packet values are based on 100 ppm driven reference clock to the device. Controlling the ppm offset between the MAC and the PHY as specified in the bit description results in a higher jumbo packet length.

5.2.2 Interrupt Mask

These bits control the device interrupt mask. The following table shows the settings available.

Table 34 • **Interrupt Mask, Address 25 (0x19)**

Bit	Name	Access	Description	Default
15	MDINT interrupt status enable	R/W	Sticky bit. 1: Enabled.	0
14	Speed state change mask	R/W	Sticky bit. 1: Enabled.	0
13	Link state change mask	R/W	Sticky bit. 1: Enabled.	0
12	FDX state change mask	R/W	Sticky bit. 1: Enabled.	0
11	Autonegotiation error mask	R/W	Sticky bit. 1: Enabled.	0
10	Autonegotiation complete mask	R/W	Sticky bit. 1: Enabled.	0

Table 34 • **Interrupt Mask, Address 25 (0x19) *(continued)***

Bit	Name	Access	Description	Default
9	Inline powered device (PoE) detect mask	R/W	Sticky bit. 1: Enabled.	0
8	Symbol error interrupt mask	R/W	Sticky bit. 1: Enabled.	0
7	Reserved	RO	Reserved.	0
6	TX FIFO over/underflow interrupt mask	R/W	Sticky bit. 1: Enabled.	0
5	RX FIFO over/underflow interrupt mask	R/W	Sticky bit. 1: Enabled.	0
4	AMS media changed mask	R/W	Sticky bit. 1: Enabled.	0
3	False-carrier interrupt mask	R/W	Sticky bit. 1: Enabled.	0
2	Link speed downshift detect mask	R/W	Sticky bit. 1: Enabled.	0
1	Master/Slave resolution error mask	R/W	Sticky bit. 1: Enabled.	0
0	RX_ER interrupt mask	R/W	Sticky bit. 1: Enabled.	0

Note: When bit 25.15 is set, the MDINT pin is enabled. When enabled, the state of this pin reflects the state of bit 26.15. Clearing this bit only inhibits the MDINT pin from being asserted. Also, before enabling this bit, read register 26 to clear any previously inactive interrupts pending that will cause bit 25.15 to be set.

5.2.3 Interrupt Status

The status of interrupts already written to the device are available for reading from register 26 in the main registers space. The following table shows the expected readouts.

Table 35 • **Interrupt Status, Address 26 (0x1A)**

Bit	Name	Access	Description	Default
15	Interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
14	Speed state change status	RO	Self-clearing bit. 1: Interrupt pending.	0
13	Link state change status	RO	Self-clearing bit. 1: Interrupt pending.	0
12	FDX state change status	RO	Self-clearing bit. 1: Interrupt pending.	0
11	Autonegotiation error status	RO	Self-clearing bit. 1: Interrupt pending.	0
10	Autonegotiation complete status	RO	Self-clearing bit. 1: Interrupt pending.	0
9	Inline powered device detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
8	Symbol error status	RO	Self-clearing bit. 1: Interrupt pending.	0

Table 35 • **Interrupt Status, Address 26 (0x1A)** ***(continued)***

Bit	Name	Access	Description	Default
7	Fast link failure detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
6	TX FIFO over/underflow detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
5	RX FIFO over/underflow detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
4	AMS media changed mask	RO	Self-clearing bit. 1: Interrupt pending.	0
3	False-carrier interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
2	Link speed downshift detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
1	Master/Slave resolution error status	RO	Self-clearing bit. 1: Interrupt pending.	0
0	RX_ER interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0

The following information applies to the interrupt status bits:

- All set bits in this register are cleared after being read (self-clearing). If bit 26.15 is set, the cause of the interrupt can be read by reading bits 26.14:0.
- For bits 26.14 and 26.12, bit 0.12 must be set for this interrupt to assert.
- For bit 26.2, bits 4.8:5 must be set for this interrupt to assert.
- For bit 26.0, this interrupt will not occur when RX_ER is used for carrier-extension decoding of a link partner's data transmission.

5.2.4 Device Auxiliary Control and Status

Register 28 provides control and status information for several device functions not controlled or monitored by other device registers. The following table shows the settings available and the expected readouts.

Table 36 • **Auxiliary Control and Status, Address 28 (0x1C)**

Bit	Name	Access	Description	Default
15	Autonegotiation complete	RO	Duplicate of bit 1.5.	0
14	Autonegotiation disabled	RO	Inverted duplicate of bit 0.12.	0
13	HP Auto-MDIX crossover indication	RO	1: HP Auto-MDIX crossover performed internally.	0
12	CD pair swap	RO	1: CD pairs are swapped.	0
11	A polarity inversion	RO	1: Polarity swap on pair A.	0
10	B polarity inversion	RO	1: Polarity swap on pair B.	0
9	C polarity inversion	RO	1: Polarity swap on pair C.	0
8	D polarity inversion	RO	1: Polarity swap on pair D.	0

Table 36 • **Auxiliary Control and Status, Address 28 (0x1C) *(continued)***

Bit	Name	Access	Description	Default
7	ActiPHY link status time-out control [1]	R/W	Sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB. 00: 1 second. 01: 2 seconds. 10: 3 seconds. 11: 4 seconds.	0
6	ActiPHY mode enable	R/W	Sticky bit. 1: Enabled.	0
5	FDX status	RO	1: Full-duplex. 0: Half-duplex.	00
4:3	Speed status	RO	00: Speed is 10BASE-T. 01: Speed is 100BASE-TX. 10: Speed is 1000BASE-T. 11: Reserved.	0
2	ActiPHY link status time-out control [0]	R/W	Sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB. 00: 1 second. 01: 2 seconds. 10: 3 seconds. 11: 4 seconds.	1
1:0	Media mode status	RO	00: No media selected. 01: Reserved. 10: SerDes media selected. 11: Reserved.	00

5.2.5 LED Mode Select

The device LED outputs are controlled using the bits in register 29 of the main register space. The following table shows the information needed to access the functionality of each of the outputs.

Table 37 • **LED Mode Select, Address 29 (0x1D)**

Bit	Name	Access	Description	Default
15:12	LED3 mode select	R/W	Sticky bit. Select from LED modes 0–15.	1000
11:8	LED2 mode select	R/W	Sticky bit. Select from LED modes 0–15.	0000
7:4	LED1 mode select	R/W	Sticky bit. Select from LED modes 0–15.	0010
3:0	LED0 mode select	R/W	Sticky bit. Select from LED modes 0–15.	0001

5.2.6 LED Behavior

The bits in register 30 control and enable you to read the status of the pulse or blink rate of the device LEDs. The following table shows the settings you can write to the register or read from the register.

Table 38 • **LED Behavior, Address 30 (0x1E)**

Bit	Name	Access	Description	Default
15:13	Reserved	RO	Reserved.	

Table 38 • **LED Behavior, Address 30 (0x1E) *(continued)***

Bit	Name	Access	Description	Default
12	LED pulsing enable	R/W	Sticky bit. 0: Normal operation. 1: LEDs pulse with a 5 kHz, programmable duty cycle when active.	0
11:10	LED blink/pulse-stretch rate	R/W	Sticky bit. 00: 2.5 Hz blink rate/400 ms pulse-stretch. 01: 5 Hz blink rate/200 ms pulse-stretch. 10: 10 Hz blink rate/100 ms pulse-stretch. 11: 20 Hz blink rate/50 ms pulse-stretch. The blink rate selection for PHY0 globally sets the rate used for all LED pins on all PHY ports.	01
9:0	Reserved	RO	Reserved.	

Note: Bits 30.11:10 are active only in port 0 and affect the behavior of LEDs for all the ports.

5.2.7 Extended Page Access

To provide functionality beyond the IEEE 802.3-specified registers and main device registers, the VSC8522-02 includes an extended set of registers that provide an additional 15 register spaces.

The register at address 31 controls the access to the extended registers for the VSC8522-02. Accessing the GPIO page register space is similar to accessing the extended page registers. The following table shows the settings available.

Table 39 • **Extended/GPIO Page Access, Address 31 (0x1F)**

Bit	Name	Access	Description	Default
15:0	Extended/GPIO page register access	R/W	0x0000: Register 16–30 accesses main register space. Writing 0x0000 to register 31 restores the main register access. 0x0001: Register 16–30 accesses extended register space 1 0x0002: Register 16–30 accesses extended register space 2 0x0003: Register 16–30 accesses extended register space 3 0x0010: Register 0–30 accesses GPIO register space	0x0000

5.3 Extended Page 1 Registers

To access the extended page 1 registers (16E1–30E1), enable extended register access by writing 0x0001 to register 31. Writing 0x0000 to register 31 restores the main register access.

When extended page 1 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E1–30E1 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Table 40 • **Extended Registers Page 1 Space**

Address	Name
16E1–17E1	Reserved
18E1	Cu Media CRC Good Counter
19E1	Extended Mode Control (LED blink control and MDI control)

Table 40 • **Extended Registers Page 1 Space *(continued)***

Address	Name
20E1	Extended PHY Control 3 (ActiPHY)
21E1–22E1	Reserved
23E1	Extended PHY Control 4 (PoE and CRC error counter)
27E1–28E1	Reserved
29E1	Ethernet Packet Generator (EPG) Control 1
30E1	EPG Control 2

5.3.1 Cu Media CRC Good Counter

Register 18E1 makes it possible to read the contents of the CRC good counter for packets that are received on the Cu media interface; the number of CRC routines that have executed successfully. The following table shows the expected readouts.

Table 41 • **Cu Media CRC Good Counter, Address 18E1 (0x12)**

Bit	Name	Access	Description	Default
15	Packet since last read	RO	Self-clearing bit. 1: Packet received since last read.	0
14	Reserved	RO	Reserved.	
13:0	Cu Media CRC good counter contents	RO	Self-clearing counter containing the number of packets with valid CRCs modulo 10,000. This counter does not saturate and will roll over to 0 on the next good packet received after 9,999.	0x0000

5.3.2 Extended Mode Control

Register 19E1 controls the extended LED and other chip modes. The following table shows the settings available.

Table 42 • **Extended Mode Control, Address 19E1 (0x13)**

Bit	Name	Access	Description	Default
15:12	Reserved	RO	Reserved.	0
11	LED Reset Blink Suppress	R/W	1: Blink LEDs after COMA_MODE is deasserted. 0: Suppress LED blink after COMA_MODE is deasserted.	0
10:4	Reserved	RO	Reserved	0
3:2	Force MDI crossover	R/W	00: Normal HP Auto-MDIX operation. 01: Reserved. 10: Copper media forced to MDI. 11: Copper media forced MDI-X.	00
1:0	Reserved	RO	Reserved	

5.3.3 ActiPHY Control

Register 20E1 controls the device ActiPHY sleep timer, its wake-up timer, the frequency of the CLKOUT signal, and its link speed downshifting feature. The following table shows the settings available.

Table 43 • **Extended PHY Control 3, Address 20E1 (0x14)**

Bit	Name	Access	Description	Default
15	Disable carrier extension	R/W	1: Disable carrier extension in SGMII-1000BASE-T copper links.	1
14:13	ActiPHY sleep timer	R/W	Sticky bit. 00: 1 second. 01: 2 seconds. 10: 3 seconds. 11: 4 seconds.	01
12:11	ActiPHY wake-up timer	R/W	Sticky bit. 00: 160 ms. 01: 400 ms. 10: 800 ms. 11: 2 seconds.	00
10	Reserved	RO	Reserved	
9	PHY address reversal	R/W	1: Enabled	Address
8	Reserved	RO	Valid only on PHY0.	
7:6	Media mode status	RO	00: No media selected. 01: Copper media selected. 10: SerDes media selected. 11: Reserved.	00
5	Enable 10BASE-T no preamble mode	R/W	Sticky bit. 1: 10BASE-T will assert RX_DV indication when data is presented to the receiver even without a preamble preceding it.	0
4	Enable link speed auto-downshift feature	R/W	Sticky bit. 1: Enable auto link speed downshift from 1000BASE-T.	0
3:2	Link speed auto downshift control	R/W	Sticky bit. 00: Downshift after 2 failed 1000BASE-T autonegotiation attempts. 01: Downshift after 3 failed 1000BASE-T autonegotiation attempts. 10: Downshift after 4 failed 1000BASE-T autonegotiation attempts. 11: Downshift after 5 failed 1000BASE-T autonegotiation attempts.	01
1	Link speed auto downshift status	RO	0: No downshift. 1: Downshift is required or has occurred.	0
0	Reserved	RO	Reserved	

5.3.4 PoE and Miscellaneous Functionality

The register at address 23E1 controls various aspects of inline powering and the CRC error counter in the VSC8522-02.

Table 44 • **Extended PHY Control 4, Address 23E1 (0x17)**

Bit	Name	Access	Description	Default
15:11	PHY address	RO	PHY address; latched on reset.	
10	Inline powered device detection	R/W	Sticky bit. 1: Enabled.	0
9:8	Inline powered device detection status	RO	Only valid when bit 10 is set. 00: Searching for devices. 01: Device found; requires inline power. 10: Device found; does not require inline power. 11: Reserved.	00
7:0	Cu Media CRC error counter	RO	Self-clearing bit. RC error counter for packets received on the Cu media interface. The value saturates at 0xFF and subsequently clears when read and restarts count.	0x00

5.3.5 Ethernet Packet Generator Control 1

The EPG control register provides access to and control of various aspects of the EPG testing feature. There are two separate EPG control registers. The following table shows the settings available in the first register.

Table 45 • **EPG Control 1, Address 29E1 (0x1D)**

Bit	Name	Access	Description	Default
15	EPG enable	R/W	1: Enable EPG	0
14	EPG run or stop	R/W	1: Run EPG	0
13	Transmission duration	R/W	1: Continuous (sends in 10,000-packet increments) 0: Send 30,000,000 packets and stop	0
12:11	Packet length	R/W	00: 125 bytes 01: 64 bytes 10: 1518 bytes 11: 10,000 bytes (jumbo packet)	0
10	Inter-packet gap	R/W	1: 8,192 ns 0: 96 ns	0
9:6	Destination address	R/W	Lowest nibble of the 6-byte destination address	0001
5:2	Source address	R/W	Lowest nibble of the 6-byte destination address	0000
1	Payload type	R/W	1: Randomly generated payload pattern 0: Fixed based on payload pattern	0
0	Bad frame check sequence (FCS) generation	R/W	1: Generate packets with bad FCS 0: Generate packets with good FCS	0

The following information applies to the EPG control number 1:

- Do not run the EPG when the VSC8522-02 is connected to a live network.
- Bit 29E1.13 (continuous EPG mode control): When enabled, this mode causes the device to send continuous packets. When disabled, the device continues to send packets only until it reaches the next 10,000-packet increment mark. It then ceases to send packets.
- The 6-byte destination address in bits 9:6 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- The 6-byte source address in bits 5:2 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- If any of bits 13:0 are changed while the EPG is running (bit 14 is set to 1), bit 14 must be cleared and then set back to 1 for the change to take effect and to restart the EPG.

5.3.6 Ethernet Packet Generator Control 2

Register 30E1 consists of the second set of bits that provide access to and control over the various aspects of the EPG testing feature. The following table shows the settings available.

Table 46 • **EPG Control 2, Address 30E1 (0x1E)**

Bit	Name	Access	Description	Default
15:0	EPG packet payload	R/W	Data pattern repeated in the payload of packets generated by the EPG	0x00

Note: If any of bits 15:0 in this register are changed while the EPG is running (bit 14 of register 29E1 is set to 1), that bit (29E1.14) must first be cleared and then set back to 1 for the change to take effect and to restart the EPG.

5.4 Extended Page 2 Registers

To access the extended page 2 registers (16E2–30E2), enable extended register access by writing 0x0002 to register 31. For more information, see Table 39, page 41.

When extended page 2 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E2–30E2 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Writing 0x0000 to register 31 restores the main register access.

The following table lists the addresses and register names in the extended register page 2 space. These registers are accessible only when the device register 31 is set to 0x0002.

Table 47 • **Extended Registers Page 2 Space**

Address	Name
16E2	Cu PMD Transmit Control
17E2	EEE Control
18E2–30E2	Reserved

5.4.1 Cu PMD Transmit Control

The register at address 16E2 consists of the bits that provide control over the amplitude settings for the transmit side Cu PMD interface. These bits provide the ability to make small adjustments in the signal amplitude to compensate for minor variations in the magnetics from different vendors. Extreme caution must be exercised when changing these settings from the default values as they have a direct impact on

the signal quality. Changing these settings also affects the linearity and harmonic distortion of the transmitted signals. Contact Microsemi for further help with changing these values.

Table 48 • **Cu PMD Transmit Control, Address 16E2 (0x10)**

Bit	Name	Access	Description	Default
15:12	1000BASE-T signal amplitude trim	R/W	Change 1000BASE-T signal amplitude	0000
11:8	100BASE-TX signal amplitude trim	R/W	Change 100BASE-TX signal amplitude	0010
7:4	10BASE-T signal amplitude trim	R/W	Change 10BASE-T signal amplitude	1111
3:0	10BASE-Te signal amplitude trim	R/W	Change 10BASE-Te signal amplitude	0000

5.4.2 EEE Control

The register at address 17E2 consists of the bits that provide additional control over the chip behavior in Energy Efficient Ethernet (IEEE 802.3az) mode for debug and to allow interoperation with legacy MACs that do not support IEEE 802.3az.

Table 49 • **EEE Control, Address 17E2 (0x11)**

Bit	Name	Access	Description	Default
15	Enable 10BASE-Te	R/W	Enable Energy Efficient (IEEE 802.3az) 10BASE-Te operating mode.	0
14	Reserved	RO	Reserved.	0
13:10	Invert LED polarity	R/W	Invert polarity of LED[3:0] signals. Default is to drive an active low signal on the LED pins.	0000
9:6	Reserved	R/O	Reserved.	
5	Enable 1000BASE-T force mode	R/W	1: Enable 1000BASE-T force mode to allow PHY to link up in 1000BASE-T mode without forcing master/slave when register 0, bits 6 and 13 are set to 2'b10.	0
4	Force transmit LPI	R/W	1: Enable the EPG to transmit LPI on the MDI instead of normal idles when receiving normal idles from the MAC. 0: Transmit idles being received from the MAC.	0
3	Inhibit 100BASE-TX transmit EEE LPI	R/W	1: Disable transmission of EEE LPI on transmit path MDI in 100BASE-TX mode when receiving LPI from MAC.	0
2	Inhibit 100BASE-TX receive EEE LPI	R/W	1: Disable transmission of EEE LPI on receive path MAC interface in 100BASE-TX mode when receiving LPI from the MDI.	0
1	Inhibit 1000BASE-T transmit EEE LPI	R/W	1: Disable transmission of EEE LPI on transmit path MDI in 1000BASE-T mode when receiving LPI from MAC.	0
0	Inhibit 1000BASE-T receive EEE LPI	R/W	1: Disable transmission of EEE LPI on receive path MAC interface in 1000BASE-T mode when receiving LPI from the MDI.	0

5.5 Extended Page 3 Registers

To access the extended page 3 registers (16E3–30E3), enable extended register access by writing 0x0003 to register 31. For more information, see Table 39, page 41.

When extended page 3 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E3–30E3 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Writing 0x0000 to register 31 restores the main register access.

The following table lists the addresses and register names in the extended register page 3 space. These registers are accessible only when the device register 31 is set to 0x0003.

Table 50 • **Extended Registers Page 3 Space**

Address	Name
16E3	MAC SerDes PCS Control
17E3	MAC SerDes PCS Status
18E3	MAC SerDes Clause 37 Advertised Ability
19E3	MAC SerDes Clause 37 Link Partner Ability
20E3	MAC SerDes Status
21E3	Media SerDes Transmit Good Packet Counter
22E3	Media SerDes Transmit CRC Error Counter
23E3–30E3	Reserved

5.5.1 MAC SerDes PCS Control

The register at address 16E3 consists of the bits that provide access to and control over MAC SerDes PCS block. The following table shows the settings available.

Table 51 • **MAC SerDes PCS Control, Address 16E3 (0x10)**

Bit	Name	Access	Description	Default
15	MAC interface disable	R/W	Sticky bit. 1: 1000BASE-X MAC interface disable when media link down.	0
14	MAC interface restart	R/W	Sticky bit. 1: 1000BASE-X MAC interface restart on media link change.	0
13	MAC interface PD enable	R/W	Sticky bit. 1: MAC interface autonegotiation parallel detect enable.	0
12	MAC interface autonegotiation restart	R/W	Self-clearing bit. 1: Restart MAC interface autonegotiation.	0
11	Force advertised ability	R/W	1: Force 16-bit advertised ability from register 18E3.	0

Table 51 • **MAC SerDes PCS Control, Address 16E3 (0x10) *(continued)***

Bit	Name	Access	Description	Default
10:8	SGMII preamble control	R/W	000 = No effect on the start of packet. 001 = If both the first two nibbles of the 10/100 packet are not 0x5, a byte of 0x55 must be prefixed to the output, otherwise there will be no effect on the start of packet. 010 = If both the first two nibbles of the 10/100 packet are not 0x5, a byte of 0x55 must be prefixed to the output. An additional byte of 0x55 must be prefixed to the output if the next two nibbles are also not 0x5. 011–111 = Reserved.	001
7	MAC SerDes autonegotiation enable	R/W	1: MAC SerDes ANEG enable.	0
6	SerDes polarity at input of MAC	R/W	1: Invert polarity of signal received at input of MAC.	0
5	SerDes polarity at output of MAC	R/W	1: Invert polarity of signal at output of MAC.	
4	Fast link status enable	R/W	1: Use fast link fail indication as link status indication to MAC SerDes 0: Use normal link status indication to MAC SerDes	0
3	Unidirectional enable	R/W	1: Enable transmit on MAC interface regardless of whether the PHY has determined that a valid link has been established. 0: Enable transmit on MAC interface only when the PHY has determined that a valid link has been established.	0
2:0	Reserved	RO	Reserved.	

5.5.2 MAC SerDes PCS Status

The register at address 17E3 consists of the bits that provide status from the MAC SerDes PCS block. The following table shows the settings available.

Table 52 • **MAC SerDes PCS Status, Address 17E3 (0x11)**

Bit	Name	Access	Description
15:13	Reserved	RO	Reserved
12	SGMII alignment error	RO	1: SGMII alignment error occurred
11	MAC interface LP autonegotiation restart	RO	1: MAC interface link partner autonegotiation restart request occurred
10	Reserved	RO	Reserved
9:8	MAC remote fault	RO	01, 10, and 11: Remote fault detected from MAC 00: No remote fault detected from MAC
7	Asymmetric pause advertisement	RO	1: Asymmetric pause advertised by MAC

Table 52 • **MAC SerDes PCS Status, Address 17E3 (0x11) *(continued)***

Bit	Name	Access	Description
6	Symmetric pause advertisement	RO	1: Symmetric pause advertised by MAC
5	Full duplex advertisement	RO	1: Full duplex advertised by MAC
4	Half duplex advertisement	RO	1: Half duplex advertised by MAC
3	MAC interface LP autonegotiation capable	RO	1: MAC interface link partner autonegotiation capable
2	MAC interface link status	RO	1: MAC interface link status connected
1	MAC interface autonegotiation complete	RO	1: MAC interface autonegotiation complete
0	MAC interface PCS signal detect	RO	1: MAC interface PCS signal detect present

5.5.3 MAC SerDes Clause 37 Advertised Ability

The register at address 18E3 consists of the bits that provide access to and control over MAC SerDes Clause 37 advertised ability. The following table shows the settings available.

Table 53 • **MAC SerDes Cl37 Advertised Ability, Address 18E3 (0x12)**

Bit	Name	Access	Description	Default
15:0	MAC SerDes advertised ability	R/W	Current configuration code word being advertised (this register is read/write if 16E3.11 = 1)	0x0000

5.5.4 MAC SerDes Clause 37 Link Partner Ability

The register at address 19E3 consists of the bits that provide status of the MAC SerDes link partner's Clause 37 advertised ability. The following table shows the settings available.

Table 54 • **MAC SerDes Cl37 LP Ability, Address 19E3 (0x13)**

Bit	Name	Access	Description
15:0	MAC SerDes LP ability	RO	Last configuration code word received from link partner

5.5.5 MAC SerDes Status

The register at address 20E3 consists of the bits that provide access to MAC SerDes status. The following table shows the settings available.

Table 55 • **MAC SerDes Status, Address 20E3 (0x14)**

Bit	Name	Access	Description
15	K28.5 comma realignment	RO	Self-clearing bit. 1: a K28.5 comma re-alignment has occurred
14	SerDes signal detect	RO	Self-clearing bit. Sticky bit. 1: SerDes signal detection occurred
13:0	Reserved	RO	Reserved

5.5.6 Media SerDes Transmit Good Packet Counter

The register at address 21E3 consists of the bits that provide status of the media SerDes transmit good packet counter. The following table shows the settings available.

Table 56 • **Media SerDes Tx Good Packet Counter, Address 21E3 (0x15)**

Bit	Name	Access	Description
15	Tx good packet counter active	RO	1: Transmit good packet counter active
14	Reserved	RO	Reserved
13:0	Tx good packet count	RO	Transmit good packet count modulo 10000

5.5.7 Media SerDes Transmit CRC Error Counter

The register at address 22E3 consists of the bits that provide status of the media SerDes transmit packet count that had a CRC error. The following table shows the settings available.

Table 57 • **Media SerDes Tx CRC Error Counter, Address 22E3 (0x16)**

Bit	Name	Access	Description
15:8	Reserved	RO	Reserved
7:0	Tx CRC packet count	RO	Transmit CRC packet count (saturates at 255)

5.6 General Purpose Registers

Accessing the General Purpose register space is similar to accessing the extended page registers. Set register 31 to 0x0010. This sets all 32 registers to the general purpose register space.

To restore main register page access, write 0x0000 to register 31.

The following table lists the addresses and register names in the general purpose register page space. These registers are accessible only when the device register 31 is set to 0x0010.

Table 58 • **General Purpose Registers Page Space**

Address	Name
0G–12G	Reserved
13G	Reserved
14G	COMA_MODE Control
15G	GPIO Input
16G	GPIO Output
17G	GPIO Output Enable
18G	Global Command and SerDes Configuration
19G	MAC Mode and Fast Link Configuration
20G–24G	Reserved
25G	Enhanced LED Control
26G–28G	Reserved
29G	Global Interrupt Status
30G	Reserved

5.6.1 COMA_MODE Control

Register 14G configures the functionality of the COMA_MODE input pin.

Table 59 • **COMA_MODE Control, Address 14G (0x0E)**

Bit	Name	Access	Description	Default
15:14	Reserved	RO	Reserved	
13	COMA_MODE output enable (active low)	R/W	1: COMA_MODE pin is an input 0: COMA_MODE pin is an output	1
12	COMA_MODE output data	R/W	Value to output on the COMA_MODE pin when it is configured as an output	0
11	COMA_MODE input data	RO	Data read from the COMA_MODE pin	
10	Reserved	R/W	Reserved	0
9	Tri-state enable for LEDs	R/W	1: Tri-state LED output signals instead of driving them high. This allows those signals to be pulled above VDDIO using an external pull-up resistor. 0: Drive LED bus output signals to high and low values as appropriate.	0
8:0	Reserved	RO	Reserved.	0

5.6.2 GPIO Input

The input register contains information about the input to the device GPIO pins. Read from this register to access the data on the device GPIO pins. The following table shows the readout you can expect.

Table 60 • **GPIO Input, Address 15G (0x0F)**

Bit	Name	Access	Description	Default
15:2	Reserved	RO	Reserved	
1:0	GPIO input	RO	Data read from the GPIO_[3:2] pins	

5.6.3 GPIO Output

The output register allows you to access and control the output from the device GPIO pins. The following table shows the values you can write.

Table 61 • **GPIO Output, Address 16G (0x10)**

Bit	Name	Access	Description	Default
15:2	Reserved	RO	Reserved	
1:0	GPIO output	R/W	Data written to the GPIO_[3:2] pins	0x00

5.6.4 GPIO Pin Configuration

Register 17G in the GPIO register space controls whether a particular GPIO pin functions as an input or an output. The following table shows the settings available.

Table 62 • **GPIO Input/Output Configuration, Address 17G (0x11)**

Bit	Name	Access	Description	Default
15:2	Reserved	RO	Reserved	

Table 62 • **GPIO Input/Output Configuration, Address 17G (0x11) *(continued)***

Bit	Name	Access	Description	Default
1:0	GPIO_[3:2] pin input or output enable	R/W	1: Pin is configured as an output. 0: Pin is configured as an input.	0x00

5.6.5 Global Command and SerDes Configuration

Register 18G is a command window. Bit 15 tells the internal processor to execute the command. When bit 15 is cleared the command has completed. Software needs to wait until bit 15 = 0 before proceeding with the next PHY register access. The following table lists the values to write to register 18G to execute the various commands.

Table 63 • **Global Command and SerDes Configuration, Address 18G (0x12)**

Command	Value
Enable 12 PHYs MAC SGMII	0x80B0
Enable 12 PHYs MAC QSGMII	0x80A0
Enable 4 PHYs (PHY8 to PHY11) media 1000BASE-X	0x8F81(1)
Enable 4 PHYs (PHY8 to PHY11) media 100BASE-FX	0x8F91(1)

1. The “F” in the command has a bit representing each of the four PHYs. To exclude a PHY from the configuration, set its bit to 0. For example, the configuration of PHY 3 and PHY 2 to 1000BASE-X would be 1100 or a “C” and the command would be 0x8CC1.

5.6.6 MAC Mode and Fast Link Configuration

Register 19G controls the MAC interface mode and the selection of the source PHY for the fast link failure indication. The following table shows the settings available for the FAST_LINK_STATUS pin.

Table 64 • **MAC Mode and Fast Link Configuration, Address 19G (0x13)**

Bit	Name	Access	Description	Default
15:14	MAC interface mode select for all PHYs in the VSC8522-02	R/W	Select MAC interface mode 00: QSGMII to CAT5 mode 01: SGMII to CAT5 mode 10: QSGMII to CAT5 mode 11: Reserved	00
13:4	Reserved	RO	Reserved	
3:0	Fast link failure port setting	R/W	0000: PHY0 0001: PHY1 0010: PHY2 0011: PHY3 0100: PHY4 0101: PHY5 0110: PHY6 0111: PHY7 1000: PHY8 1001: PHY9 1010: PHY10 1011: PHY11 1100–1111: Output disabled	0xF

5.6.7 Enhanced LED Control

The following table contains the bits to control advanced functionality of the serial LED signals.

Table 65 • **Enhanced LED Control, Address 25G (0x19)**

Bit	Name	Access	Description	Default
15:8	LED pulsing duty cycle control	R/W	Programmable control for LED pulsing duty cycle when bit 30.12 is set to 1. Valid settings are between 0 and 198. A setting of 0 corresponds to a 0.5% duty cycle and 198 corresponds to a 99.5% duty cycle. Intermediate values change the duty cycle in 0.5% increments	00
7	Serial LED output 2 enable	R/W	Enable the serial LED output functionality for GPIO_5, GPIO_6, GPIO_7, and GPIO_8 pins 1: Pins function as serial LED outputs 0: Pins retain their normal function	0
6	Serial LED output 1 enable	R/W	Enable the serial LED output functionality for GPIO_[3:0] pins 1: Pins function as serial LED outputs 0: Pins retain their normal function	0
5:3	Serial LED frame rate selection	R/W	Select frame rate of serial LED stream 000: 2500 Hz frame rate 001: 1000 Hz frame rate 010: 500 Hz frame rate 011: 250 Hz frame rate 100: 200 Hz frame rate 101: 125 Hz frame rate 110: 40 Hz frame rate 111: Reserved.	
2:1	Serial LED select	R/W	Select which LEDs from each PHY to enable on the serial stream 00: Enable all 4 LEDs of each PHY 01: Enable LEDs 2, 1 and 0 of each PHY 10: Enable LEDs 1 and 0 of each PHY 11: Enable LED 0 of each PHY	00
0	Reserved	RO	Reserved.	0

5.6.8 Global Interrupt Status

The following table contains the interrupt status from the various sources to indicate which one caused that last interrupt on the pin.

Table 66 • **Global Interrupt Status, Address 29G (0x1D)**

Bit	Name	Access	Description
15:12	Reserved	RO	Reserved
11	PHY11 interrupt source(1)	RO	PHY11 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
10	PHY10 interrupt source(1)	RO	PHY10 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt

Table 66 • **Global Interrupt Status, Address 29G (0x1D) *(continued)***

Bit	Name	Access	Description
9	PHY9 interrupt source(1)	RO	PHY9 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
8	PHY8 interrupt source(1)	RO	PHY8 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
7	PHY7 interrupt source(1)	RO	PHY7 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
6	PHY6 interrupt source(1)	RO	PHY6 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
5	PHY5 interrupt source(1)	RO	PHY5 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
4	PHY4 interrupt source(1)	RO	PHY4 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
3	PHY3 interrupt source(1)	RO	PHY3 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
2	PHY2 interrupt source(1)	RO	PHY2 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
1	PHY1 interrupt source(1)	RO	PHY1 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
0	PHY0 interrupt source(1)	RO	PHY0 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt

1. This bit is set to 1 when the corresponding PHY's Interrupt Status register 26 (0x1A) is read.

5.7 Clause 45 Registers to Support Energy Efficient Ethernet

This section describes the Clause 45 registers that are required to support Energy Efficient Ethernet. Access to these registers is through the IEEE standard registers 13 and 14 (MMD access control and MMD data or address registers) as described in section 4.2.11 and 4.2.12.

The following table lists the addresses and register names in the Clause 45 register page space.

Table 67 • **Clause 45 Registers Page Space**

Address	Name
3.1	PCS Status 1
3.20	EEE Capability
3.22	EEE Wake Error Counter
7.60	EEE Advertisement
7.61	EEE Link Partner Advertisement

5.7.1 PCS Status 1

The bits in the PCS Status 1 register provide a status of the EEE operation from the PCS for the link that is currently active.

Table 68 • **PCS Status 1, Address 3.1**

Bit	Name	Access	Description
15:12	Reserved	RO	Reserved
11	Tx LPI received	RO/LH	1: Tx PCS has received LPI 0: LPI not received
10	Rx LPI received	RO/LH	1: Rx PCS has received LPI 0: LPI not received
9	Tx LPI indication	RO	1: Tx PCS is currently receiving LPI 0: PCS is not currently receiving LPI
8	Rx LPI indication	RO	1: Rx PCS is currently receiving LPI 0: PCS is not currently receiving LPI
7:3	Reserved	RO	Reserved
2	PCS receive link status	RO	1: PCS receive link up 0: PCS receive link down
1:0	Reserved	RO	Reserved

5.7.2 EEE Capability

This register is used to indicate the capability of the PCS to support EEE functions for each PHY type. The following table shows the bit assignments for the EEE capability register.

Table 69 • **EEE Capability, Address 3.20**

Bit	Name	Access	Description
15:3	Reserved	RO	Reserved
2	1000BASE-T EEE	RO	1: EEE is supported for 1000BASE-T 0: EEE is not supported for 1000BASE-T
1	100BASE-TX EEE	RO	1: EEE is supported for 100BASE-TX 0: EEE is not supported for 100BASE-TX
0	Reserved	RO	Reserved

5.7.3 EEE Wake Error Counter

This register is used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. The definition of the fault event to be counted is defined for each PHY and can occur during a refresh or a wakeup as defined by the PHY. This 16-bit counter is reset to all zeros when the EEE wake error counter is read or when the PHY undergoes hardware or software reset.

Table 70 • **EEE Wake Error Counter, Address 3.22**

Bit	Name	Access	Description
15:0	Wake error counter	RO	Count of wake time faults for a PHY

5.7.4 EEE Advertisement

This register defines the EEE advertisement that is sent in the unformatted next page following a EEE technology message code. The following table shows the bit assignments for the EEE advertisement register.

Table 71 • **EEE Advertisement, Address 7.60**

Bit	Name	Access	Description	Default
15:3	Reserved	RO	Reserved	
2	1000BASE-T EEE	R/W	1: Advertise that the 1000BASE-T has EEE capability 0: Do not advertise that the 1000BASE-T has EEE capability	0
1	100BASE-TX EEE	R/W	1: Advertise that the 100BASE-TX has EEE capability 0: Do not advertise that the 100BASE-TX has EEE capability	0
0	Reserved	RO	Reserved	

5.7.5 EEE Link Partner Advertisement

All the bits in the EEE LP Advertisement register are read only. A write to the EEE LP advertisement register has no effect. When the AN process has been completed, this register will reflect the contents of the link partner's EEE advertisement register. The following table shows the bit assignments for the EEE advertisement register.

Table 72 • **EEE Advertisement, Address 7.61**

Bit	Name	Access	Description
15:3	Reserved	RO	Reserved
2	1000BASE-T EEE	RO	1: Link partner is advertising EEE capability for 1000BASE-T 0: Link partner is not advertising EEE capability for 1000BASE-T
1	100BASE-TX EEE	RO	1: Link partner is advertising EEE capability for 100BASE-TX 0: Link partner is not advertising EEE capability for 100BASE-TX
0	Reserved	RO	Reserved

6 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC8522-02 device.

6.1 DC Characteristics

This section contains the DC specifications for the VSC8522-02 device.

6.1.1 VDD_IO

The following table shows the DC specifications for the pins referenced to VDD_IO. The specifications listed in the following table are valid only when VDD = 1.0 V, VDD_VS = 1.0 V, VDD_AL = 1.0 V, or VDD_AH = 2.5 V.

Table 73 • **VDD_IO DC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.0	2.8	V	I_{OH} = –1.0 mA
Output low voltage	V_{OL}	–0.3	0.4	V	I_{OL} = 1.0 mA
Input high voltage	V_{IH}	1.85	3.0	V	
Input low voltage	V_{IL}	–0.3	0.7	V	
Input leakage current, GPIO pins	I_{ILEAK_GPIO}	–89	32	µA	Internal resistor included
Input leakage current, all other pins	I_{ILEAK}	–32	32	µA	Internal resistor included
Output leakage current, GPIO pins	I_{OLEAK_GPIO}	–89	32	µA	Internal resistor included
Output leakage current, all other pins	I_{OLEAK}	–32	32	µA	Internal resistor included
Output low current drive strength	I_{OL}		6	mA	
Output high current drive strength	I_{OH}	–6		mA	

6.1.2 Internal Pull-Up or Pull-Down Resistors

Internal pull-up or pull-down resistors are specified in the following table. For more information about signals with internal pull-up or pull-down resistors, see Pins by Function, page 69.

All internal pull-up resistors are connected to their respective I/O supply.

Table 74 • **Internal Pull-Up or Pull-Down Resistors**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Internal pull-up resistor, GPIO pins	R_{PU}	33	53	90	kΩ
Internal pull-up resistor, all other pins	R_{PU}	96	120	144	kΩ
Internal pull-down resistor	R_{PD}	96	120	144	kΩ

6.1.3 Reference Clock

The following table shows the DC specifications for a differential reference clock input signal.

Table 75 • **Reference Clock DC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input voltage range	V_{IP},V_{IN}	–25		1260	mV
Input differential voltage	V_{ID}	150(1)		1000	mV
Input common-mode voltage	V_{ICM}	0		1200(2)	mV
Differential input impedance	R_I		100		Ω

1. To meet jitter specifications, the minimum input differential voltage must be 400 mV. When using a single-ended clock input, the REFCLK_P low voltage must be less than V_{DDA} – 200 mV, and the high voltage level must be greater than V_{DDA} + 200 mV.
2. The maximum common-mode voltage is provided without a differential signal. The common-mode voltage is only limited by the maximum and minimum input voltage range and by the differential amplitude of the input signal.

6.1.4 Enhanced SerDes Interface (QSGMII)

All DC specifications for the enhanced SerDes interface are compliant with QSGMII Specification Revision 1.3 and meet or exceed the requirements in the standard. They are also compliant with OIF-CEI-02.0 requirements where applicable. The following table shows the DC specifications for the enhanced SerDes driver.

Table 76 • **Enhanced SerDes Driver DC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output differential peak voltage, QSGMII mode	$\|V_{ODp}\|$	250	400	mV	V_{DD_VS} = 1.0 V R_L = 100 Ω ±1% maximum drive
Output current, drivers shorted to ground, SGMII and QSGMII modes	$\|I_{OSA}\|$, $\|I_{OSB}\|$		40	mA	
Output current, drivers shorted together, SGMII and QSGMII modes	$\|I_{OSAB}\|$		12	mA	

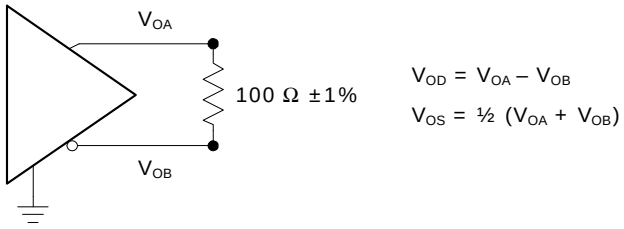
The following table lists the DC specifications for the enhanced SerDes receiver.

Table 77 • **Enhanced SerDes Receiver DC Specifications**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input voltage range, V_{IA} or V_{IB}(1)	V_I	–0.25		1.2	V
Input differential peak-to-peak voltage	$\|V_{ID}\|$	100		1600	mV
Input common-mode voltage	V_{ICM}	0		1200	mV
Receiver differential input impedance	R_I	80	100	120	Ω

1. QSGMII DC input sensitivity is less than 400 mV.

Figure 21 • **QSGMII DC Transmit Test Circuit**



6.1.5 Current Consumption

The typical current consumption values in QSGMII to 1000BASE-T mode are based on nominal voltages with the MAC interface operating in QSGMII mode, and all media side ports operating in 1000BASE-T with full-duplex enabled. Data traffic is a 64-bit random data pattern at 100% utilization.

Table 78 • **QSGMII to 1000BASE-T Current Consumption**

Parameter	Symbol	Typical	Maximum	Unit
Worst-case power consumption	P_D		6.75	W
Current with V_{DD} at 1.0 V	I_{VDD}	1.15		A
Current with V_{DD_A} at 1.0 V	I_{VDD_A}	0.18		A
Current with V_{DD_AH} at 2.5 V	I_{VDD_AH}	1.37		A
Current with V_{DD_AL} at 1.0 V	I_{VDD_AL}	0.19		A
Current with V_{DD_IO} at 2.5 V	I_{VDD_IO}	0.06		A
Current with V_{DD_VS} at 1.0 V	I_{VDD_VS}	0.09		A

6.2 AC Characteristics

This section provides the AC specifications for the VSC8522-02 device.

6.2.1 Reference Clock

To meet QSGMII jitter generation requirements, Microsemi requires the use of a differential reference clock source. Use of a 25 MHz single-ended reference clock is not recommended. However, to implement a QSGMII chip interconnect using a 25 MHz single-ended reference clock and achieve error-free data transfer on that interface, use an Ethernet switch with higher jitter tolerance than specified in the standard, such as Microsemi VSC742*x* family of products. For more information about QSGMII interoperability when using a 25 MHz single-ended reference clock, contact your Microsemi representative.

The following table shows the AC specifications for a differential reference clock input. Performance is guaranteed for 156.25 MHz and 125 MHz differential clocks only, however 25 MHz and single-ended clocks are also supported.

Table 79 • **Reference Clock AC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Reference clock frequency, REFCLK_SEL[2:0] = 100	*f*	–100 ppm	25.00	100 ppm	MHz	
Reference clock frequency, REFCLK_SEL[2:0] = 000	*f*	–100 ppm	125.00	100 ppm	MHz	
Reference clock frequency, REFCLK_SEL[2:0] = 001	*f*	–100 ppm	156.25	100 ppm	MHz	
Duty cycle	DC	40	50	60	%	

Table 79 • **Reference Clock AC Characteristics *(continued)***

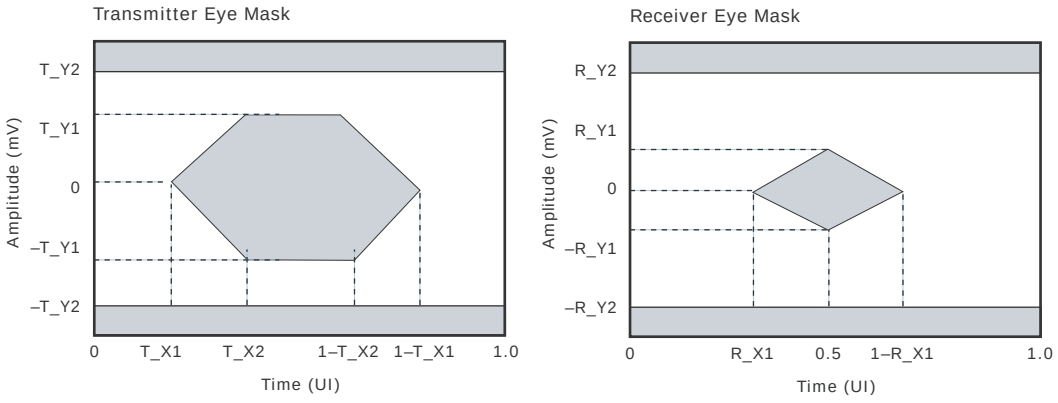
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Rise time and fall time	t_R, t_F			1.5	ns	20% to 80% threshold
REFCLK input RMS jitter, bandwidth from 12 kHz to 500 kHz				20	ps	
REFCLK input RMS jitter, bandwidth from 500 kHz to 15 MHz				4	ps	
REFCLK input RMS jitter, bandwidth from 15 MHz to 40 MHz				20	ps	
REFCLK input RMS jitter, bandwidth from 40 MHz to 80 MHz				100	ps	
Jitter gain from REFCLK to SerDes output, bandwidth from 0 MHz to 0.1 MHz				0.3	dB	
Jitter gain from REFCLK to SerDes output, bandwidth from 0.1 MHz to 7 MHz				3	dB	
Jitter gain from REFCLK to SerDes output, bandwidth greater than 7 MHz				3 –20 × log (*f*/7 MHz)	dB	

6.2.2 Enhanced SerDes Interface

All AC specifications for the enhanced SerDes interface are compliant with QSGMII Specification Revision 1.3 and meet or exceed the requirements in the standard. They are also compliant with the OIF-CEI-02.0 requirements where applicable.

The values in the tables in the following sections apply to QSGMII mode and are based on the test circuit shown in Figure 21, page 59. The transmit and receive eye specifications relate to the eye diagrams shown in the following illustration, with the compliance load as defined in the test circuit.

Figure 22 • **QSGMII Transient Parameters**



6.2.3 Enhanced SerDes Outputs

The following table provides the AC specifications for the enhanced SerDes outputs in QSGMII mode.

Table 80 • **Enhanced SerDes Outputs AC Specifications, QSGMII Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Unit interval, 5G	UI				200 ps
V_{OD} rise time and fall time	t_R, t_F	30	96	ps	20% to 80% of V_S R_L = 100 Ω ±1%
Differential peak-to-peak output voltage	V_{OD}		30	mV	Tx disabled
Differential output return loss, 100 MHz to 2.5 GHz	RL_{O_DIFF}	8		dB	R_L = 100 Ω ±1%
Differential output return loss, 2.5 GHz to 5 GHz	RL_{O_DIFF}	8 dB – 16.6 log (f/2.5 GHz)		dB	R_L = 100 Ω ±1%
Eye mask X1	T_X1		0.15	UI	
Eye mask X2	T_X2		0.4	UI	
Eye mask Y1	T_Y1	200		mV	
Eye mask Y2	T_Y2		450	mV	

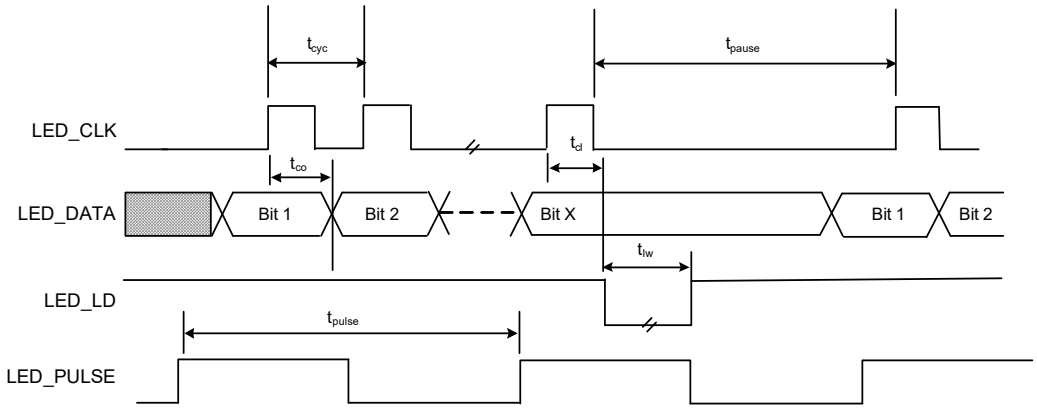
6.2.4 Enhanced Serial LEDs

This section contains the AC specifications for the enhanced serial LEDs. The duty cycle of the LED_PULSE signal is programmable and can be varied from 0.5% to 99.5%.

Table 81 • **Enhanced Serial LEDs AC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit
LED_CLK cycle time	t_{CYC}	255	257	ns
Pause between LED_DATA bit sequences	t_{PAUSE}	387.712	24987	µs
LED_CLK to LED_DATA	t_{CO}	127	129	ns
LED_CLK to LED_LD	t_{CL}	255	257	ns
LED_LD pulse width	t_{LW}	127	129	ns
LED_PULSE cycle time	t_{PULSE}	199	201	µs

Figure 23 • **Enhanced Serial LED Timing**



6.2.5 Enhanced SerDes Driver Jitter Characteristics

The following table lists the jitter characteristics for the enhanced SerDes driver in QSGMII mode.

Table 82 • **Enhanced SerDes Driver Jitter Characteristics, QSGMII Mode**

Parameter	Symbol	Maximum	Unit	Condition
Total output jitter	TJ_O	60	ps	Measured according to IEEE 802.3.38.5.
Deterministic output jitter	DJ_O	10	ps	Measured according to IEEE 802.3.38.5.

6.2.6 Enhanced SerDes Inputs

The following table lists the AC specifications for the enhanced SerDes inputs in QSGMII mode.

Table 83 • **Enhanced SerDes Inputs AC Specifications, QSGMII Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Unit interval, 5G	UI				200 ps
Differential input return loss, 100 MHz to 2.5 GHz	RL_{I_DIFF}	8		dB	R_L = 100 Ω ±1%
Differential input return loss, 2.5 GHz to 5 GHz	RL_{I_DIFF}	8 dB – 16.6 log (f/2.5 GHz)		dB	R_L = 100 Ω ±1%
Common-mode input return loss, 100 MHz to 2.5 GHz	RL_{ICM}	6		dB	
Eye mask X1	R_X1		0.3	UI	
Eye mask Y1	R_Y1		50	mV	
Eye mask Y2	R_Y2		450	mV	

6.2.7 Enhanced SerDes Receiver Jitter Tolerance

The following table lists the jitter tolerance for the enhanced SerDes receiver in QSGMII mode.

Table 84 • **Enhanced SerDes Receiver Jitter Tolerance, QSGMII Mode**

Parameter	Symbol	Maximum	Unit	Condition
Bounded high-probability jitter(1)	BHPJ	90	ps	92 ps peak-to-peak random jitter and 38 ps sinusoidal jitter (SJHF).
Sinusoidal jitter, maximum	SJ_{MAX}	1000	ps	
Sinusoidal jitter, high frequency	SJ_{HF}	10	ps	
Total jitter tolerance	TJT_I	120	ps	92 ps peak-to-peak random jitter and 38 ps sinusoidal jitter (SJHF).

1. This is the sum of uncorrelated bounded high probability jitter (0.15 UI), and correlated bounded high probability jitter (0.30 UI). Uncorrelated bounded high probability jitter is distribution where the value of the jitter shows no correlation to any signal level being transmitted, formally defined as deterministic jitter (DJ). Correlated bounded high probability jitter is jitter distribution where the value of the jitter shows a strong correlation to the signal level being transmitted.

6.2.8 JTAG Interface

This section provides the AC specifications for the JTAG interface. The specifications meet or exceed the requirements of IEEE 1149.1-2001. The JTAG receive signal requirements are requested at the pin of the device. The JTAG_TRST signal is asynchronous to the clock, and does not have a setup or hold time requirement.

Table 85 • **JTAG Interface AC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
TCK frequency	f		10	MHz	
TCK cycle time	t_C	100		ns	
TCK high time	$t_{W(CH)}$	40		ns	
TCK low time	$t_{W(CL)}$	40		ns	
Setup time to TCK rising	t_{SU}	10		ns	
Hold time from TCK rising	t_H	10		ns	
TDO valid after TCK falling	$t_{V(C)}$		28	ns	C_L = 10 pF
TDO hold time from TCK falling	$t_{H(TDO)}$	0		ns	C_L = 0 pF
TDO disable time(1)	t_{DIS}		30	ns	See Figure 25, page 64.
nTRST time low	$t_{W(TL)}$	30		ns	

1. The pin begins to float when a 300 mV change from the actual V_{OH}/V_{OL} level occurs.

Figure 24 • **JTAG Interface Timing Diagram**

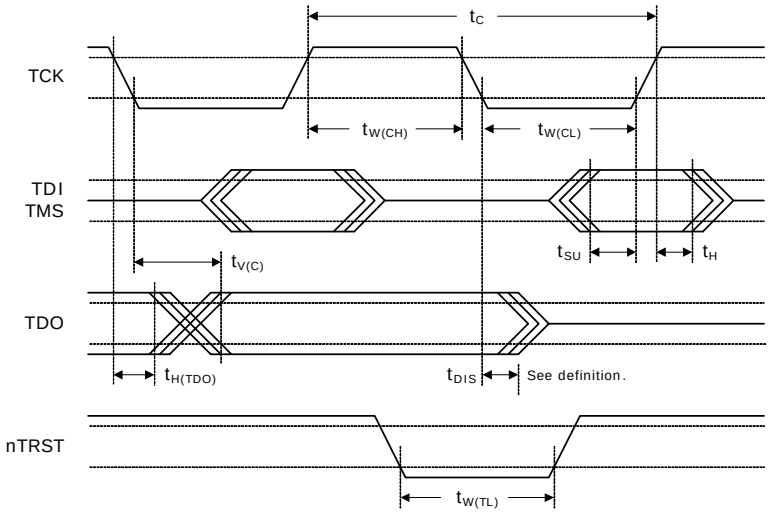
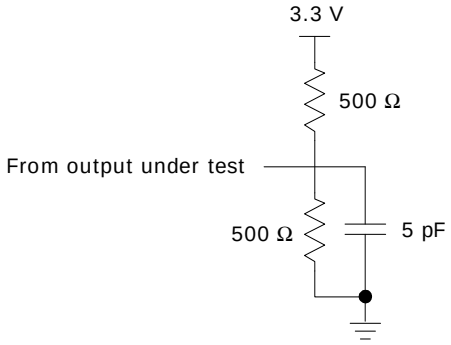


Figure 25 • **Test Circuit for TDO Disable Time**



6.2.9 Serial Management Interface

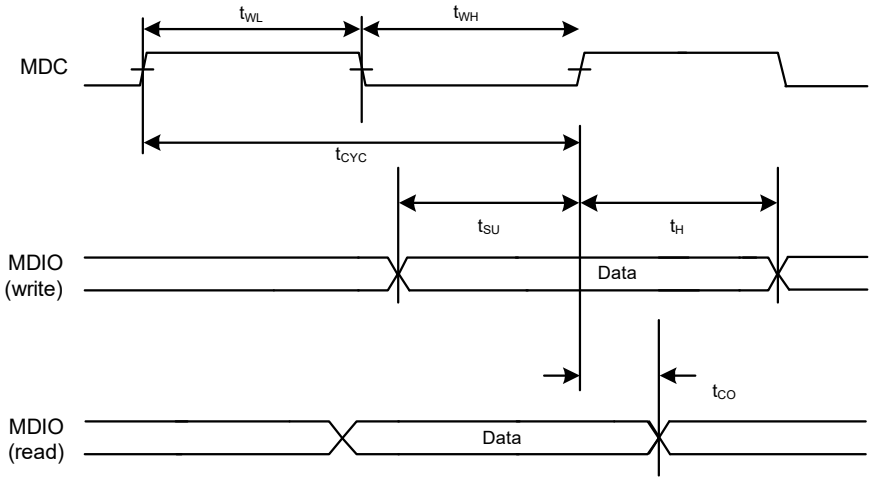
This section contains the AC specifications for the serial management interface (SMI).

Table 86 • **SMI Interface AC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
MDC frequency(1)	f_{CLK}	0.488		20.83	MHz	
MDC cycle time	t_{CYC}	48		2048	ns	
MDC time high	t_{WH}	20			ns	C_L = 50 pF
MDC time low	t_{WL}	20			ns	C_L = 50 pF
MDIO setup time to MDC on write	t_{SU}	15			ns	
MDIO hold time to MDC on write	t_H	15			ns	
MDC rise time, MDC = 0: 1 MHz	t_R			100	ns	
MDC rise time, MDC = 1 MHz: f_{CLK} maximum	t_R			t_{CYC} × 10%(1)	ns	
MDC fall time, MDC = 0: 1 MHz	t_F			100	ns	
MDC fall time, MDC = 1 MHz: f_{CLK} maximum	t_F			t_{CYC} × 10%(1)	ns	
MDC to MDIO valid	t_{CO}		10	300	ns	Time-dependant on the value of the external pull-up resistor on the MDIO pin

1. For f_{CLK} greater than 1 MHz, the minimum rise time and fall time is in relation to the frequency of the MDC clock period. For example, if f_{CLK} is 2 MHz, the minimum clock rise time and fall time is 50 ns.

Figure 26 • **SMI Interface Timing**



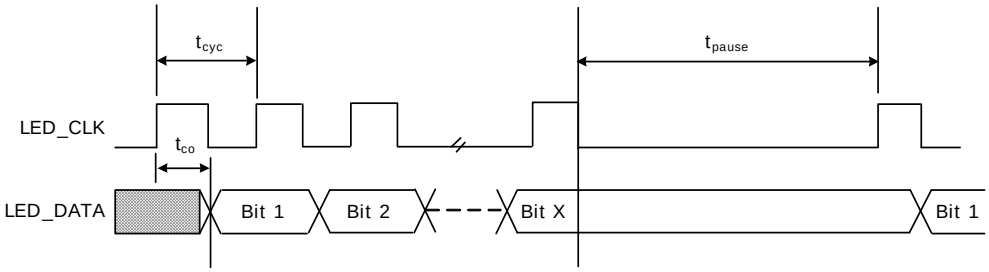
6.2.10 Reset Timing

This section contains the AC specifications that apply to device reset functionality. The signal applied to the NRESET input must comply with the specifications listed in the following table.

Table 87 • **NRESET Timing Specifications**

Parameter	Symbol	Minimum	Maximum	Unit
NRESET assertion time after power supplies and clock stabilize	t_W	2		ms
Recovery time from reset inactive to device fully active	t_{REC}		105	ms
NRESET pulse width	$t_{W(RL)}$	100		ns
Wait time between NRESET de-assert and access of the SMI interface	t_{WAIT}	105		ms

Figure 27 • **Reset Timing**



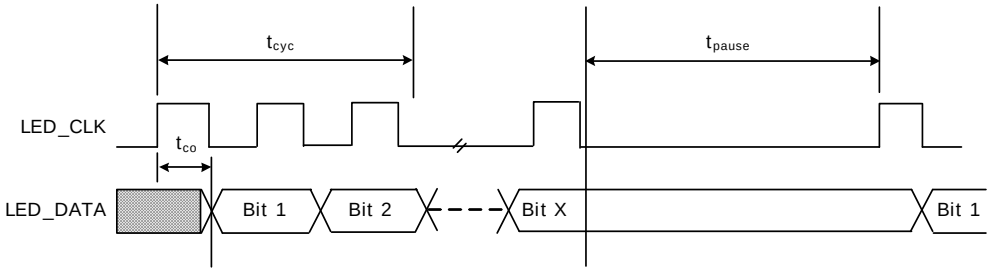
6.2.11 Serial LEDs

This section contains the AC specifications for the serial LEDs.

Table 88 • **Serial LEDs AC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit
LED_CLK cycle time	t_{CYC}	1		µs
Pause between LED bit sequences	t_{PAUSE}	25		ms
LED_CLK to LED_DATA	t_{CO}		1	ns

Figure 28 • **Serial LED Timing**



6.2.12 Power Supply Sequencing

During power on and off, V_{DD_A} and V_{DD_VS} must never be more than 300 mV above V_{DD}. V_{DD_VS} must be powered, even if the associated interface is not used. These power supplies must not remain at ground or left floating.

There are no sequencing requirements for V_{DD_AL}, V_{DD_AH}, or V_{DD_IO}. These power supplies can remain at ground or left floating if not used.

The NRESET and JTAG_nTRST inputs must be held low until all power supply voltages

have reached their recommended operating condition values.

6.3 Operating Conditions

The following table shows the recommended operating conditions for the device.

Table 89 • **Recommended Operating Conditions**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage for V_{DD}	V_{DD}	0.95	1.00	1.05	V
Power supply voltage for V_{DD_A}	V_{DD_A}	0.95	1.00	1.05	V
Power supply voltage for V_{DD_AH}	V_{DD_AH}	2.38	2.50	2.62	V
Power supply voltage for V_{DD_AL}	V_{DD_AL}	0.95	1.00	1.05	V
Power supply voltage for V_{DD_IO}	V_{DD_IO}	2.38	2.50	2.62	V
Power supply voltage for V_{DD_VS}	V_{DD_VS}	0.95	1.00	1.05	V
VSC8522-02 operating temperature(1)	T	0		125	°C
VSC8522-04 operating temperature(1)	T	–40		125	°C

1. Minimum specification is ambient temperature, and the maximum is junction temperature.

6.4 Stress Ratings

This section contains the stress ratings for the VSC8522-02 device.

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 90 • **Stress Ratings**

Parameter	Symbol	Minimum	Maximum	Unit
Power supply voltage for core supply	V_{DD}	–0.3	1.10	V
Power supply voltage for SerDes and Enhanced SerDes interfaces	V_{DD_VS}	–0.3	1.32	V

Table 90 • **Stress Ratings *(continued)***

Parameter	Symbol	Minimum	Maximum	Unit
Power supply voltage for analog circuits in twisted pair interface	V_{DD_AL}	–0.3	1.10	V
Power supply voltage for analog circuits in twisted pair interface	V_{DD_AH}	–0.3	2.75	V
Power supply voltage for MIIM, PI, and miscellaneous I/O	V_{DD_IO}	–0.3	2.75	V
Input voltage for GPIO and logic input pins			3.3	V
Storage temperature	T_S	–55	125	°C
Electrostatic discharge voltage, charged device model	V_{ESD_CDM}	–500	500	V
Electrostatic discharge voltage, human body model	V_{ESD_HBM}	–1750	1750	V

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Microsemi recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

7 Pin Descriptions

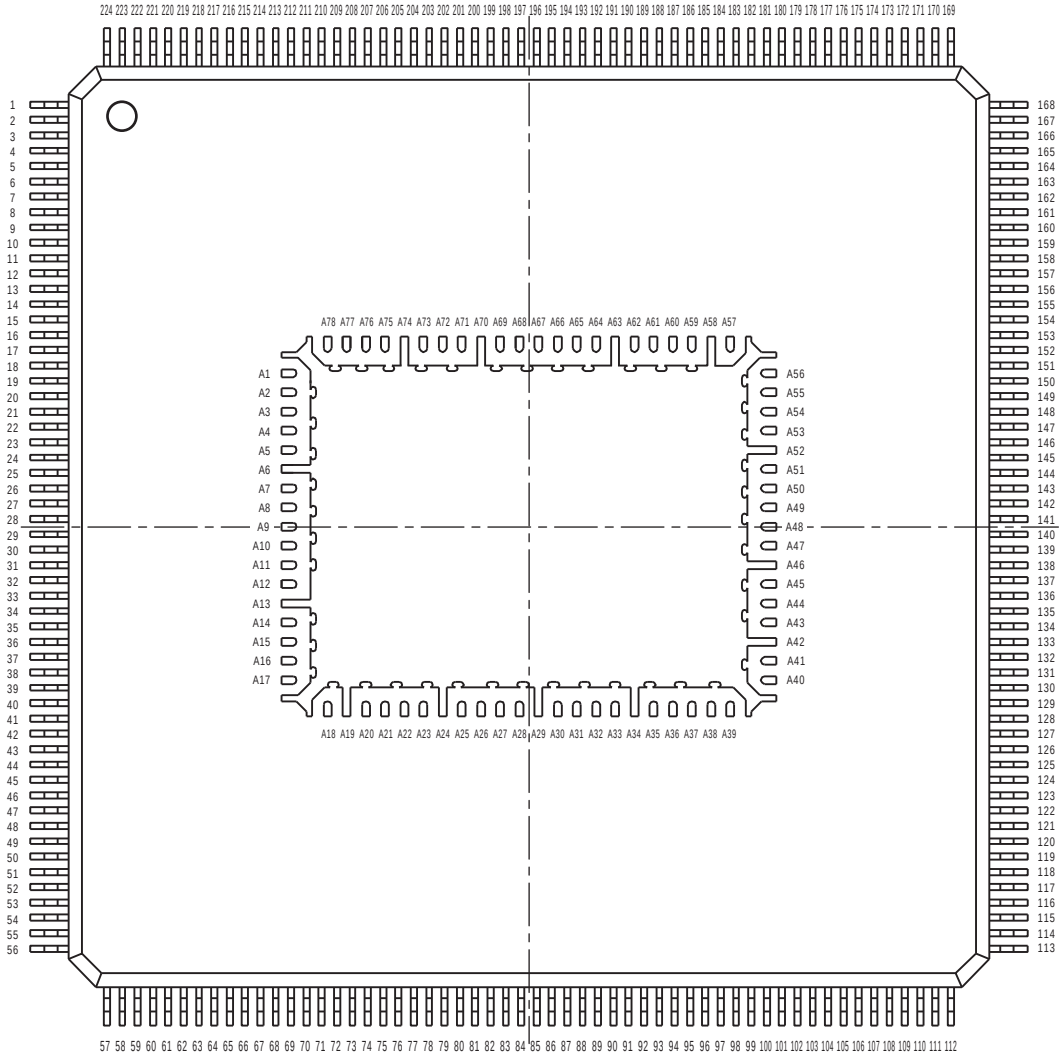
The VSC8522-02 device has 302 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file, so that you can copy it electronically. In Adobe Reader, double-click the attachment icon.

7.1 Pin Diagram

The following illustration shows the pin diagram for the VSC8522-02 device, as seen from the top view looking through the device.

Figure 29 • **Pin Diagram**



7.2 Pins by Function

This section contains the functional pin descriptions for the VSC8522-02 device. The following table lists the definitions for the pin type symbols.

Table 91 • **Pin Type Symbol Definitions**

Symbol	Pin Type	Description
3V		3.3 V-tolerant pin.
ABIAS	Analog bias	Analog bias pin.
ADIFF	Analog differential	Analog differential signal pair.
I	Input	Input without on-chip pull-up or pull-down resistor.
I/O	Bidirectional	Bidirectional input or output signal.
NC	No connect	No connect pins must be left floating.
O	Output	Output signal.
OD	Open drain	Open drain output.
OS	Open source	Open source output.
PD	Pull-down	On-chip pull-down resistor to VSS.
PU	Pull-up	On-chip pull-up resistor to VDD_IO.
ST	Schmitt-trigger	Input has Schmitt-trigger circuitry.

7.2.1 JTAG Interface Pins

The following table shows the functional pins for the JTAG interface.

Table 92 • **JTAG Pins**

Name	Pin	Type	Description
JTAG_CLK	175	I, PU, ST, 3V	JTAG clock pin
JTAG_DI	174	I, PU, ST, 3V	JTAG data input pin
JTAG_DO	172	O	JTAG data output pin
JTAG_TMS	173	I, PU, ST, 3V	JTAG test mode select pin
JTAG_TRST	171	I, PU, ST, 3V	JTAG reset pin

7.2.2 MAC SerDes/QSGMII Interface Pins

The following table shows the functional pins for the MAC SerDes/QSGMII interface.

Table 93 • **MAC SerDes/QSGMII Interface Pins**

Name	Pin	Type	Description
SERDES_E[1:3]_RXN	A31, A27, A21	ADIFF	6G SerDes receive negative polarity pins
SERDES_E[1:3]_RXP	A30, A28, A20	ADIFF	6G SerDes receive positive polarity pins
SERDES_E[1:3]_TXN	A33, A25, A23	ADIFF	6G SerDes transmit negative polarity pins
SERDES_E[1:3]_TXP	A32, A26, A22	ADIFF	6G SerDes transmit positive polarity pins
SERDES_REXT_[0:1]	106, 107	ABIAS	Analog bias calibration. Connect an external 620 Ω ±1% resistor between SERDES_REXT_1 and SERDES_REXT_0.

7.2.3 Miscellaneous Pins

The following table shows the miscellaneous pins.

Table 94 • **Miscellaneous Pins**

Name	Pin	Type	Description
ESLED0_CLK	50	I/O	Enhanced serial LED clock
ESLED0_LD	49	I/O	Enhanced serial LED load
ESLED1_CLK	45	I/O	LED direct-drive output Enhanced serial LED clock
ESLED1_DO	44	I/O	LED direct-drive output Enhanced serial LED data
ESLED1_LD	A14	I/O	LED direct-drive output Enhanced serial LED load
ESLED1_PULSE	43	I/O	LED direct-drive output Enhanced serial LED pulse
FAST_LINK_STATUS	38	I/O	Fast link failure indication.
GPIO_15	42	I/O	LED direct-drive output General purpose I/O
GPIO_16	41	I/O	LED direct-drive output General purpose I/O
GPIO_29	40	I/O	General purpose I/O
PHYADD[3:4]	222, 221	I, PD	PHY address range select.
REFCLK_N REFCLK_P	69 70	I, ADIFF	Reference clock input. The input can be either differential or single-ended. In differential mode, REFCLK_P is the true part of the differential signal, and REFCLK_N is the complement part of the differential signal. In single-ended mode, REFCLK_P is used as single-ended LVTTL input, and the REFCLK_N should be pulled to VDD_A. Required applied frequency depends on REFCLK_SEL[2:0] input state.
REFCLK_SEL[0:2]	216, 217, 215	I, PD	Reference clock frequency select. 0: Connect to pull-down or leave floating. 1: Connect to pull-up to VDD_IO. 000: 125 MHz (default). 001: 156.25 MHz. 100: 25 MHz.

7.2.4 Multipurpose Pins

The following table shows the functional descriptions for the multipurpose I/O pins.

Table 95 • **Multipurpose Pins**

Name	Pin	Type	Description
ESLED0_DO / GPIO_2	A15	I/O	Enhanced serial LED data General purpose I/O
ESLED0_PULSE / GPIO_3	47	I/O	Enhanced serial LED pulse General purpose I/O

7.2.5 Power Supply Pins

The following table shows the power supply pins. All power supply pins must be connected to their respective voltage input, even though certain pin functions may not be used for a specific application.

Table 96 • **Power Supply Pins**

Name	Pin	Type	Description
VDD_[1:41]	57, 58, 59, 76, 77, 78, 86, 87, 88, 89, 90, 99, 100, 101, 102, 105, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, A10, A43, A44, A45, A61, A62, A72, A73	1.0V	Connect to 1.0 V
VDD_A_[1:15]	60, 63, 64, 68, 71, 72, 74, 80, 82, 85, 91, 93, 95, 98, 104	1.0V	Analog SerDes 1.0 V
VDD_AH_[1:21]	A2, A3, A4, A5, A7, A8, A9, A47, A48, A49, A50, A51, A53, A54, A55, A64, A65, A66, A67, A68, A69	2.5V	Analog 2.5 V
VDD_AL_[1:12]	1, 20, 37, 126, 127, 128, 129, 130, 133, 160, 183, 201	1.0V	Analog 1.0 V
VDD_IO_[1:11]	39, 56, 67, 83, 108, A59, A60, A71, A75, A76, A77	2.5V	Connect to 2.5 V
VDD_VS_[1:12]	61, 62, 73, 75, 79, 81, 84, 92, 94, 96, 97, 103	1.0V	Analog SerDes 1.0 V
VSS_[1:16] VSS_163	A6, A13, A18, A19, A24, A29, A34, A39, A40, A41, A42, A46, A52, A58, A63, A70, A74	0V	Ground

7.2.6 Reserved Pins

The following table shows the reserved device pins. Except for pin 223 (RESERVED_0), which must be connected to ground, all RESERVED pins must be left floating.

Table 97 • **Reserved Pins**

Name	Pin	Type	Description
RESERVED_0	223	NC	Reserved. Connect to ground.
RESERVED_[3:8]	220, 218, 167, 168, 169, 170	NC	Reserved. Leave unconnected.
RESERVED_[10:18]	A56, A57, 212, 213, A78, A1, A17, A16	NC	Reserved. Leave unconnected.
RESERVED_[22:30]	66, 65, A11, 53, 52, 48, 51, 219, 46	NC	Reserved. Leave unconnected.
RESERVED_[100:103]	A38, A37, A36, A35	NC	Reserved. Leave unconnected.

7.2.7 Serial Management Interface Pins

The following table shows the functional pins for the serial management interface.

Table 98 • **Serial Management Interface Pins**

Name	Pin	Type	Description
COMA_MODE	214	I/O, PU, ST, 3V	When this pin is asserted high, all PHYs are held in a powered down state. When this pin is deasserted low, all PHYs are powered up and resume normal operation. This signal is also used to synchronize the operation of multiple chips on the same PCB to provide visual synchronization for LEDs driven from the separate chips.
MDC	54	I	Management data clock pin.
MDINT	A12	I/O, OD, OS	Management interrupt signal.
MDIO	55	I/O, OD	Management data input/output pin.
NRESET	224	I, PD, ST, 3V	Device reset pin, active low.

7.2.8 Twisted Pair Interface Pins

The following table shows the functional pins for the twisted pair interface.

Table 99 • **Twisted Pair Interface Pins**

Name	Pin	Type	Description
P[0:11]_D0N	138, 146, 156, 165, 182, 191, 202, 210, 8, 16, 27, 35	ADIFF	Connects to RJ45 pin 2 through a magnetic.
P[0:11]_D0P	139, 147, 157, 166, 184, 192, 203, 211, 9, 17, 28, 36	ADIFF	Connects to RJ45 Pin 1 through a magnetic.
P[0:11]_D1N	136, 144, 154, 163, 180, 189, 199, 208, 6, 14, 25, 33	ADIFF	Connects to RJ45 Pin 6 through a magnetic.
P[0:11]_D1P	137, 145, 155, 164, 181, 190, 200, 209, 7, 15, 26, 34	ADIFF	Connects to RJ45 Pin 3 through a magnetic.
P[0:11]_D2N	134, 142, 152, 161, 178, 187, 197, 206, 4, 12, 23, 31	ADIFF	Connects to RJ45 Pin 5 through a magnetic.
P[0:11]_D2P	135, 143, 153, 162, 179, 188, 198, 207, 5, 13, 24, 32	ADIFF	Connects to RJ45 Pin 4 through a magnetic.
P[0:11]_D3N	131, 140, 150, 158, 176, 185, 195, 204, 2, 10, 21, 29	ADIFF	Connects to RJ45 Pin 8 through a magnetic.
P[11:0]_D3P	132, 141, 151, 159, 177, 186, 196, 205, 3, 11, 22, 30	ADIFF	Connects to RJ45 Pin 7 through a magnetic.
REF_FILT_[0:2]	148, 193, 18	ABIAS	Copper media reference filter pins. Connect each of these pins to one external 1 µF capacitor each and then all going to ground.

Table 99 • **Twisted Pair Interface Pins *(continued)***

Name	Pin	Type	Description
REF_REXT_[0:2]	149, 194, 19	ABIAS	Copper media reference external pins. Connect each of these pins to one external 2.0 kΩ (1%) resistor each and then all going to ground.

7.3 Pins by Number

This section provides a numeric list of the VSC8522-02 pins.

1	VDD_AL_1
2	P8_D3N
3	P8_D3P
4	P8_D2N
5	P8_D2P
6	P8_D1N
7	P8_D1P
8	P8_D0N
9	P8_D0P
10	P9_D3N
11	P9_D3P
12	P9_D2N
13	P9_D2P
14	P9_D1N
15	P9_D1P
16	P9_D0N
17	P9_D0P
18	REF_FILT_2
19	REF_REXT_2
20	VDD_AL_2
21	P10_D3N
22	P10_D3P
23	P10_D2N
24	P10_D2P
25	P10_D1N
26	P10_D1P
27	P10_D0N
28	P10_D0P
29	P11_D3N
30	P11_D3P
31	P11_D2N
32	P11_D2P
33	P11_D1N
34	P11_D1P
35	P11_D0N
36	P11_D0P
37	VDD_AL_3
38	FAST_LINK_STATUS
39	VDD_IO_1
40	GPIO_29
41	GPIO_16
42	GPIO_15
43	ESLED1_PULSE
44	ESLED1_DO
45	ESLED1_CLK
46	RESERVED_30
47	ESLED0_PULSE / GPIO_3
48	RESERVED_27
49	ESLED0_LD
50	ESLED0_CLK
51	RESERVED_28
52	RESERVED_26
53	RESERVED_25
54	MDC
55	MDIO
56	VDD_IO_2
57	VDD_1
58	VDD_2
59	VDD_3
60	VDD_A_1
61	VDD_VS_1
62	VDD_VS_2
63	VDD_A_2
64	VDD_A_3
65	RESERVED_23
66	RESERVED_22
67	VDD_IO_3
68	VDD_A_4
69	REFCLK_N
70	REFCLK_P
71	VDD_A_5
72	VDD_A_6
73	VDD_VS_3
74	VDD_A_7
75	VDD_VS_4

Pins by number *(continued)*

76	VDD_4
77	VDD_5
78	VDD_6
79	VDD_VS_5
80	VDD_A_8
81	VDD_VS_6
82	VDD_A_9
83	VDD_IO_4
84	VDD_VS_7
85	VDD_A_10
86	VDD_7
87	VDD_8
88	VDD_9
89	VDD_10
90	VDD_11
91	VDD_A_11
92	VDD_VS_8
93	VDD_A_12
94	VDD_VS_9
95	VDD_A_13
96	VDD_VS_10
97	VDD_VS_11
98	VDD_A_14
99	VDD_12
100	VDD_13
101	VDD_14
102	VDD_15
103	VDD_VS_12
104	VDD_A_15
105	VDD_16
106	SERDES_REXT_0
107	SERDES_REXT_1
108	VDD_IO_5
109	VDD_17
110	VDD_18
111	VDD_19
112	VDD_20
113	VDD_21

114	VDD_22
115	VDD_23
116	VDD_24
117	VDD_25
118	VDD_26
119	VDD_27
120	VDD_28
121	VDD_29
122	VDD_30
123	VDD_31
124	VDD_32
125	VDD_33
126	VDD_AL_4
127	VDD_AL_5
128	VDD_AL_6
129	VDD_AL_7
130	VDD_AL_8
131	P0_D3N
132	P0_D3P
133	VDD_AL_9
134	P0_D2N
135	P0_D2P
136	P0_D1N
137	P0_D1P
138	P0_D0N
139	P0_D0P
140	P1_D3N
141	P1_D3P
142	P1_D2N
143	P1_D2P
144	P1_D1N
145	P1_D1P
146	P1_D0N
147	P1_D0P
148	REF_FILT_0
149	REF_REXT_0
150	P2_D3N
151	P2_D3P

Pins by number *(continued)*

152	P2_D2N
153	P2_D2P
154	P2_D1N
155	P2_D1P
156	P2_D0N
157	P2_D0P
158	P3_D3N
159	P3_D3P
160	VDD_AL_10
161	P3_D2N
162	P3_D2P
163	P3_D1N
164	P3_D1P
165	P3_D0N
166	P3_D0P
167	RESERVED_5
168	RESERVED_6
169	RESERVED_7
170	RESERVED_8
171	JTAG_TRST
172	JTAG_DO
173	JTAG_TMS
174	JTAG_DI
175	JTAG_CLK
176	P4_D3N
177	P4_D3P
178	P4_D2N
179	P4_D2P
180	P4_D1N
181	P4_D1P
182	P4_D0N
183	VDD_AL_11
184	P4_D0P
185	P5_D3N
186	P5_D3P
187	P5_D2N
188	P5_D2P
189	P5_D1N
190	P5_D1P
191	P5_D0N
192	P5_D0P
193	REF_FILT_1
194	REF_REXT_1
195	P6_D3N
196	P6_D3P
197	P6_D2N
198	P6_D2P
199	P6_D1N
200	P6_D1P
201	VDD_AL_12
202	P6_D0N
203	P6_D0P
204	P7_D3N
205	P7_D3P
206	P7_D2N
207	P7_D2P
208	P7_D1N
209	P7_D1P
210	P7_D0N
211	P7_D0P
212	RESERVED_12
213	RESERVED_13
214	COMA_MODE
215	REFCLK_SEL2
216	REFCLK_SEL0
217	REFCLK_SEL1
218	RESERVED_4
219	RESERVED_29
220	RESERVED_3
221	PHYADD4
222	PHYADD3
223	RESERVED_0
224	NRESET
A1	RESERVED_15
A2	VDD_AH_1
A3	VDD_AH_2

Pins by number *(continued)*

A4	VDD_AH_3
A5	VDD_AH_4
A6	VSS_1
A7	VDD_AH_5
A8	VDD_AH_6
A9	VDD_AH_7
A10	VDD_34
A11	RESERVED_24
A12	MDINT
A13	VSS_2
A14	ESLED1_LD
A15	ESLED0_DO / GPIO_2
A16	RESERVED_18
A17	RESERVED_17
A18	VSS_163
A19	VSS_3
A20	SERDES_E3_RXP
A21	SERDES_E3_RXN
A22	SERDES_E3_TXP
A23	SERDES_E3_TXN
A24	VSS_4
A25	SERDES_E2_TXN
A26	SERDES_E2_TXP
A27	SERDES_E2_RXN
A28	SERDES_E2_RXP
A29	VSS_5
A30	SERDES_E1_RXP
A31	SERDES_E1_RXN
A32	SERDES_E1_TXP
A33	SERDES_E1_TXN
A34	VSS_6
A35	RESERVED_103
A36	RESERVED_102
A37	RESERVED_101
A38	RESERVED_100
A39	VSS_7
A40	VSS_8
A41	VSS_9
A42	VSS_10
A43	VDD_35
A44	VDD_36
A45	VDD_37
A46	VSS_11
A47	VDD_AH_8
A48	VDD_AH_9
A49	VDD_AH_10
A50	VDD_AH_11
A51	VDD_AH_12
A52	VSS_12
A53	VDD_AH_13
A54	VDD_AH_14
A55	VDD_AH_15
A56	RESERVED_10
A57	RESERVED_11
A58	VSS_13
A59	VDD_IO_6
A60	VDD_IO_7
A61	VDD_38
A62	VDD_39
A63	VSS_14
A64	VDD_AH_16
A65	VDD_AH_17
A66	VDD_AH_18
A67	VDD_AH_19
A68	VDD_AH_20
A69	VDD_AH_21
A70	VSS_15
A71	VDD_IO_8
A72	VDD_40
A73	VDD_41
A74	VSS_16
A75	VDD_IO_9
A76	VDD_IO_10
A77	VDD_IO_11
A78	RESERVED_14

7.4 Pins by Name

This section provides an alphabetical list of the VSC8522-02 pins.

COMA_MODE	214
ESLED0_CLK	50
ESLED0_DO / GPIO_2	A15
ESLED0_LD	49
ESLED0_PULSE / GPIO_3	47
ESLED1_CLK	45
ESLED1_DO	44
ESLED1_LD	A14
ESLED1_PULSE	43
FAST_LINK_STATUS	38
GPIO_15	42
GPIO_16	41
GPIO_29	40
JTAG_CLK	175
JTAG_DI	174
JTAG_DO	172
JTAG_TMS	173
JTAG_TRST	171
MDC	54
MDINT	A12
MDIO	55
NRESET	224
P0_D0N	138
P0_D0P	139
P0_D1N	136
P0_D1P	137
P0_D2N	134
P0_D2P	135
P0_D3N	131
P0_D3P	132
P1_D0N	146
P1_D0P	147
P1_D1N	144
P1_D1P	145
P1_D2N	142
P1_D2P	143
P1_D3N	140
P1_D3P	141
P10_D0N	27
P10_D0P	28
P10_D1N	25
P10_D1P	26
P10_D2N	23
P10_D2P	24
P10_D3N	21
P10_D3P	22
P11_D0N	35
P11_D0P	36
P11_D1N	33
P11_D1P	34
P11_D2N	31
P11_D2P	32
P11_D3N	29
P11_D3P	30
P2_D0N	156
P2_D0P	157
P2_D1N	154
P2_D1P	155
P2_D2N	152
P2_D2P	153
P2_D3N	150
P2_D3P	151
P3_D0N	165
P3_D0P	166
P3_D1N	163
P3_D1P	164
P3_D2N	161
P3_D2P	162
P3_D3N	158
P3_D3P	159
P4_D0N	182
P4_D0P	184
P4_D1N	180
P4_D1P	181
P4_D2N	178

Pins by name *(continued)*

P4_D2P	179
P4_D3N	176
P4_D3P	177
P5_D0N	191
P5_D0P	192
P5_D1N	189
P5_D1P	190
P5_D2N	187
P5_D2P	188
P5_D3N	185
P5_D3P	186
P6_D0N	202
P6_D0P	203
P6_D1N	199
P6_D1P	200
P6_D2N	197
P6_D2P	198
P6_D3N	195
P6_D3P	196
P7_D0N	210
P7_D0P	211
P7_D1N	208
P7_D1P	209
P7_D2N	206
P7_D2P	207
P7_D3N	204
P7_D3P	205
P8_D0N	8
P8_D0P	9
P8_D1N	6
P8_D1P	7
P8_D2N	4
P8_D2P	5
P8_D3N	2
P8_D3P	3
P9_D0N	16
P9_D0P	17
P9_D1N	14
P9_D1P	15
P9_D2N	12
P9_D2P	13
P9_D3N	10
P9_D3P	11
PHYADD3	222
PHYADD4	221
REF_FILT_0	148
REF_FILT_1	193
REF_FILT_2	18
REF_REXT_0	149
REF_REXT_1	194
REF_REXT_2	19
REFCLK_N	69
REFCLK_P	70
REFCLK_SEL0	216
REFCLK_SEL1	217
REFCLK_SEL2	215
RESERVED_0	223
RESERVED_3	220
RESERVED_4	218
RESERVED_5	167
RESERVED_6	168
RESERVED_7	169
RESERVED_8	170
RESERVED_10	A56
RESERVED_11	A57
RESERVED_12	212
RESERVED_13	213
RESERVED_14	A78
RESERVED_15	A1
RESERVED_17	A17
RESERVED_18	A16
RESERVED_22	66
RESERVED_23	65
RESERVED_24	A11
RESERVED_25	53
RESERVED_26	52

Pins by name *(continued)*

RESERVED_27	48
RESERVED_28	51
RESERVED_29	219
RESERVED_30	46
RESERVED_100	A38
RESERVED_101	A37
RESERVED_102	A36
RESERVED_103	A35
SERDES_E1_RXN	A31
SERDES_E1_RXP	A30
SERDES_E1_TXN	A33
SERDES_E1_TXP	A32
SERDES_E2_RXN	A27
SERDES_E2_RXP	A28
SERDES_E2_TXN	A25
SERDES_E2_TXP	A26
SERDES_E3_RXN	A21
SERDES_E3_RXP	A20
SERDES_E3_TXN	A23
SERDES_E3_TXP	A22
SERDES_REXT_0	106
SERDES_REXT_1	107
VDD_1	57
VDD_2	58
VDD_3	59
VDD_4	76
VDD_5	77
VDD_6	78
VDD_7	86
VDD_8	87
VDD_9	88
VDD_10	89
VDD_11	90
VDD_12	99
VDD_13	100
VDD_14	101
VDD_15	102
VDD_16	105

VDD_17	109
VDD_18	110
VDD_19	111
VDD_20	112
VDD_21	113
VDD_22	114
VDD_23	115
VDD_24	116
VDD_25	117
VDD_26	118
VDD_27	119
VDD_28	120
VDD_29	121
VDD_30	122
VDD_31	123
VDD_32	124
VDD_33	125
VDD_34	A10
VDD_35	A43
VDD_36	A44
VDD_37	A45
VDD_38	A61
VDD_39	A62
VDD_40	A72
VDD_41	A73
VDD_A_1	60
VDD_A_2	63
VDD_A_3	64
VDD_A_4	68
VDD_A_5	71
VDD_A_6	72
VDD_A_7	74
VDD_A_8	80
VDD_A_9	82
VDD_A_10	85
VDD_A_11	91
VDD_A_12	93
VDD_A_13	95

Pins by name *(continued)*

VDD_A_14	98
VDD_A_15	104
VDD_AH_1	A2
VDD_AH_2	A3
VDD_AH_3	A4
VDD_AH_4	A5
VDD_AH_5	A7
VDD_AH_6	A8
VDD_AH_7	A9
VDD_AH_8	A47
VDD_AH_9	A48
VDD_AH_10	A49
VDD_AH_11	A50
VDD_AH_12	A51
VDD_AH_13	A53
VDD_AH_14	A54
VDD_AH_15	A55
VDD_AH_16	A64
VDD_AH_17	A65
VDD_AH_18	A66
VDD_AH_19	A67
VDD_AH_20	A68
VDD_AH_21	A69
VDD_AL_1	1
VDD_AL_2	20
VDD_AL_3	37
VDD_AL_4	126
VDD_AL_5	127
VDD_AL_6	128
VDD_AL_7	129
VDD_AL_8	130
VDD_AL_9	133
VDD_AL_10	160
VDD_AL_11	183
VDD_AL_12	201
VDD_IO_1	39
VDD_IO_2	56
VDD_IO_3	67
VDD_IO_4	83
VDD_IO_5	108
VDD_IO_6	A59
VDD_IO_7	A60
VDD_IO_8	A71
VDD_IO_9	A75
VDD_IO_10	A76
VDD_IO_11	A77
VDD_VS_1	61
VDD_VS_2	62
VDD_VS_3	73
VDD_VS_4	75
VDD_VS_5	79
VDD_VS_6	81
VDD_VS_7	84
VDD_VS_8	92
VDD_VS_9	94
VDD_VS_10	96
VDD_VS_11	97
VDD_VS_12	103
VSS_1	A6
VSS_2	A13
VSS_3	A19
VSS_4	A24
VSS_5	A29
VSS_6	A34
VSS_7	A39
VSS_8	A40
VSS_9	A41
VSS_10	A42
VSS_11	A46
VSS_12	A52
VSS_13	A58
VSS_14	A63
VSS_15	A70
VSS_16	A74
VSS_163	A18

8 Package Information

VSC8522XJQ-02 and VSC8522XJQ-04 are packaged in a lead-free (Pb-free), 302-pin, plastic thin quad flat package (TQFP) with an exposed pad, 24 mm × 24 mm body size, 1 mm body thickness, 0.4 mm pin pitch for the outer leads, 0.5 mm pin pitch for the inner leads, and 1.2 mm maximum height.

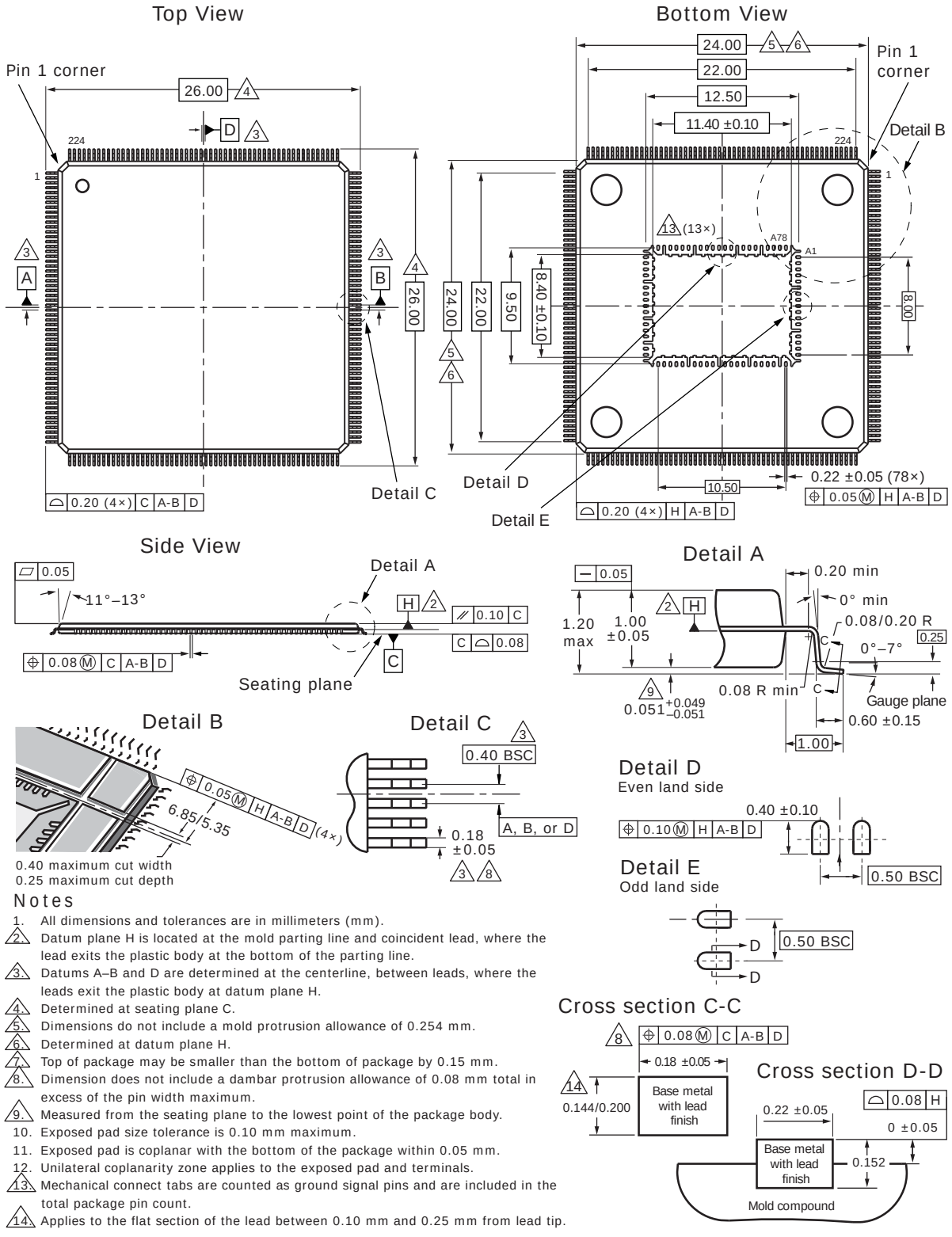
Lead-free products from Microsemi comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the device.

8.1 Package Drawing

The following illustration shows the package drawing for the device. The drawing contains the top view, bottom view, side view, detail views, dimensions, tolerances, and notes.

Figure 30 • **Package Drawing**



Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Datum plane H is located at the mold parting line and coincident lead, where the lead exits the plastic body at the bottom of the parting line.
3. Datums A–B and D are determined at the centerline, between leads, where the leads exit the plastic body at datum plane H.
4. Determined at seating plane C.
5. Dimensions do not include a mold protrusion allowance of 0.254 mm.
6. Determined at datum plane H.
7. Top of package may be smaller than the bottom of package by 0.15 mm.
8. Dimension does not include a dambar protrusion allowance of 0.08 mm total in excess of the pin width maximum.
9. Measured from the seating plane to the lowest point of the package body.
10. Exposed pad size tolerance is 0.10 mm maximum.
11. Exposed pad is coplanar with the bottom of the package within 0.05 mm.
12. Unilateral coplanarity zone applies to the exposed pad and terminals.
13. Mechanical connect tabs are counted as ground signal pins and are included in the total package pin count.
14. Applies to the flat section of the lead between 0.10 mm and 0.25 mm from lead tip.

8.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC JESD51 family of documents. These documents are available on the JEDEC Web site at www.jedec.org. The thermal specifications are

modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information about the thermal measurement method used for this device, see the JESD51-1 standard.

Table 100 • **Thermal Resistances**

Symbol	°C/W	Parameter
θ_{JCtop}	5.13	Die junction to package case top
θ_{JB}	7.86	Die junction to printed circuit board
θ_{JA}	15.39	Die junction to ambient
θ_{JMA} at 1 m/s	11.53	Die junction to moving air measured at an air speed of 1 m/s
θ_{JMA} at 2 m/s	9.34	Die junction to moving air measured at an air speed of 2 m/s

To achieve results similar to the modeled thermal measurements, the guidelines for board design described in the JESD51 family of publications must be applied. For information about applications using QFP packages with an exposed pad, see the following:

- JESD51-2A, *Integrated Circuits Thermal Test Method Environmental Conditions, Natural Convection (Still Air)*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions, Forced Convection (Moving Air)*
- JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions, Junction-to-Board*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

8.3 Moisture Sensitivity

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

9 Design Considerations

This section provides information about the design considerations for the VSC8522-02 device.

9.1 10BASE-T mode unable to re-establish link

10BASE-T mode is unable to re-establish link with the following devices if the link drops while sending data: SparX-III™ and Caracal™ family of switches, VSC8512-02, VSC8522-02, VSC8522-12, VSC8504, VSC8552, VSC8572, and VSC8574. No issue is observed for other link partner devices. The probability of this error occurring is low except in a test environment.

The workaround is to contact Microsemi for the current API software release.

This item was previously published in the VSC8522-02 Errata revision 1.0 as EA100054.

9.2 Software script for link performance

Software script is required for improved link performance. PHY ports may exhibit suboptimal performance. Contact Microsemi for a script to be applied during system initialization.

This item was previously published in the VSC8522-02 Errata revision 1.0 as EA100034.

9.3 10BASE-T signal amplitude

10BASE-T signal amplitude can be lower than the minimum specified in IEEE 802.3 paragraph 14.3.1.2.1 (2.2 V) at low supply voltages. This issue is not estimated to present any system level impact. Performance is not impaired with cables up to 130 m with various link partners.

This item was previously published in the VSC8522-02 Errata revision 1.0 as EA100036.

9.4 Clause 45 register 7.60

Clause 45, register 7.60, bit 10 reads back as a logic 1. This is a reserved bit in the standard and should be ignored by software.

This item was previously published in the VSC8522-02 Errata revision 1.0 as EA100037.

9.5 Clause 45 register 3.22

Clause 45, register 3.22 is cleared upon read only when extended page access register (register 31) is set to 0. This register cannot be read when page access register is set to a value other than 0.

The workaround is to set the extended page access register to 0 before accessing clause 45, register 3.22.

This item was previously published in the VSC8522-02 Errata revision 1.0 as EA100038.

9.6 Clause 45 register 3.1

Clause 45, register 3.1, Rx and Tx LPI received bits are cleared upon read only when extended page access register (register 31) is set to 0.

The workaround is to set the extended page access register to 0 before accessing clause 45, register 3.1.

This item was previously published in the VSC8522-02 Errata revision 1.0 as EA100039.

9.7 Clause 45 register address post-increment

Clause 45 register address post-increment only works when reading registers and only when the extended page access register (register 31) is set to 0. The estimated impact is low, as there are very few Clause 45 registers in a Gigabit PHY, and they can be addressed individually.

The workaround is to access Clause 45 registers individually.

This item was previously published in the VSC8522-02 Errata revision 1.0 as EA100040.

10 Ordering Information

The device is offered with two operating temperature ranges. The range for VSC8522-02 is 0 °C ambient to 125 °C junction. The range for VSC8522-04 is
–40 °C ambient to 125 °C junction.

VSC8522XJQ-02 and VSC8522XJQ-04 are packaged in a lead-free (Pb-free), 302-pin, plastic thin quad flat package (TQFP) with an exposed pad, 24 mm × 24 mm body size, 1 mm body thickness, 0.4 mm pin pitch for the outer leads, 0.5 mm pin pitch for the inner leads, and 1.2 mm maximum height.

Lead-free products from Microsemi comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the device.

Table 101 • **Ordering Information**

Part Order Number	Description
VSC8522XJQ-02	Lead-free, 302-pin, plastic TQFP with an exposed pad, 24 mm × 24 mm body size, 1 mm body thickness, 0.4 mm pin pitch for the outer leads, 0.5 mm pin pitch for the inner leads, and 1.2 mm maximum height. The operating temperature is 0 °C ambient to 125 °C junction.
VSC8522XJQ-04	Lead-free, 302-pin, plastic TQFP with an exposed pad, 24 mm × 24 mm body size, 1 mm body thickness, 0.4 mm pin pitch for the outer leads, 0.5 mm pin pitch for the inner leads, and 1.2 mm maximum height. The operating temperature is –40 °C ambient to 125 °C junction.