

# FDZ2553N

## Monolithic Common Drain N-Channel 2.5V Specified PowerTrench® BGA MOSFET

### General Description

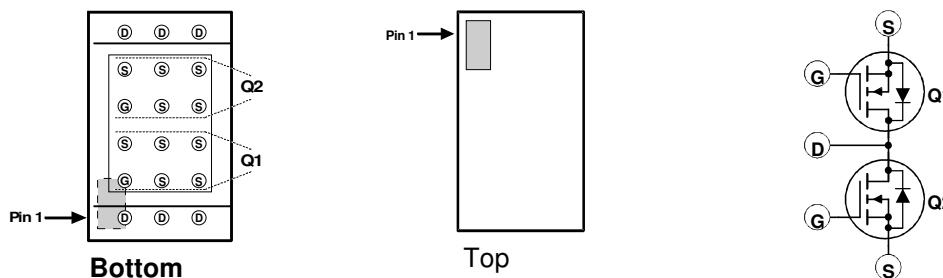
Combining Fairchild's advanced 2.5V specified PowerTrench process with state-of-the-art BGA packaging, the FDZ2553N minimizes both PCB space and  $R_{DS(ON)}$ . This Monolithic Common Drain BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, and low  $R_{DS(ON)}$ .

### Applications

- Battery management
- Load switch
- Battery protection

### Features

- 9.6 A, 20 V.  $R_{DS(ON)} = 14 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$   
 $R_{DS(ON)} = 20 \text{ m}\Omega @ V_{GS} = 2.5 \text{ V}$
- Occupies only 0.10 cm<sup>2</sup> of PCB area: 1/3 the area of SO-8.
- Ultra-thin package: less than 0.80 mm height when mounted to PCB.
- Outstanding thermal transfer characteristics: significantly better than SO-8.
- Ultra-low  $Q_g \times R_{DS(ON)}$  figure-of-merit
- High power and current handling capability



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	20	V
V <sub>GSS</sub>	Gate-Source Voltage	±12	V
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	9.6	A
		20	
P <sub>D</sub>	Power Dissipation (Steady State) (Note 1a)	2.1	W
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	60	°C/W
R <sub>θJB</sub>	Thermal Resistance, Junction-to-Ball (Note 1)	6.3	
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	0.6	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
2553N	FDZ2553N	7"	12mm	3000 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		14		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6	0.9	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 9.6\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 7.9\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 9.6\text{ A}, T_J = 125^\circ\text{C}$		11 15 15	14 20 20	m $\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	10			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 9.6\text{ A}$		45		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$		1299		pF
$C_{oss}$	Output Capacitance	$f = 1.0\text{ MHz}$		317		pF
$C_{riss}$	Reverse Transfer Capacitance			166		pF

**Switching Characteristics** (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A},$		9.0	18	ns
$t_r$	Turn–On Rise Time	$V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		11	20	ns
$t_{d(off)}$	Turn–Off Delay Time			29	46	ns
$t_f$	Turn–Off Fall Time			11	20	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 9.6\text{ A},$		12	17	nC
$Q_{gs}$	Gate–Source Charge	$V_{GS} = 4.5\text{ V}$		2.3		nC
$Q_{gd}$	Gate–Drain Charge			3.2		nC

**Drain–Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain–Source Diode Forward Current				1.7	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.7\text{ A}$ (Note 2)		0.7	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 9.6\text{ A},$		21		nS
$Q_{rr}$	Diode Reverse Recovery Charge	$d_{IF}/d_t = 100\text{ A}/\mu\text{s}$		13		nC

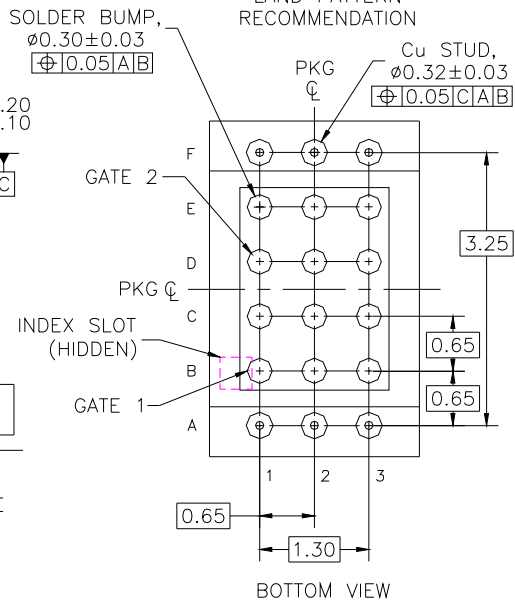
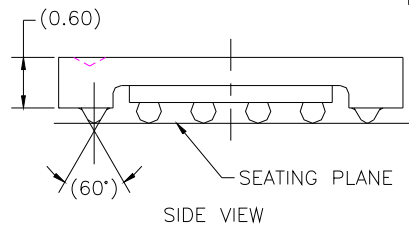
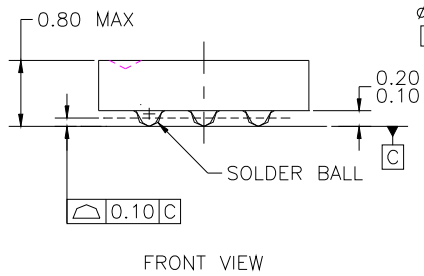
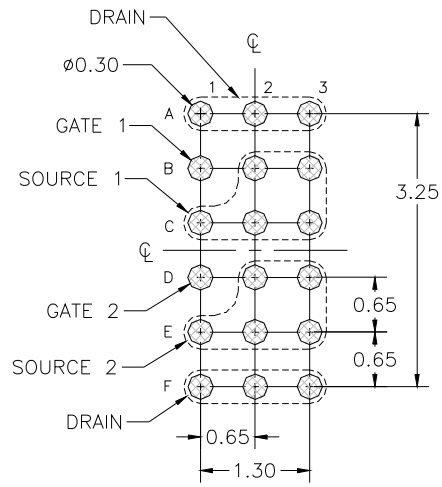
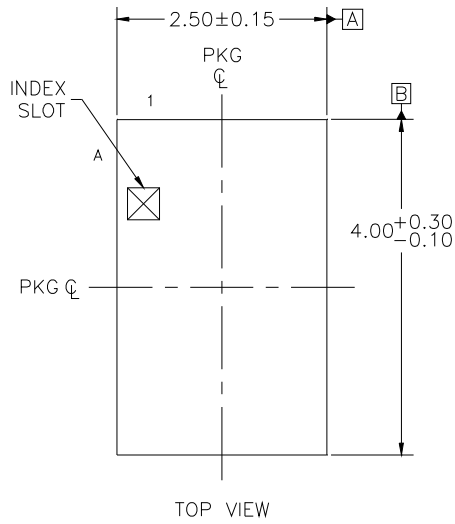
**Notes:**

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. The thermal resistance from the junction to the circuit board side of the solder ball,  $R_{\theta JB}$ , is defined for reference. For  $R_{\theta JC}$ , the thermal reference point for the case is defined as the top surface of the copper chip carrier.  $R_{\theta JC}$  and  $R_{\theta JB}$  are guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.

- $R_{\theta JA} = 60^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB
- $R_{\theta JA} = 108^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) NO JEDEC REGISTRATION REFERENCE AS OF JULY 1999.
- C) BALL CONFIGURATION TABLE

TERMINAL	DESIGNATION
A1,A2,A3,F1,F2,F3	DRAIN
B1	GATE 1
B2,B3,C1,C2,C3	SOURCE 1
D1	GATE 2
D2,D3,E1,E2,E3	SOURCE 2

BGA12AREVC

Typical Characteristics

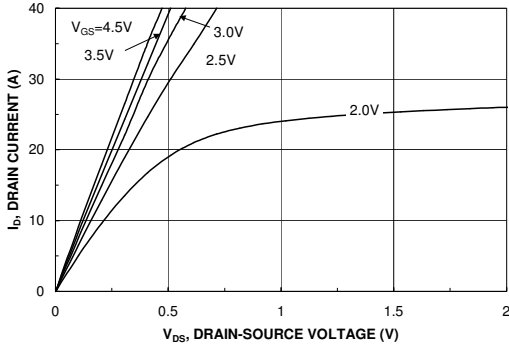


Figure 1. On-Region Characteristics.

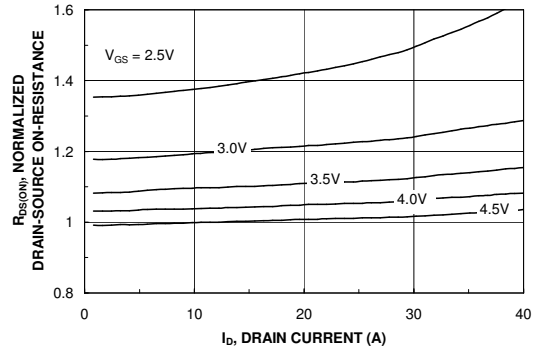


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

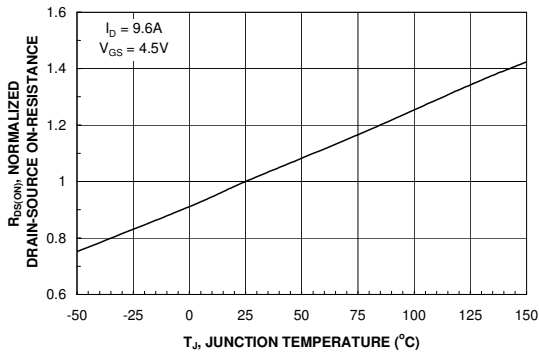


Figure 3. On-Resistance Variation with Temperature.

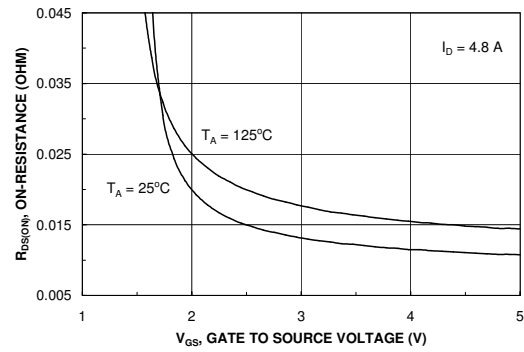


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

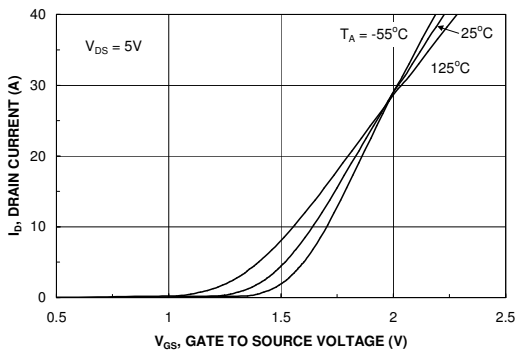


Figure 5. Transfer Characteristics.

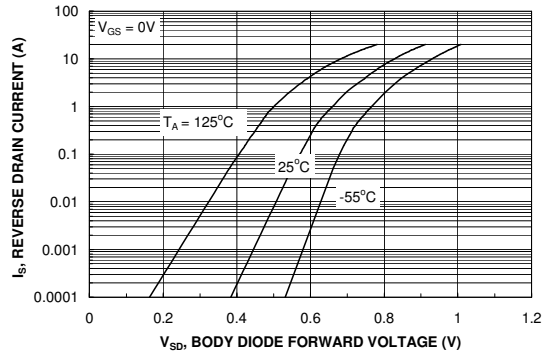


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

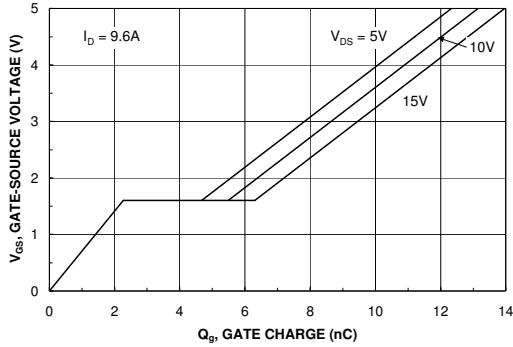


Figure 7. Gate Charge Characteristics.

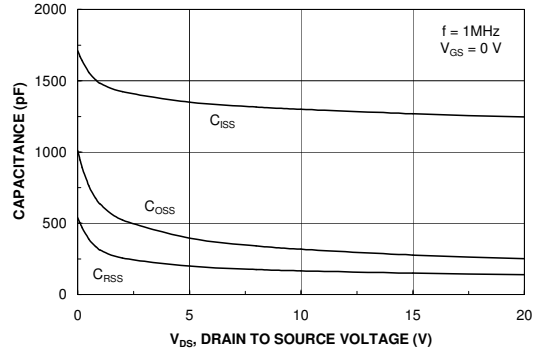


Figure 8. Capacitance Characteristics.

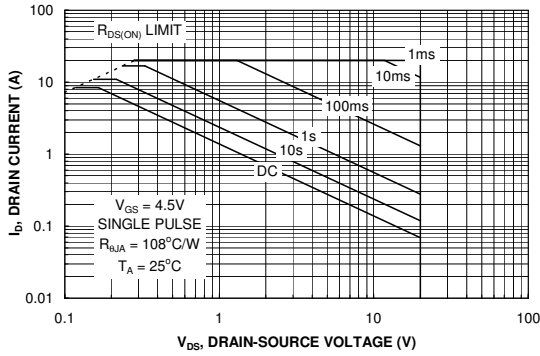


Figure 9. Maximum Safe Operating Area.

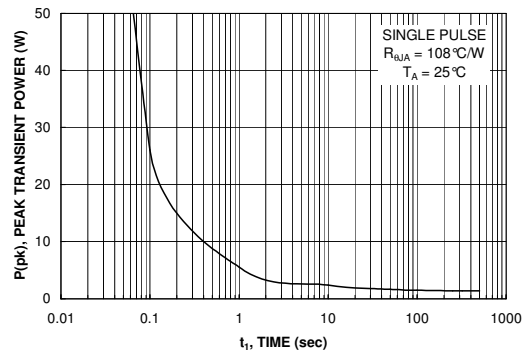


Figure 10. Single Pulse Maximum Power Dissipation.

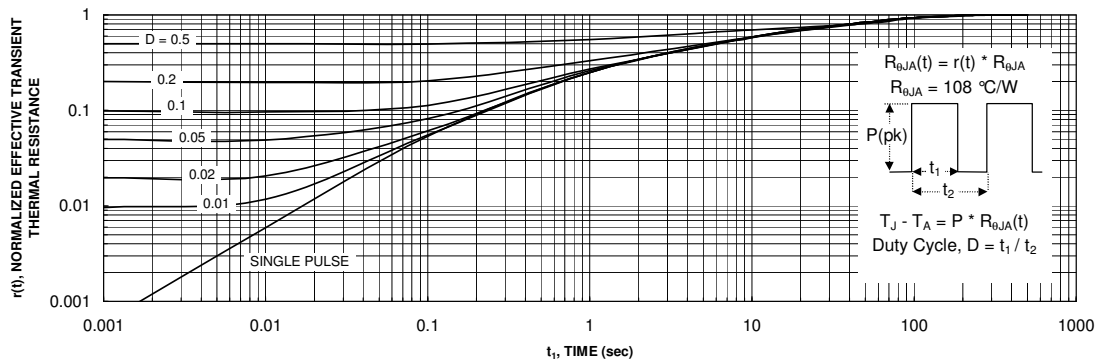


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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