Rochester Electronics®

Datasheet

CD54/74HC/HCT160, CD54/74HC/HCT161 CD54/74HC/HCT162, CD54/74HC/HCT163

High-Speed CMOS Logic

The RCA-CD54/74HC/HCT160, 161, 162, and 163 devices are presettable synchronous counters that feature look-ahead carry logic for use in high-speed counting applications. The CD54/74HC/HCT160 and 161 are asynchronous reset decade and binary counters, respectively; the CD54/74HC/HCT162 and 163 devices are decade and binary counters, respectively and are reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

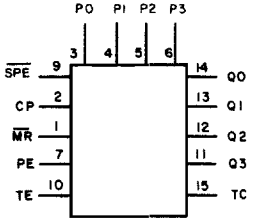
FOR REFERENCE ONLY

File Number **1550**

CD54/74HC/HCT160, CD54/74HC/HCT161 CD54/74HC/HCT162, CD54/74HC/HCT163

High-Speed CMOS Logic

FUNCTIONAL DIAGRAM



92CS-37958

Presettable Counters

CD54/74HC/HCT160 BCD Decade Counter, Asynchronous Reset
CD54/74HC/HCT161 4-Bit Binary Counter, Asynchronous Reset
CD54/74HC/HCT162 BCD Decade Counter, Synchronous Reset
CD54/74HC/HCT163 4-Bit Binary Counter, Synchronous Reset

Type Features:

- *Synchronous Counting and Loading*
- *Two Count Enable Inputs for n-Bit Cascading*
- *Asynchronous Reset (CD54/74HC/HCT160, 161)*
- *Synchronous Reset (CD54/74HC/HCT162, 163)*
- *Look-Ahead Carry for High-Speed Counting*

The RCA-CD54/74HC/HCT160, 161, 162, and 163 devices are presettable synchronous counters that feature look-ahead carry logic for use in high-speed counting applications. The CD54/74HC/HCT160 and 161 are asynchronous reset decade and binary counters, respectively; the CD54/74HC/HCT162 and 163 devices are decade and binary counters, respectively and are reset synchronously with the clock. Counting and parallel presetting are both accomplished synchronously with the negative-to-positive transition of the clock.

A low level on the synchronous parallel enable input, $\overline{SPE}$, disables the counting operation and allows data at the P0 to P3 inputs to be loaded into the counter (provided that the setup and hold requirements for $\overline{SPE}$ are met).

All counters are reset with a low level on the Master Reset input, $\overline{MR}$. In the CD54/74HC/HCT162 and 163 counters (synchronous reset types), the requirements for setup and hold time with respect to the clock must be met.

Two count enables, PE and TE, in each counter are provided for n-bit cascading. In all counters reset action occurs regardless of the level of the $\overline{SPE}$, PE and TE inputs (and the clock input, CP, in the CD54/74HC/HCT160 and 161 types).

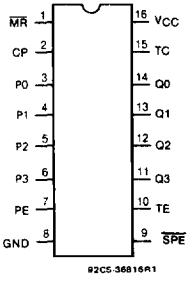
If a decade counter is preset to an illegal state or assumes an illegal state when power is applied, it will return to the normal sequence in one count as shown in state diagram.

The look-ahead carry feature simplifies serial cascading of the counters. Both count enable inputs (PE and TE) must be high to count. The TE input is gated with the Q outputs of all four stages so that at the maximum count the terminal count (TC) output goes high for one clock period. This TC pulse is used to enable the next cascaded stage.

The CD54HC160 through 163 and the CD54HCT160 through 163 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC160 through 163 and the CD74HCT160 through 163 are supplied in 16-lead dual-in-line plastic packages (E suffix), and in 16-lead dual-in-line surface mount plastic packages (M suffix). All types are also supplied in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



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TERMINAL ASSIGNMENT

CD54/74HC/HCT160, CD54/74HC/HCT161
CD54/74HC/HCT162, CD54/74HC/HCT163

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC} +0.5$ V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC} +0.5$ V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V $< V_O < V_{CC} +0.5$ V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}): ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) ..... **400 mW**
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... **Derate Linearly at 6 mW/° C to 70 mW**
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125° C
PACKAGE TYPE E, M ..... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

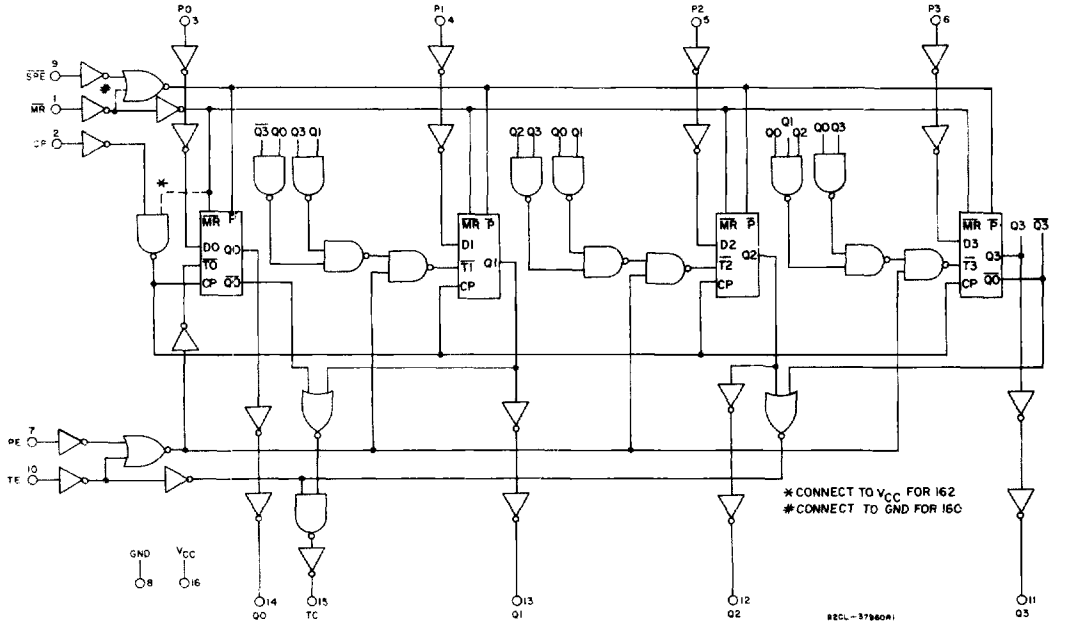
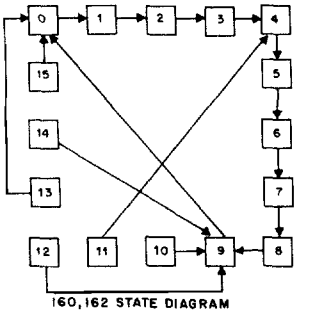


Fig. 1 - Logic diagram for the CD54/74HC/HCT160 and 162.



160, 162 STATE DIAGRAM

92CS-40259R1

NOTE: ILLEGAL STATES IN BCD COUNTERS CORRECTED IN ONE COUNT.

CD54/74HC/HCT160, CD54/74HC/HCT161
CD54/74HC/HCT162, CD54/74HC/HCT163

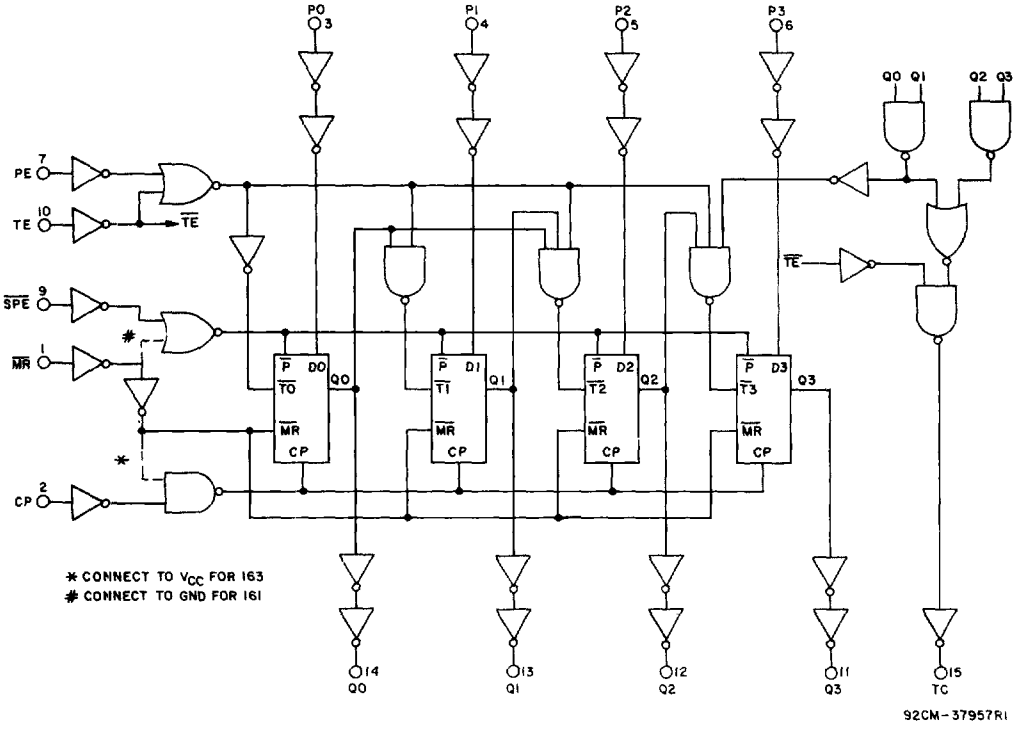


Fig. 2 - Logic diagram for the CD54/74HC/HCT161 and 163.

MODE SELECT - FUNCTION TABLE, 160, 161

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	P_n	Q_n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(a)
Count	H	↑	h	h	h(c)	X	count	(a)
Inhibit	H	X	l(b)	X	h(c)	X	q_n	(a)
	H	X	X	l(b)	h(c)	X	q_n	L

CD54/74HC/HCT160, CD54/74HC/HCT161
CD54/74HC/HCT162, CD54/74HC/HCT163

MODE SELECT - FUNCTION TABLE, 162, 163

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	PE	TE	$\overline{SPE}$	P_n	Q_n	TC
Reset (Clear)	l	⎍	X	X	X	X	L	L
Parallel Load	h(f)	⎍	X	X	l	l	L	L
	h(f)	⎍	X	X	l	h	H	(d)
Count	h(f)	⎍	h	h	h(f)	X	count	(d)
Inhibit	h(f)	X	l(e)	X	h(f)	X	q_n	(d)
	h(f)	X	X	l(e)	h(f)	X	q_n	L

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
⎍ = LOW-to-HIGH clock transition.

NOTES
(a) The TC output is HIGH when TE is HIGH and the counter is at Terminal Count (HHHH for 161 and HLLH for 160).
(b) The HIGH-to-LOW transition of PE or TE on the 54/74161 and 54/74160 should only occur while CP is HIGH for conventional operation.
(c) The LOW-to-HIGH transition of $\overline{SPE}$ on the 54/74161 and 54/74160 should only occur while CP is HIGH for conventional operation.
(d) The TC output is HIGH when TE is HIGH and the counter is at Terminal Count (HLLH for 162 and HHHH for 163).
(e) The HIGH-to-LOW transition of PE or TE on the 54/74163 should only occur while CP is HIGH for conventional operation.
(f) The LOW-to-HIGH transition of $\overline{SPE}$ or $\overline{MR}$ on the 54/74163 should only occur while CP is HIGH for conventional operation.

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

*Unless otherwise specified, all voltages are referenced to Ground.

CD54/74HC/HCT160, CD54/74HC/HCT161
CD54/74HC/HCT162, CD54/74HC/HCT163

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC160-163/CD54HC160-163									CD74HCT160-163/CD54HCT160-163								UNITS
	TEST CONDITIONS			74HC/54HC SERIES			74HC SERIES		54HC SERIES	TEST CONDITIONS		74HCT/54HCT SERIES			74HCT SERIES		54HCT SERIES	
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C	V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C	
				Min	Typ	Max	Min	Max	Min Max			Min	Typ	Max	Min	Max	Min Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5 —	—	4.5 to 5.5	2	—	—	2	—	2 —	V
			4.5	3.15	—	—	3.15	—	3.15 —									
			6	4.2	—	—	4.2	—	4.2 —									
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	— 0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	— 0.8	V
			4.5	—	—	1.35	—	1.35	— 1.35									
			6	—	—	1.8	—	1.8	— 1.8									
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9 —	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4 —	V
			4.5	4.4	—	—	4.4	—	4.4 —									
			6	5.9	—	—	5.9	—	5.9 —									
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7 —	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7 —	V
		-5.2	6	5.48	—	—	5.34	—	5.2 —									
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	— 0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	— 0.1	V
			4.5	—	—	0.1	—	0.1	— 0.1									
			6	—	—	0.1	—	0.1	— 0.1									
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	— 0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	— 0.4	V
		5.2	6	—	—	0.26	—	0.33	— 0.4									
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	— ±1	Any Voltage Between V_{CC} and Gnd	5.5	—	—	±0.1	—	±1	— ±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	— 160	V_{CC} or Gnd	5.5	—	—	8	—	80	— 160	μA
Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*										V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	— 490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads *
P0-P3	0.25
PE	0.65
CP	1.05
$\overline{MR}$	0.8
$\overline{SPE}$	0.5
TE	1.05

*Unit load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

CD54/74HC/HCT160, CD54/74HC/HCT161
CD54/74HC/HCT162, CD54/74HC/HCT163

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	CL (pF)	TYPICAL 54/74HC	TYPICAL 54/74HCT	UNITS
Propagation Delay CP to TC	t_{PHL}	15	15	18	ns
CP to Qn	t_{PLH}	15	15	16	ns
TE to TC		15	9	13	ns
$\overline{MR}$ to Qn (160, 161)	t_{PHL}	15	18	21	ns
Power Dissipation Capacitance *	C_{PD}	—	60	63	pF

* CPD is used to determine the dynamic power consumption, per package.
$P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 f_o)$ where: f_i = input frequency. f_o = output frequency.
C_L = output load capacitance. V_{CC} = supply voltage.

PREREQUISITE FOR SWITCHING FUNCTION

CHARACTERISTIC	TEST CONDITIONS V_{CC} V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Max. CP Freq. * f_{MAX}	2	6	—	—	—	5	—	—	—	4	—	—	—	MHz
	4.5	30	—	30	—	24	—	24	—	20	—	20	—	
	6	35	—	—	—	28	—	—	—	24	—	—	—	
CP Width (Low) t_{WL}	2	80	—	—	—	100	—	—	—	120	—	—	—	ns
	4.5	16	—	16	—	20	—	20	—	24	—	24	—	
	6	14	—	—	—	17	—	—	—	20	—	—	—	
$\overline{MR}$ Pulse Width t_W 160, 161	2	100	—	—	—	125	—	—	—	150	—	—	—	ns
	4.5	20	—	20	—	25	—	25	—	30	—	30	—	
	6	17	—	—	—	21	—	—	—	26	—	—	—	
Setup Time t_{SU} Pn to CP	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
	4.5	12	—	10	—	15	—	13	—	18	—	15	—	
	6	10	—	—	—	13	—	—	—	15	—	—	—	
Setup Time t_{SU} PE or TE to CP	2	50	—	—	—	65	—	—	—	75	—	—	—	ns
	4.5	10	—	13	—	13	—	16	—	15	—	20	—	
	6	9	—	—	—	11	—	—	—	13	—	—	—	
Setup Time t_{SU} $\overline{SPE}$ to CP	2	60	—	—	—	75	—	—	—	90	—	—	—	ns
	4.5	12	—	12	—	15	—	15	—	18	—	18	—	
	6	10	—	—	—	13	—	—	—	15	—	—	—	
Setup Time t_{SU} $\overline{MR}$ to CP (162, 163)	2	65	—	—	—	80	—	—	—	100	—	—	—	ns
	4.5	13	—	13	—	16	—	16	—	20	—	20	—	
	6	11	—	—	—	14	—	—	—	17	—	—	—	
Hold Time t_H Pn to CP	2	3	—	—	—	3	—	—	—	3	—	—	—	ns
	4.5	3	—	5	—	3	—	5	—	3	—	5	—	
	6	3	—	—	—	3	—	—	—	3	—	—	—	
Hold Time t_H TE or PE to CP	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
	4.5	0	—	3	—	0	—	3	—	0	—	3	—	
	6	0	—	—	—	0	—	—	—	0	—	—	—	
Hold Time 160, t_H $\overline{SPE}$ to CP 162	2	3	—	—	—	3	—	—	—	3	—	—	—	ns
	4.5	3	—	3	—	3	—	3	—	3	—	3	—	
	6	3	—	—	—	3	—	—	—	3	—	—	—	
161, t_H 163	2	0	—	—	—	0	—	—	—	0	—	—	—	ns
	4.5	0	—	3	—	0	—	3	—	0	—	3	—	
	6	0	—	—	—	0	—	—	—	0	—	—	—	
Recovery Time 160 t_{REC} $\overline{MR}$ to CP 161	2	75	—	—	—	95	—	—	—	110	—	—	—	ns
	4.5	15	—	15	—	19	—	19	—	22	—	22	—	
	6	13	—	—	—	16	—	—	—	19	—	—	—	

* Applies to non-cascaded operation only. With cascaded counters clock to terminal count propagation delays, count enables (PE or TE)-to-clock set-up times, and count enables (PE or TE)-to-clock hold times determine max. clock frequency. For example with these HC devices:

$$f_{max}\,(CP) = \frac{1}{\text{CP-to-TC prop. delay + TE-to-CP setup + TE-to-CP Hold}} = \frac{1}{37 + 10 + 0} \approx 21\ \text{MHz (min.)}$$

CD54/74HC/HCT160, CD54/74HC/HCT161
CD54/74HC/HCT162, CD54/74HC/HCT163

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay CP to TC	t_{PLH}	2	—	185	—	—	—	230	—	—	—	280	—	—	
	t_{PHL}	4.5	—	37	—	42	—	46	—	53	—	56	—	63	ns
		6	—	31	—	—	—	39	—	—	—	48	—	—	
CP to Qn	t_{PLH}	2	—	185	—	—	—	230	—	—	—	280	—	—	
	t_{PHL}	4.5	—	37	—	39	—	46	—	49	—	56	—	59	ns
		6	—	31	—	—	—	39	—	—	—	48	—	—	
TE to TC	t_{PLH}	2	—	120	—	—	—	150	—	—	—	180	—	—	
	t_{PHL}	4.5	—	24	—	32	—	30	—	40	—	36	—	48	ns
		6	—	20	—	—	—	26	—	—	—	31	—	—	
$\overline{MR}$ to Qn, (160, 161)	t_{PHL}	2	—	210	—	—	—	265	—	—	—	315	—	—	
		4.5	—	42	—	50	—	53	—	63	—	63	—	75	ns
		6	—	36	—	—	—	45	—	—	—	54	—	—	
$\overline{MR}$ to TC (160, 161)	t_{PHL}	2	—	210	—	—	—	265	—	—	—	315	—	—	
		4.5	—	42	—	50	—	53	—	63	—	63	—	75	ns
		6	—	36	—	—	—	45	—	—	—	54	—	—	
Output Transition Time	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	ns
		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_{IN}		—	10	—	10	—	10	—	10	—	10	—	10	pF

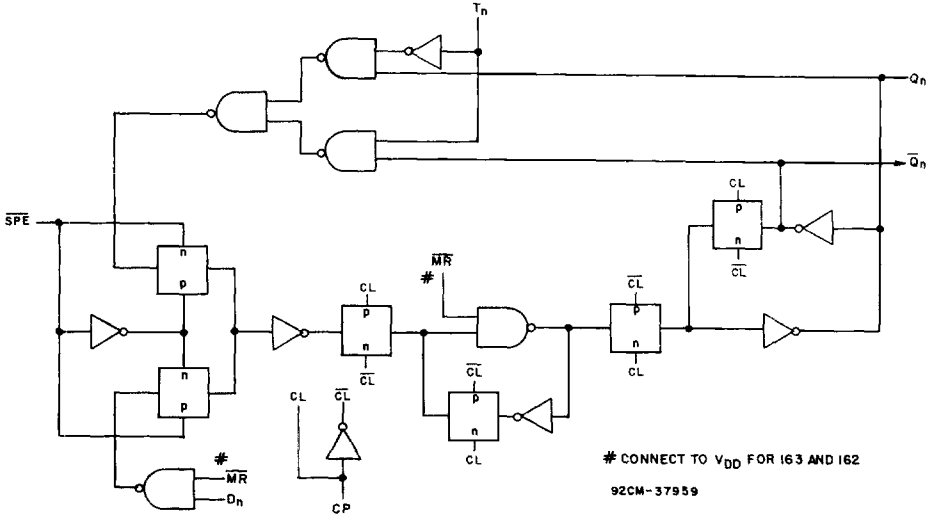
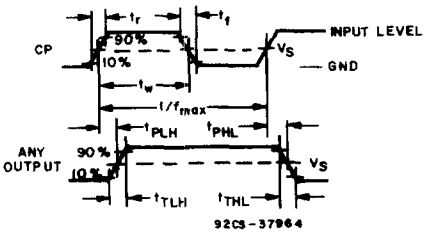
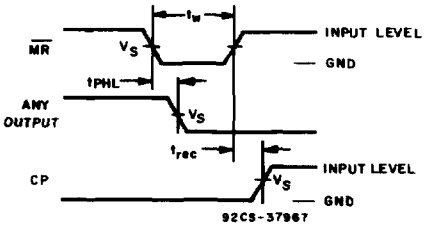


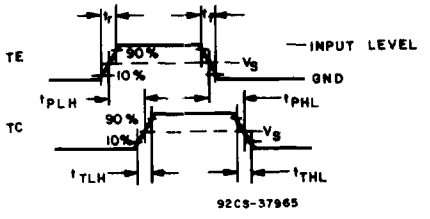
Fig. 3 - Detail of flip-flops for all types.

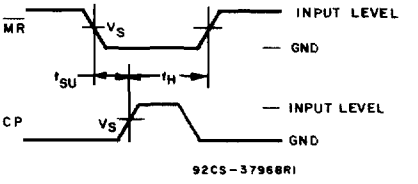
CD54/74HC/HCT160, CD54/74HC/HCT161
CD54/74HC/HCT162, CD54/74HC/HCT163

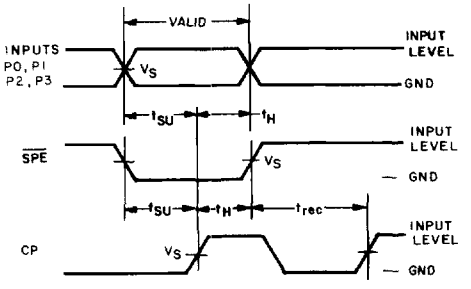
Transition times, propagation delay times, setup, hold, and recovery times.

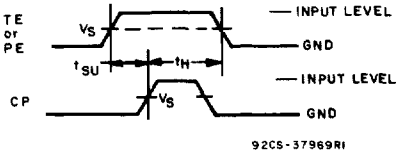










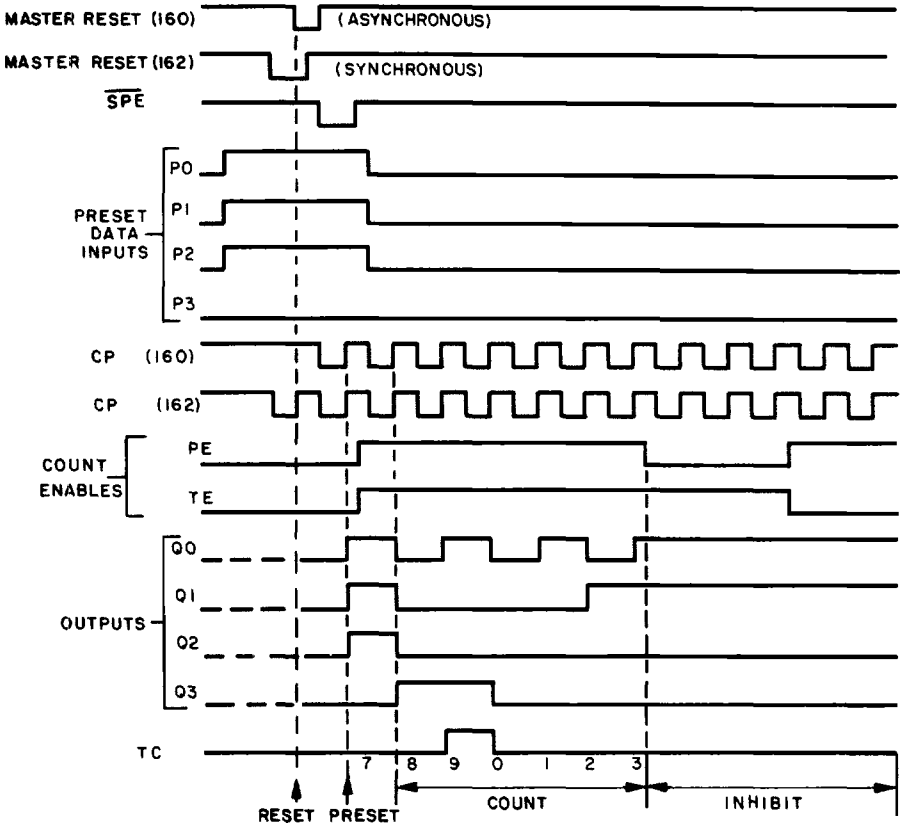


	CD54/74HC	CD54/74HCT
Input Level	V_{CC}	3 V
V_S	0.5 V_{CC}	1.3 V

CD54/74HC/HCT160, CD54/74HC/HCT161
CD54/74HC/HCT162, CD54/74HC/HCT163

Timing diagrams for the CD54/74HC/HCT160 and 162.

Sequence illustrated in waveforms
1. Reset outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit.



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CD54/74HC/HCT160, CD54/74HC/HCT161
CD54/74HC/HCT162, CD54/74HC/HCT163

Timing diagrams for the CD54/74HC/HCT161 and 163.

Sequence illustrated in waveforms
1. **Reset outputs to zero.**
2. **Preset to binary twelve.**
3. **Count to thirteen, fourteen, fifteen, zero, one, and two.**
4. **Inhibit.**