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# FCI25N60N

## N-Channel SupreMOS® MOSFET

600 V, 25 A, 125 mΩ

### Features

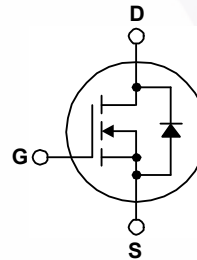
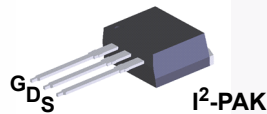
- $R_{DS(on)} = 107\text{ m}\Omega$  (Typ.) @  $V_{GS} = 10\text{ V}$ ,  $I_D = 12.5\text{ A}$
- Ultra Low Gate Charge (Typ.  $Q_g = 57\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 262\text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant

### Application

- Solar Inverter
- AC-DC Power Supply

### Description

The SupreMOS® MOSFET is Fairchild Semiconductor's next generation of high voltage super-junction (SJ) technology employing a deep trench filling process that differentiates it from the conventional SJ MOSFETs. This advanced technology and precise process control provides lowest  $R_{sp}$  on-resistance, superior switching performance and ruggedness. SupreMOS MOSFET is suitable for high frequency switching power converter applications such as PFC, server/telecom power, FPD TV power, ATX power, and industrial power applications.



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCI25N60N_F102	Unit
$V_{DSS}$	Drain to Source Voltage	600	V
$V_{GSS}$	Gate to Source Voltage	$\pm 30$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	25
		- Continuous ( $T_C = 100^\circ\text{C}$ )	16
$I_{DM}$	Drain Current	- Pulsed (Note 1)	75
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	861
$I_{AR}$	Avalanche Current	(Note 1)	8.3
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	2.2
dv/dt	MOSFET dv/dt		100
	Peak Diode Recovery dv/dt	(Note 3)	15
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	216
		- Derate Above $25^\circ\text{C}$	1.72
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FCI25N60N_F102	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.58	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCI25N60N_F102	FCI25N60N	I <sup>2</sup> -PAK	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}, T_J = 25^\circ\text{C}$	600	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 1 \text{ mA}$ , Referenced to $25^\circ\text{C}$	-	0.74	-	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	10	$\mu\text{A}$
		$V_{DS} = 480 \text{ V}, T_J = 125^\circ\text{C}$	-	-	100	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	2.0	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 12.5 \text{ A}$	-	0.107	0.125	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_D = 12.5 \text{ A}$	-	-	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	2520	3352	pF
$C_{oss}$	Output Capacitance		-	103	137	pF
$C_{rss}$	Reverse Transfer Capacitance		-	3.2	5	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 380 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	55	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0 \text{ V to } 480 \text{ V}, V_{GS} = 0 \text{ V}$	-	262	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380 \text{ V}, I_D = 12.5 \text{ A}, V_{GS} = 10 \text{ V}$	-	57	74	nC
$Q_{gs}$	Gate to Source Gate Charge		-	10	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	18	-
ESR	Equivalent Series Resistance (G-S)	$f = 1 \text{ MHz}$	-	1	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380 \text{ V}, I_D = 12.5 \text{ A}, V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	-	21	52	ns
$t_r$	Turn-On Rise Time		-	22	54	ns
$t_{d(off)}$	Turn-Off Delay Time		-	68	146	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	5	20

### Drain-Source Diode Characteristics

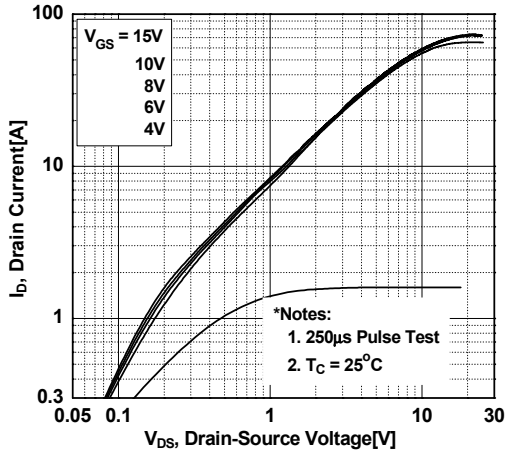
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	25	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	75	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 12.5 \text{ A}$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{SD} = 12.5 \text{ A}$	-	370	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F/dt = 100 \text{ A}/\mu\text{s}$	-	7	-	$\mu\text{C}$

#### Notes:

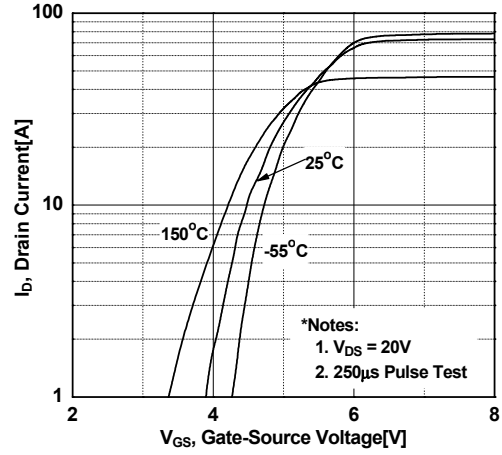
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $I_{AS} = 8.3 \text{ A}, R_G = 25 \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 25 \text{ A}, di/dt \leq 200 \text{ A}/\mu\text{s}, V_{DD} \leq 380 \text{ V}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

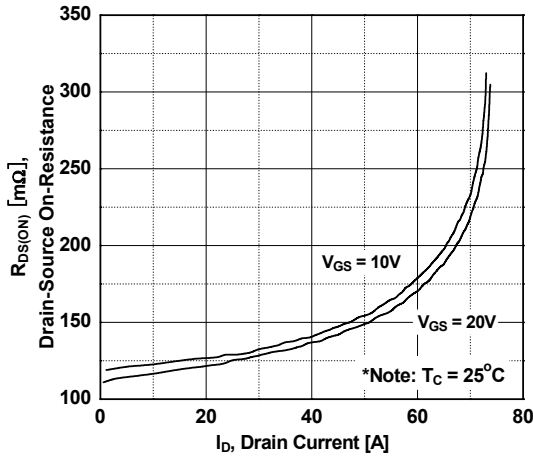
**Figure 1. On-Region Characteristics**



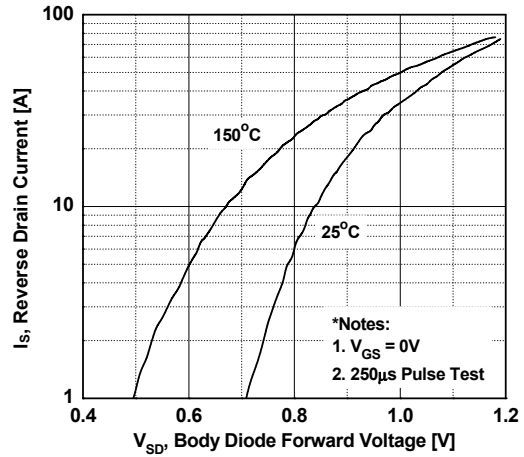
**Figure 2. Transfer Characteristics**



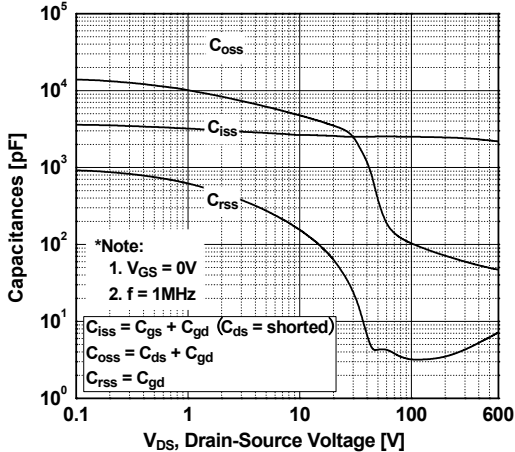
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



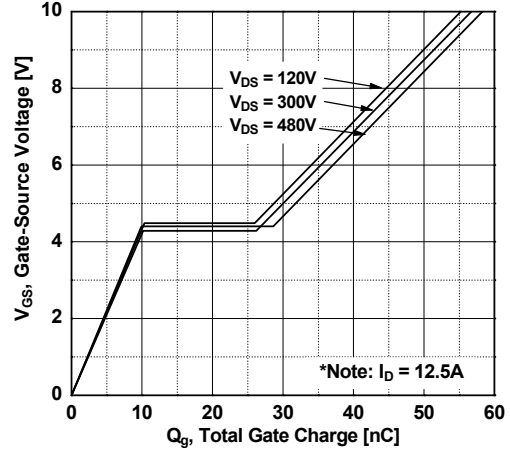
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

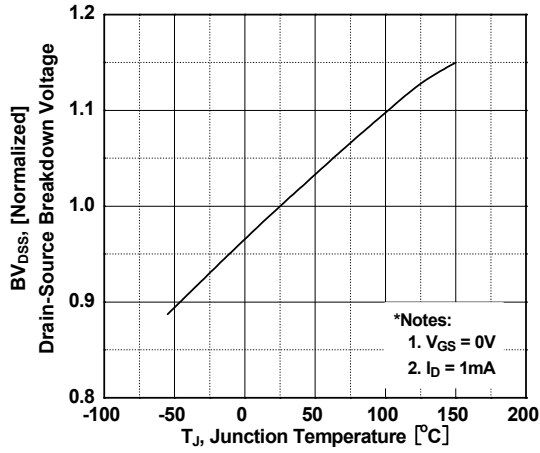


**Figure 6. Gate Charge Characteristics**

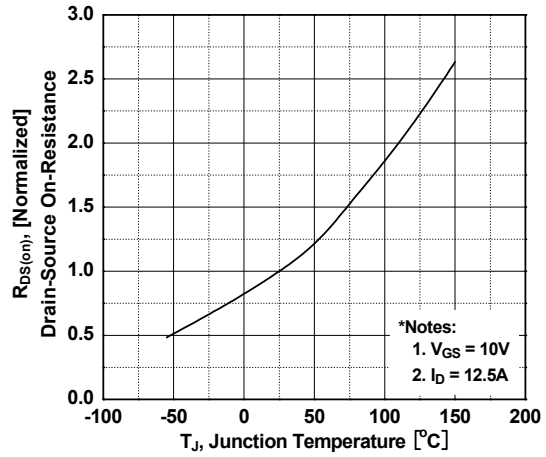


**Typical Performance Characteristics** (Continued)

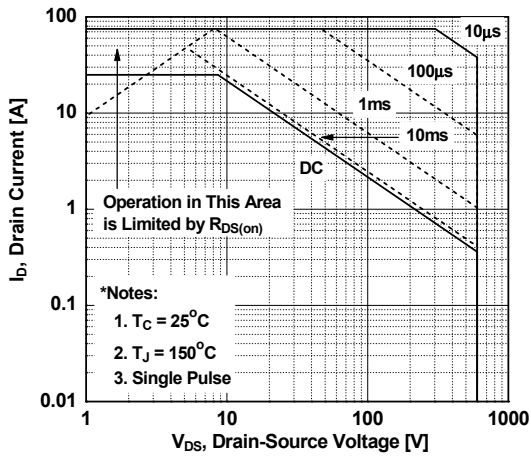
**Figure 7. Breakdown Voltage Variation vs. Temperature**



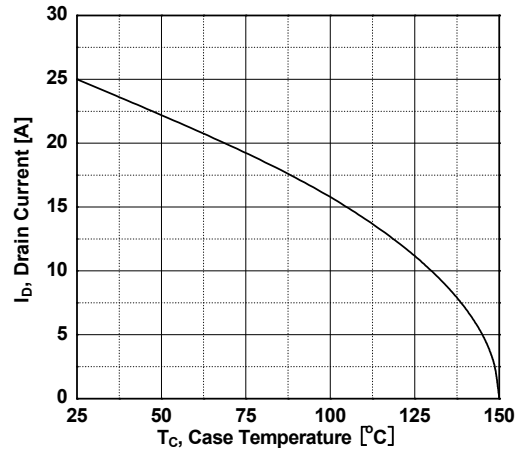
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

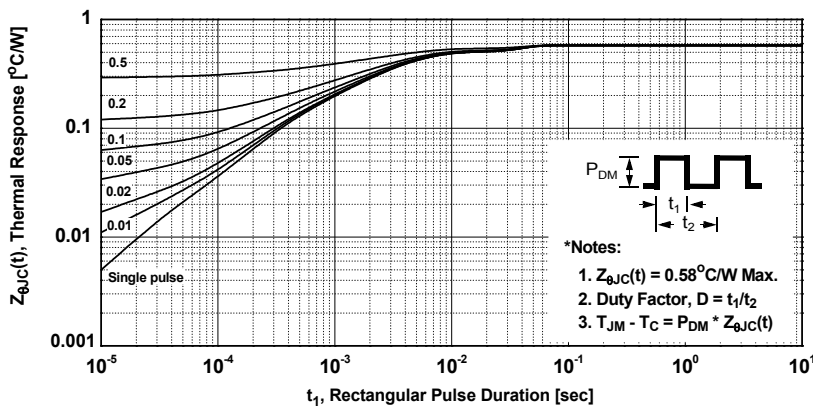




Figure 12. Gate Charge Test Circuit & Waveform



Figure 13. Resistive Switching Test Circuit & Waveforms

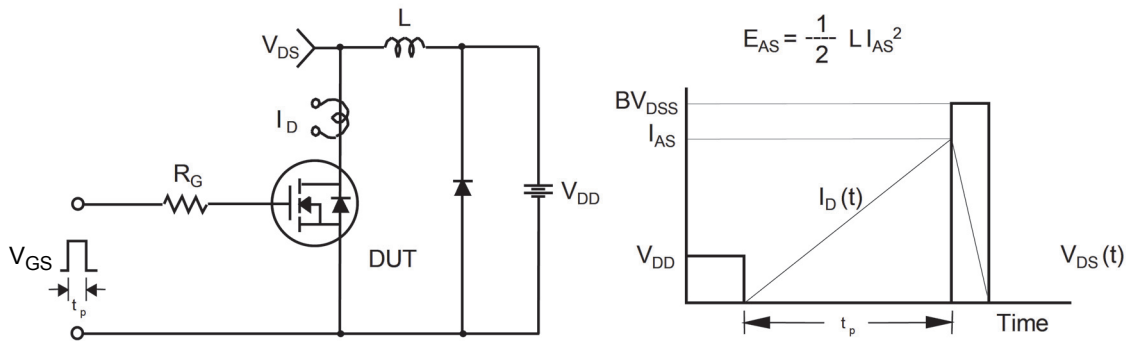
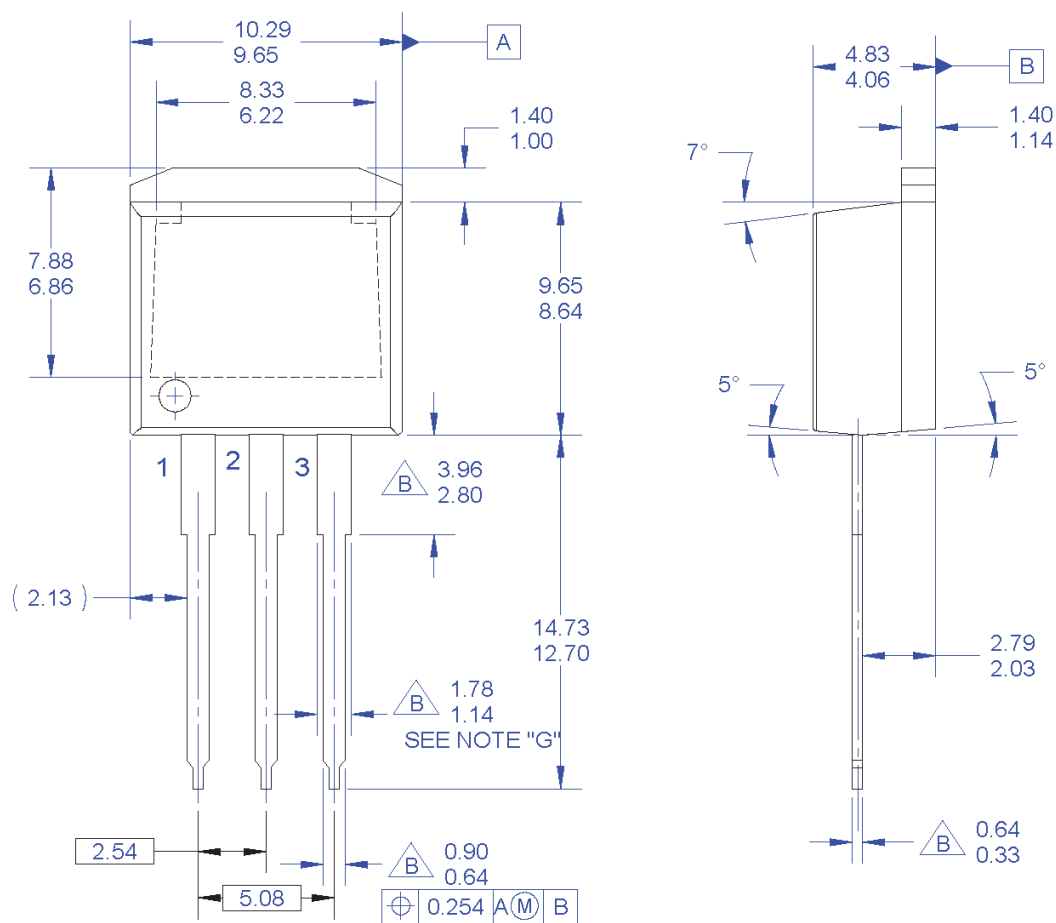


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



**NOTES:**

- A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
- △ B. DOES NOT COMPLY JEDEC STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
- G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
- H. DRAWING FILE NAME: TO262A03REV5

**Figure 16. TO262 (I²PAK), Molded, 3-Lead, Jedec Variation AA**

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