TPS25985x 4.5 V – 16 V, 0.59-mΩ, 80-A Stackable eFuse with Accurate and Fast Current Monitor

1 Features

- Input operating voltage range: 4.5 V to 16 V
  - 20-V absolute maximum
  - Withstands negative voltages up to –1 V at output
- Integrated FET with low on-resistance: 0.59 mΩ (typ.)
- Rated for 60-A RMS current and 80-A peak current
- Supports parallel connection of multiple eFuses for higher current support
  - Active device state synchronization and load sharing during start-up and steady-state for unlimited scalability
- Robust overcurrent protection
  - Adjustable overcurrent threshold (I_{OCP}): 10 A to 60 A with accuracy of ±6% (max.)
  - Circuit-breaker response during steady state operation with adjustable transient blanking timer (ITIMER) to support peak currents up to 2 × I_{OCP}
  - Adjustable active current limit during start-up (I_{LIM})
- Robust short-circuit protection
  - Fast-trip response (< 200 ns) to output short-circuit events
  - Adjustable (2 × I_{OCP})and fixed thresholds
  - Immune to supply line transients — no nuisance tripping
- Precise analog load current monitoring
  - ±1.4% accuracy
  - > 500-kHz bandwidth
- Fast overvoltage protection (fixed 16.6-V threshold)
- Adjustable output slew rate control (dVdt) for inrush current protection
- Active high enable input with adjustable undervoltage lockout (UVLO)
- Overtemperature Protection (OTP) to ensure FET SOA
  - Assured FET SOA: 12 W$\sqrt{s}$
- Integrated FET health monitoring and reporting
- Analog die temperature monitor output (TEMP)
- Dedicated fault indication pin ($\overline{FLT}$)
- Power Good indication pin (PG)
- Uncommitted general purpose fast comparator
- Small footprint: QFN 4.5-mm × 5-mm, 0.6-mm pitch
  - 29-mil clearance between power and GND pins
- 100% Pb Free

2 Applications

- Input hotswap and hotplug
- Server and high performance computing
- Network interface cards
- Graphics and hardware accelerator cards
- Datacenter switches and routers
- Fan trays

3 Description

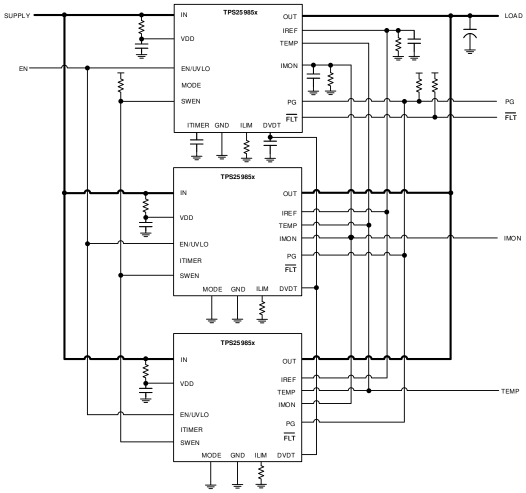
The TPS25985x is an integrated, high-current circuit protection and power management solution in a small package. The device provides multiple protection modes using very few external components and is a robust defense against overloads, short-circuits, and excessive inrush current.

Applications with particular inrush current requirements can set the output slew rate with a single external capacitor. Output current limit level can be set by user as per system needs. A user adjustable overcurrent blanking timer allows systems to support transient peaks in the load current without tripping the eFuse.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS25985xRQP	QFN (26)	4.50 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (May 2022) to Revision A (September 2022)	Page
• Changed status from "Advance Information" to "Production Data"	1

5 Description (continued)

Multiple TPS25985x devices can be connected in parallel to increase the total current capacity for high power systems. All devices actively synchronize their operating state and share current during start-up as well as steady state to avoid over-stressing some of the devices which can result in premature or partial shutdown of the parallel chain.

An integrated fast and accurate sense analog load current monitor facilitates predictive maintenance and advanced dynamic platform power management techniques such as Intel® PSYS and PROCHOT# to maximize system throughput and power supply utilization.

The devices are characterized for operation over a junction temperature range of –40°C to +125°C.

6 Pin Configuration and Functions

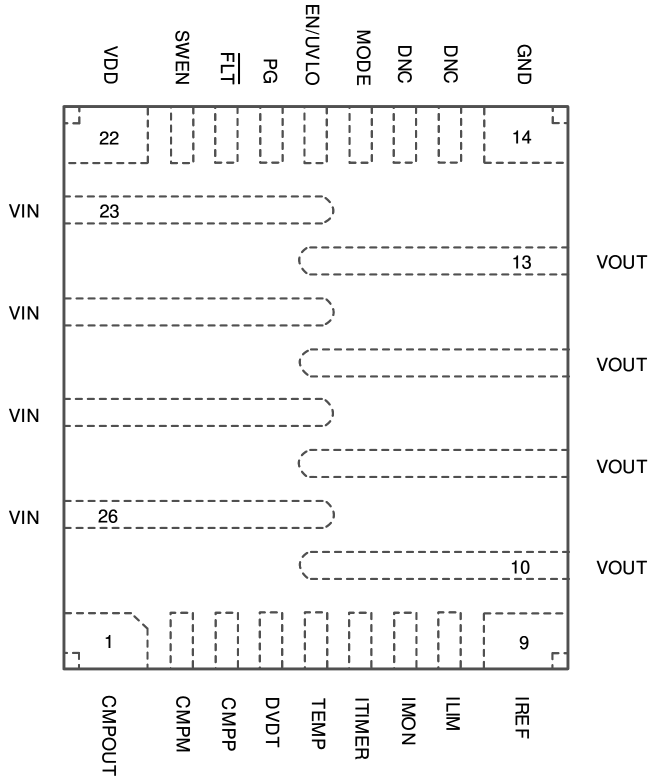


Figure 6-1. TPS25985x RQP Package 26-pin QFN Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
CMPOUT	1	O	General purpose comparator open-drain output
CMPM	2	I	General purpose comparator negative input
CMPP	3	I	General purpose comparator positive input
DVDT	4	I/O	Start-up output slew rate control pin. Leave this pin open to allow fastest start-up. Connect capacitor to ground to slow down the slew rate to manage inrush current.
TEMP	5	O	Die junction temperature monitor analog voltage output. Can be tied together with TEMP outputs of multiple devices in a parallel configuration to indicate the peak temperature of the chain.
ITIMER	6	I/O	A capacitor from this pin to GND sets the overcurrent blanking interval during which the output current can temporarily exceed the overcurrent threshold (but lower than fast-trip threshold) during steady-state operation before the device overcurrent response takes action.
IMON	7	O	An external resistor from this pin to GND sets the overcurrent protection threshold and fast-trip threshold during steady-state. This pin also acts as a fast and accurate analog output load current monitor signal during steady-state. *Do not leave floating.*
ILIM	8	O	An external resistor from this pin to GND sets the current limit threshold and fast-trip threshold during start-up. This also sets the active current sharing threshold during steady-state. *Do not leave floating.*

Table 6-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	**NO.**		
IREF	9	I/O	Reference voltage for overcurrent, short-circuit protection and active current sharing blocks. Can be generated using internal current source and resistor on this pin, or can be driven from external voltage source. *Do not leave floating.*
OUT	10, 11, 12, 13	P	Power output. Must be soldered to output power plane uniformly to ensure proper heat dissipation and to maintain optimal current distribution through the device.
GND	14	G	Device ground reference pin. Connect to system ground.
DNC	15	X	Do not connect anything to this pin.
DNC	16	X	Do not connect anything to this pin.
MODE	17	I	MODE selection pin. Leave the pin floating for standalone and primary mode of operation. Connect the pin to GND to configure device as a secondary device in a parallel chain.
EN/UVLO	18	I	Active high enable input. Connect resistor divider from input supply to set the undervoltage threshold. *Do not leave floating.*
PG	19	I/O	Open-drain active high Power Good indication
$\overline{\text{FLT}}$	20	O	Open-drain active low fault indication
SWEN	21	I/O	Open-drain signal to indicate and control power switch ON/OFF status. This pin facilitates active synchronization between multiple devices in a parallel chain.
VDD	22	P	Controller power input pin. Can be used to power the internal control circuitry with a filtered and stable supply which is not affected by system transients. Connect this pin to VIN through a series resistor and add a decoupling capacitor to GND.
IN	23, 24, 25, 26	P	Power input. Must be soldered to input power plane uniformly to ensure proper heat dissipation and to maintain optimal current distribution through the device.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{INMAX}	Maximum Input Voltage Range	IN	–0.3	20	V
V_{DDMAX}	Maximum Supply Voltage Range	VDD	–0.3	20	V
V_{OUTMAX}	Maximum Output Voltage Range	OUT	–1	Min(20 V, VIN + 0.3)	
$V_{IREFMAX}$	Maximum IREF Pin Voltage Range	IREF		5.5	V
$V_{DVDTMAX}$	Maximum DVDT Pin Voltage Range	DVDT		5.5	V
$V_{MODEMAX}$	Maximum MODE Pin Voltage Range	MODE	Internally Limited		V
$V_{SWENMAX}$	Maximum SWEN Pin Voltage Range	SWEN		5.5	V
$I_{SWENMAX}$	Maximum SWEN Pin Sink Current	SWEN		10	mA
V_{ENMAX}	Maximum Enable Pin Voltage Range	EN/UVLO		20	V
$V_{FLTBMAX}$	Maximum $\overline{\text{FLT}}$ Pin Voltage Range	$\overline{\text{FLT}}$		5.5	V
$I_{FLTBMAX}$	Maximum $\overline{\text{FLT}}$ Pin Sink Current	$\overline{\text{FLT}}$		10	mA
V_{PGMAX}	Maximum PG Pin Voltage Range	PG		5.5	V
I_{PGMAX}	Maximum PG Pin Sink Current	PG		10	mA
$V_{CMPPMAX}$	Maximum CMPP Pin Voltage Range	CMPP		5.5	V
$V_{CMPMMAX}$	Maximum CMPM Pin Voltage Range	CMPM		5.5	V
$V_{CMPOUTMAX}$	Maximum CMPOUT Pin Voltage Range	CMPOUT		5.5	V
$I_{CMPOUTMAX}$	Maximum CMPOUT Pin Sink Current	CMPOUT		10	mA
$V_{TEMPMAX}$	Maximum TEMP Pin Voltage Range	TEMP		5.5	V
$V_{ILIMMAX}$	Maximum ILIM pin voltage	ILIM	Internally Limited		V
$V_{IMONMAX}$	Maximum IMON pin voltage	IMON	Internally Limited		V
$V_{ITIMERMAX}$	Maximum ITIMER pin voltage	ITIMER	Internally Limited		V
I_{MAX}	Maximum Continuous Switch Current	IN to OUT	Internally Limited		A
T_{JMAX}	Junction temperature		Internally Limited		°C
T_{LEAD}	Maximum Soldering Temperature			300	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input Voltage Range	IN	4.5	16	V

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{DD}	Supply Voltage Range	VDD	4.5	16	V
V_{OUT}	Output Voltage Range	OUT		V_{IN}	V
$V_{EN/UVLO}$	Enable Pin Voltage Range	EN/UVLO		Min(V_{DD} + 1 V, V_{IN} + 1 V)	V
V_{DVDT}	DVDT Pin Cap Voltage Rating	DVDT	4		V
V_{PG}	PG Pin Pull-up Voltage Range	PG		5	V
V_{FLTB}	$\overline{\text{FLT}}$ Pin Pull-up Voltage Range	$\overline{\text{FLT}}$		5	V
V_{SWEN}	SWEN Pin Pull-up Voltage Range	SWEN	2.5	5	V
V_{ITIMER}	ITIMER Pin Cap Voltage Rating	ITIMER	4		V
V_{IREF}	IREF Pin Voltage Range	IREF	0.3	1.2	V
V_{ILIM}	ILIM Pin Voltage Range	ILIM		0.4	V
V_{IMON}	IMON Pin Voltage Range	IMON		1.2	V
V_{CMPx}	CMPP, CMPM Common Mode Voltage Range	CMPP, CMPM	0.3	1.5	V
V_{CMPOUT}	CMPOUT Pin Pull-up Voltage Range	CMPOUT		5	V
I_{MAX}	RMS Switch Current, $T_J \leq 125°C$	IN to OUT		60	A
$I_{MAX,\ PLS}$	Peak Output Current, $T_J \leq 125°C$	IN to OUT		80	A
T_J	Junction temperature		–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1) (2)		TPS25985X	UNIT
		RQP (QFN)	
		26 PINS	
$R_{\theta JA(eff)}$	Junction-to-ambient thermal resistance (effective)	19.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	4.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

(2) Based on simulations conducted with the device mounted on a custom 8-layer PCB (4s4p)

7.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, VDD = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, SWEN = 10 kΩ pull-up to 5 V, R_{ILIM} = 550 Ω, R_{IMON} = 1100 Ω, V_{IREF} = 1 V, DVDT = Open, ITIMER = Open, $\overline{\text{FLT}}$ = 10 kΩ pull-up to 5 V, PG = 10 kΩ pull-up to 5 V, TEMP = Open, MODE = Open, CMPM = Open, CMPP = Open, CMPOUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VDD)						
V_{DD}	VDD input operating voltage range		4.5		16	V
$I_{QON(VDD)}$	VDD ON state quiescent current	$V_{VDD} > V_{UVP(R)}$, $V_{EN} \geq V_{UVLO(R)}$		0.45	0.55	mA
$I_{QOFF(VDD)}$	VDD OFF state current	$V_{EN} < V_{UVLO(F)}$		82	240	µA
$V_{UVP(R)}$	VDD undervoltage protection threshold	VDD Rising	4.03	4.21	4.38	V
$V_{UVP(F)}$	VDD undervoltage protection threshold	VDD Falling	3.8	4.05	4.24	V
INPUT SUPPLY (IN)						
V_{IN}	VIN input operating voltage range		4.5		16	V
$V_{UVPIN(R)}$	V_{IN} undervoltage protection threshold	V_{IN} Rising	4	4.23	4.5	V
$V_{UVPIN(F)}$	V_{IN} undervoltage protection threshold	V_{IN} Falling	3.9	4.08	4.4	V
$I_{QON(IN)}$	IN ON state quiescent current	$V_{EN} \geq V_{UVLO(R)}$		2.83	4.7	mA

7.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, VDD = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, SWEN = 10 kΩ pull-up to 5 V, R_{ILIM} = 550 Ω, R_{IMON} = 1100 Ω, V_{IREF} = 1 V, DVDT = Open, ITIMER = Open, $\overline{FLT}$ = 10 kΩ pull-up to 5 V, PG = 10 kΩ pull-up to 5 V, TEMP = Open, MODE = Open, CMPM = Open, CMPP = Open, CMPOUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{QOFF(IN)}$	IN OFF state current	$V_{EN} < V_{UVLO(F)}$		2.9	400	µA
ENABLE / UNDERVOLTAGE LOCKOUT (EN/UVLO)						
$V_{UVLO(R)}$	EN/UVLO pin voltage rising threshold for turning on	EN/UVLO Rising	1.12	1.2	1.28	V
$V_{UVLO(F)}$	EN/UVLO pin voltage falling threshold for turning off and engaging output discharge (primary device)	EN/UVLO Falling, MODE = Open	1.02	1.09	1.18	V
	EN/UVLO pin voltage threshold for turning off and engaging QOD (secondary device)	EN/UVLO Falling, MODE = GND	0.92	0.99	1.08	V
$V_{SD(F)}$	EN/UVLO pin voltage threshold for entering full shutdown	EN/UVLO Falling	0.5	0.8		V
I_{ENLKG}	EN/UVLO pin leakage current	V_{EN} < Min(V_{IN} + 1 V, V_{DD} + 1 V)	–0.1		0.1	µA
OVERVOLTAGE PROTECTION (IN)						
$V_{OVP(R)}$	Input overvoltage protection threshold (rising)	V_{IN} rising	15.7	16.6	17.9	V
$V_{OVP(F)}$	Input overvoltage protection threshold (falling)	V_{IN} falling	15.4	16.44	17.8	V
ON-RESISTANCE (IN - OUT)						
R_{ON}	ON resistance	I_{OUT} = 8 A, T_J = 25℃		0.582	0.737	mΩ
		I_{OUT} = 8 A, T_J = -40 to 125℃			1	mΩ
OVERCURRENT PROTECTION REFERENCE (IREF)						
I_{IREF}	IREF pin internal sourcing current		24.3	24.98	25.7	µA
CURRENT LIMIT (ILIM)						
$G_{ILIM(LIN)}$	ILIM current monitor gain (ILIM:IOUT)		17.62	18.18	18.74	µA/A
$CL_{REF(SAT)\%}$	Ratio of start-up current limit threshold (ILIM) to steady-state overcurrent protection threshold reference (IREF)	$V_{OUT} > V_{FB}$, PG not asserted	17	22	29	%
I_{LIM}	Start-up current limit regulation threshold	R_{ILIM} = 138 Ω, V_{IREF} = 1.2 V, $V_{OUT} > V_{FB}$	28.4	39.51	52.8	A
		R_{ILIM} = 160 Ω, V_{IREF} = 1..2 V, $V_{OUT} > V_{FB}$	26.5	34.66	45	A
		R_{ILIM} = 400 Ω, V_{IREF} = 1.2 V, $V_{OUT} > V_{FB}$	8	13.65	18.2	A
		R_{ILIM} = 800 Ω, V_{IREF} = 1.2 V, $V_{OUT} > V_{FB}$	5.7	9.73	13	A
V_{FB}	Foldback voltage		1.5	1.99	2.5	V
OUTPUT CURRENT MONITOR AND OVERCURRENT PROTECTION (IMON)						
G_{IMON}	IMON current monitor gain (IMON:IOUT)	Device in steady state (PG asserted)	17.808	18.19	18.57	µA/A
I_{OCP}	Steady-state overcurrent protection (Circuit-Breaker) threshold	R_{IMON} = 1100 Ω, V_{IREF} = 1.2 V	58.04	60.11	61.96	A
		R_{IMON} = 1100 Ω, V_{IREF} = 1V	48.3	50.1	51.7	A
		R_{IMON} = 1100 Ω, V_{IREF} = 0.5 V	24.1	25.09	25.9	A
		R_{IMON} = 1100 Ω, V_{IREF} = 0.24 V	11.35	12.05	12.65	A
TRANSIENT OVERCURRENT BLANKING TIMER (ITIMER)						
I_{ITIMER}	ITIMER pin internal discharge current	$I_{OUT} > I_{OCP}$, ITIMER ↓	1.29	2.07	2.98	µA
R_{ITIMER}	ITIMER pin internal pull-up resistance		10	13.87	19	kΩ
V_{INT}	ITIMER pin internal pull-up voltage	$I_{OUT} < I_{OCP}$	3	3.65	4.1	V
$V_{ITIMERTHR}$	ITIMER comparator falling threshold	$I_{OUT} > I_{OCP}$, ITIMER ↓		2.16		V

7.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, VDD = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, SWEN = 10 kΩ pull-up to 5 V, R_{ILIM} = 550 Ω, R_{IMON} = 1100 Ω, V_{IREF} = 1 V, DVDT = Open, ITIMER = Open, $\overline{FLT}$ = 10 kΩ pull-up to 5 V, PG = 10 kΩ pull-up to 5 V, TEMP = Open, MODE = Open, CMPM = Open, CMPP = Open, CMPOUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔV_{ITIMER}	ITIMER discharge voltage threshold	$I_{OUT} > I_{OCP}$, ITIMER ↓	1.24	1.50	1.76	V
SHORT-CIRCUIT PROTECTION						
I_{FFT}	Fixed fast-trip threshold in steady-state	PG asserted High, Standalone/Primary mode, MODE = Open	99	148	210	A
		PG asserted High, Secondary mode, MODE = GND	130	222	290	A
$SFT_{REF(LIN)\%}$	Scalable fast-trip threshold (IMON) to overcurrent protection threshold reference (IREF) ratio during steady-state	Standalone/Primary mode, MODE = Open	186	200	214	%
		Secondary mode, MODE = GND	210	225	240	%
$SFT_{REF(SAT)\%}$	Scalable fast trip threshold to start-up current limit threshold ratio (ILIM) (Inrush)	Standalone/Primary mode, MODE = Open	34	50	66	%
		Secondary mode, MODE = GND	34	50	66	%
$R_{ON(ACS)}$	Maximum R_{ON} during steady-state active current sharing	$V_{ILIM} > CL_{REF(ACS)\%} \times V_{IREF}$		0.778	1.31	mΩ
$G_{IMON(ACS)}$	IMON:IOUT ratio during active current sharing	PG asserted High, $V_{ILIM} > CL_{REF(ACS)\%} \times V_{IREF}$	18.02	18.39	18.87	µA/A
$CL_{REF(ACS)\%}$	Ratio of active current sharing trigger threshold to steady state overcurrent protection threshold	PG asserted High	34.67	36.67	38.67	%
INRUSH CURRENT PROTECTION (DVDT)						
I_{DVDT}	DVDT pin charging current	Primary/Standalone mode, MODE = Open	1.4	2.03	2.9	µA
G_{DVDT}	DVDT gain		18	20.5	22	V/V
R_{DVDT}	dVdt pin to GND discharge resistance		350	529.6	670	Ω
$R_{ON(GHI)}$	R_{ON} when PG is asserted			0.749	1.31	mΩ
COMPARATOR INPUTS (CMPP, CMPM)						
$V_{CM(CMP)}$	CMPx common mode voltage range		0.3		1.5	
I_{CMPx}	CMPx pin leakage current	0.3 V < V_{CMPx} < 1.5 V	–0.1		0.1	µA
QUICK OUTPUT DISCHARGE (QOD)						
I_{QOD}	Quick output discharge internal pull-down current	$V_{SD(F)} < V_{EN} < V_{UVLO(F)}$, $-40 < T_J <$ 125°C	11.6	20.65	26.5	mA
TEMPERATURE SENSOR OUTPUT (TEMP)						
G_{TMP}	TEMP sensor gain		2.58	2.65	2.72	mV/°C
V_{TMP}	TEMP pin output voltage	T_J = 25°C	672	678.5	685	mV
I_{TMPSRC}	TEMP pin sourcing current		75	93.4	170	µA
I_{TMPSNK}	TEMP pin sinking current		8	10.1	14	µA
OVERTEMPERATURE PROTECTION (OTP)						
TSD	Thermal shutdown threshold	T_J Rising		150		°C
TSD_{HYS}	Thermal shutdown hysteresis	T_J Falling		12.5		°C
FET HEALTH MONITOR						
V_{DSFLT}	FET D-S fault threshold	SWEN = L	0.38	0.49	0.59	V
SINGLE POINT FAILURE (ILIM, IMON, IREF, ITIMER)						
$I_{OC\_BKP(LIN)}$	Back-up overcurrent protection threshold (steady -state)		70	94.2	140	A

7.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, VDD = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, SWEN = 10 kΩ pull-up to 5 V, R_{ILIM} = 550 Ω, R_{IMON} = 1100 Ω, V_{IREF} = 1 V, DVDT = Open, ITIMER = Open, $\overline{FLT}$ = 10 kΩ pull-up to 5 V, PG = 10 kΩ pull-up to 5 V, TEMP = Open, MODE = Open, CMPM = Open, CMPP = Open, CMPOUT = Open. All voltages referenced to GND.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OC\_BKP(SAT)}$	Back-up overcurrent protection threshold (start-up)		50	102.2	160	A

7.6 Logic Interface

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWEN						
R_{SWEN}	SWEN pin pull-down resistance	SWEN de-asserted Low	4.4	8.1	13	Ω
$I_{SWENLKG}$	SWEN pin leakage current	SWEN asserted High	–2		2	µA
$V_{IH\_SWEN(min)}$	SWEN input logic high				1.44	V
$V_{IL\_SWEN(max)}$	SWEN input logic low		0.4			V
FAULT INDICATION (FLTB)						
R_{FLTB}	$\overline{FLT}$ pin pull-down resistance	$\overline{FLT}$ asserted Low	4.4	8.09	13	Ω
$I_{FLTBLKG}$	$\overline{FLT}$ pin leakage current	$\overline{FLT}$ de-asserted High	–2		2	µA
POWER GOOD INDICATION (PG)						
R_{PG}	PG pin pull-down resistance	PG de-asserted Low	4.3	7.14	13	Ω
I_{PGKG}	PG pin leakage current	PG asserted High	–2		2	µA
COMPARATOR OUTPUT (CMPOUT)						
R_{CMPOUT}	CMPOUT pin pull-down resistance	CMPOUT de-asserted Low	5	8.1	40	Ω
I_{CMPOUT}	CMPOUT pin leakage current	CMPOUT asserted High	–2		2	µA

7.7 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVP}	Overvoltage protection response time	$V_{IN} > V_{OVP(R)}$ to SWEN↓		1.57		µs
t_{INSDLY}	Insertion delay	$V_{DD} > V_{UVP(R)}$ to SWEN↑		13.7		ms
t_{FFT}	Fixed Fast-Trip response time	$I_{OUT} > 1.5 \times I_{FFT}$ to I_{OUT}↓		192		ns
t_{SFT}	Scalable Fast-Trip response time	$I_{OUT} > 3 \times I_{OCP}$ to I_{OUT}↓		364		ns
t_{CMP}	General purpose comparator response time	$V_{CMPP} > 1.3 \times V_{CMPM}$ to CMPOUT↑		366		ns
t_{ITIMER}	Overcurrent blanking interval	$I_{OUT} = 1.5 \times I_{OCP}$, C_{ITIMER} = Open		0		ms
		$I_{OUT} = 1.5 \times I_{OCP}$, C_{ITIMER} = 4.7 nF		3.79		ms
t_{RST}	Auto-Retry Interval	Auto-retry variant, Primary mode (MODE = Open)		107.5		ms
$t_{EN(DG)}$	EN/UVLO de-glitch time			6		µs
t_{SU_TMR}	Start-up timeout interval	SWEN↑ to FLT↓		215		ms
$t_{Discharge}$	QOD discharge time (90% to 10% of V_{OUT})	$V_{SD(F)} < V_{EN/UVLO} < V_{UVLO(F)}$, V_{IN} = 12 V, C_{OUT} = 1 mF		588		ms
t_{QOD}	QOD enable timer	$V_{SD(F)} < V_{EN/UVLO} < V_{UVLO(F)}$		4.66		ms
t_{PGA}	PG assertion delay			20		us

7.8 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled. Typical values are taken at T_J = 25°C unless specifically noted otherwise. V_{IN} = 12 V, R_{OUT} = 500 Ω, C_{OUT} = 1 mF

PARAMETER		C_{dVdt} = 3.3 nF	C_{dVdt} = 33 nF	UNITS
SR_{ON}	Output rising slew rate	9.79	1.20	V/ms
$t_{D,ON}$	Turn on delay	0.34	1.54	ms
t_R	Rise time	1.00	8.13	ms
t_{ON}	Turn on time	1.38	10.35	ms
$t_{D,OFF}$	Turn off delay	1081	1060	µs
t_F	Fall time	Depends on R_{OUT} and C_{OUT}		µs

7.9 Typical Characteristics

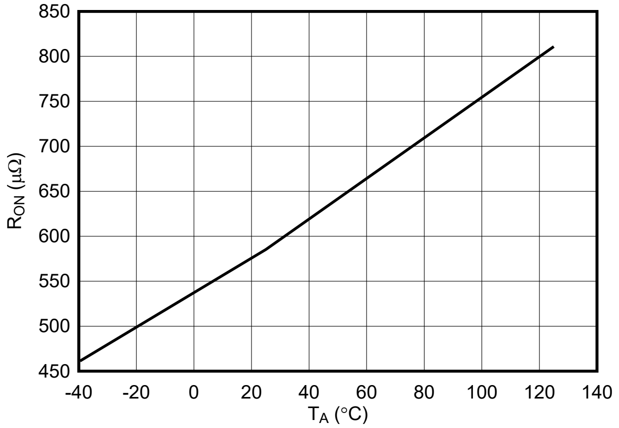


Figure 7-1. ON Resistance Across Temperature

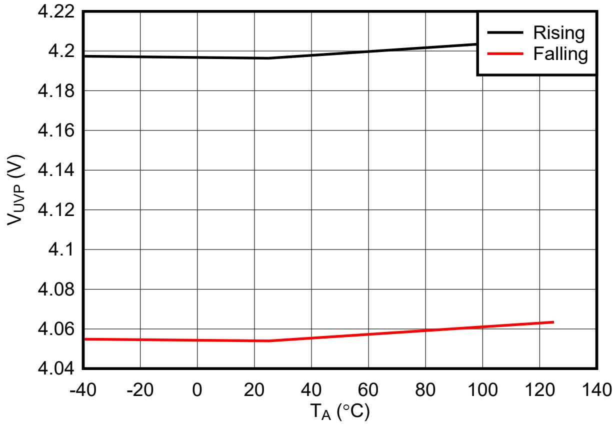


Figure 7-2. VDD Undervoltage Thresholds Across Temperature

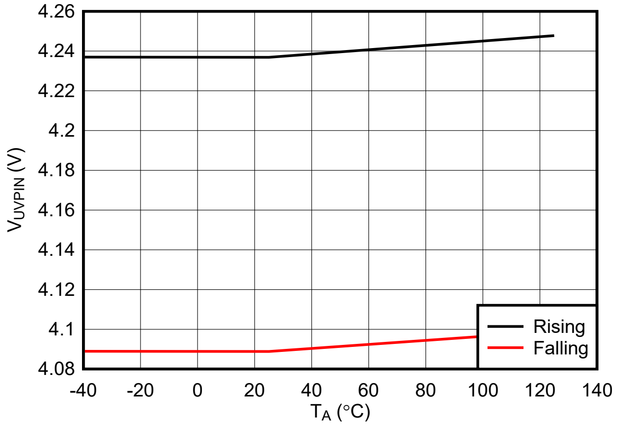


Figure 7-3. VIN Undervoltage Thresholds Across Temperature

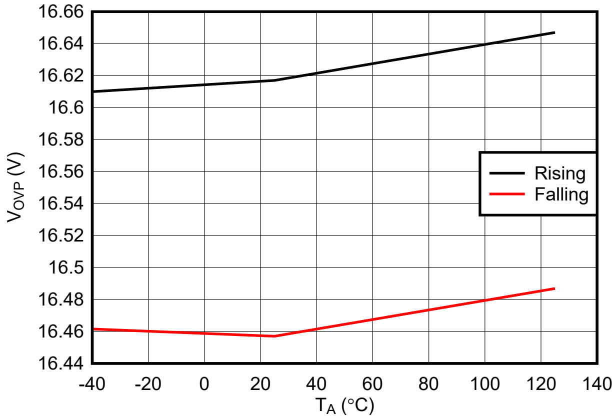


Figure 7-4. Overvoltage Protection Threshold Across Temperature

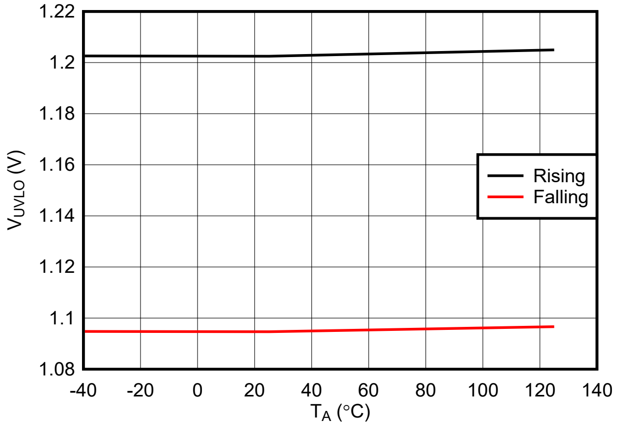


Figure 7-5. EN/UVLO Thresholds Across Temperature

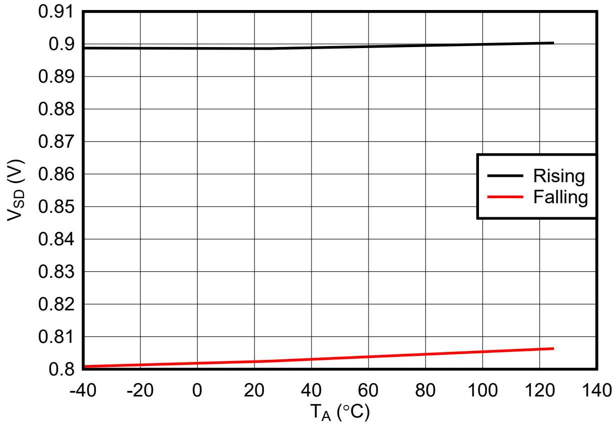


Figure 7-6. EN/UVLO Based Shutdown Falling Threshold Across Temperature

7.9 Typical Characteristics (continued)

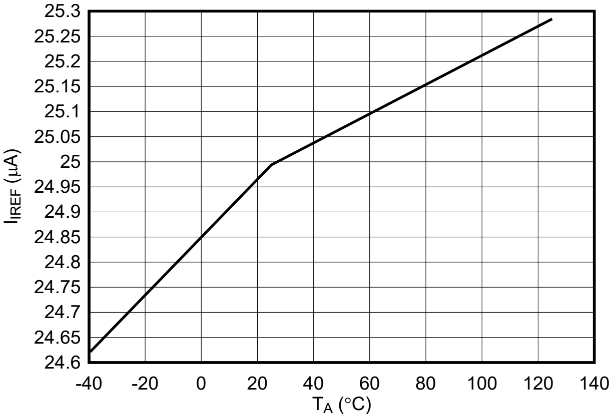


Figure 7-7. IREF Charging Current Across Temperature

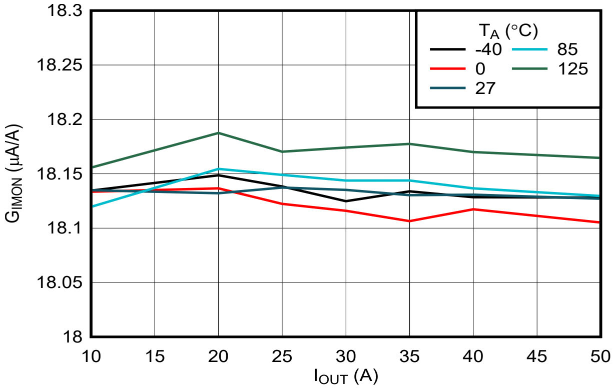


Figure 7-8. IMON Gain Across Load and Temperature

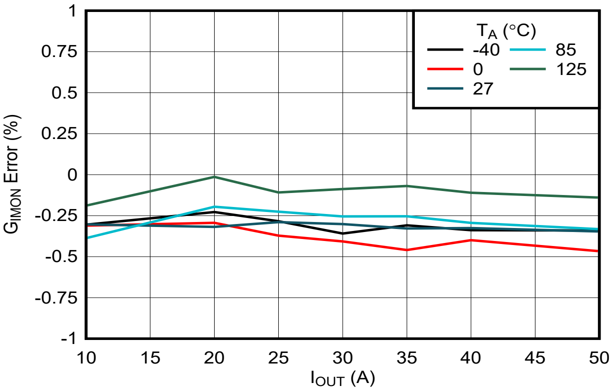


Figure 7-9. IMON Gain Accuracy Across Load and Temperature

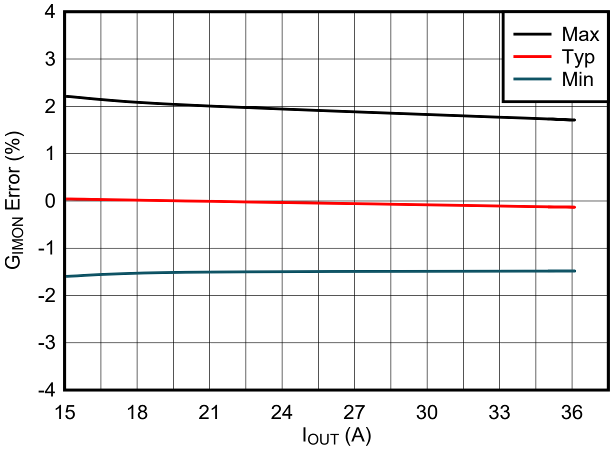


Figure 7-10. IMON Gain Accuracy Across Process and Temperature Corners

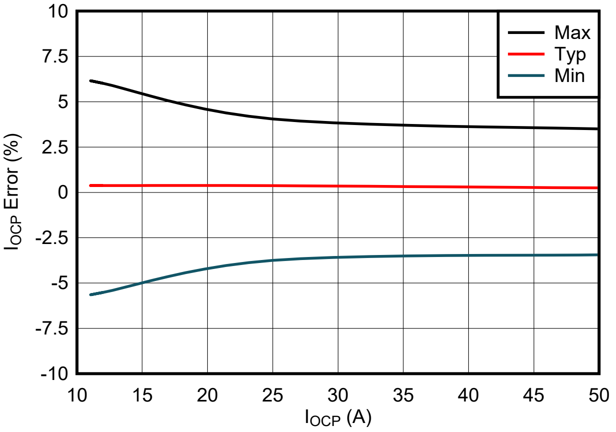


Figure 7-11. Steady-State Overcurrent Protection Threshold (Circuit-Breaker) Accuracy

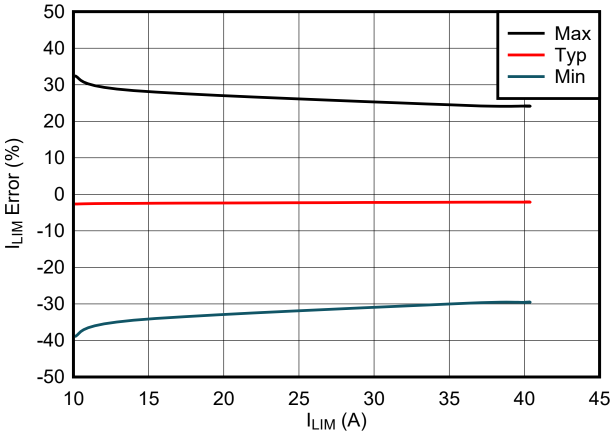


Figure 7-12. Start-up Overcurrent Protection Threshold (Current Limit) Accuracy

7.9 Typical Characteristics (continued)

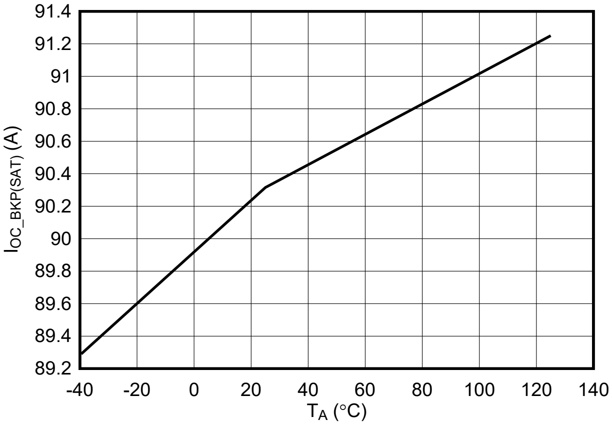


Figure 7-13. Backup Overcurrent Protection Threshold (Start-up) Accuracy

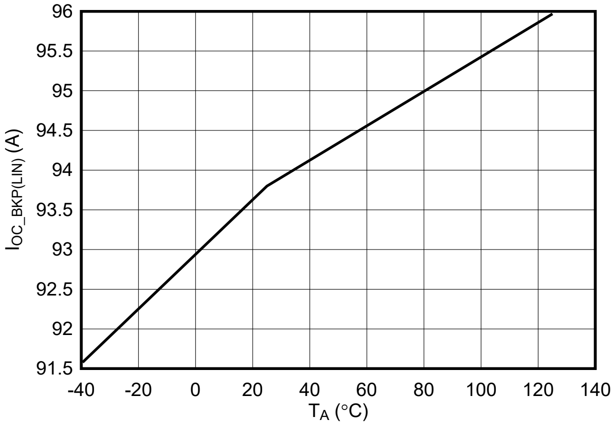


Figure 7-14. Backup Overcurrent Protection Threshold (Steady-State) Accuracy

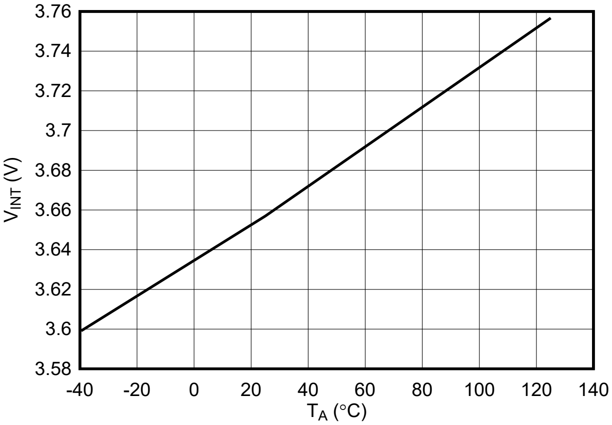


Figure 7-15. ITIMER Pin Internal Pullup Voltage Across Temperature

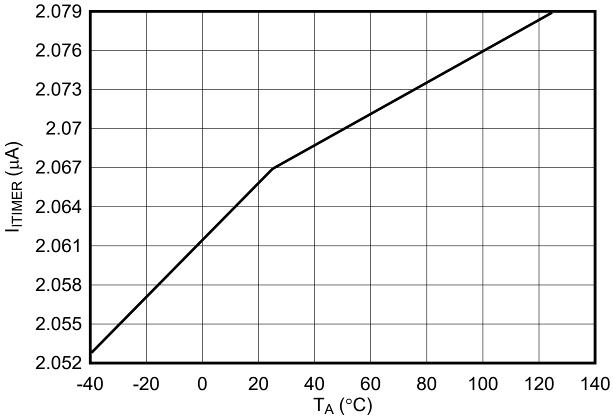


Figure 7-16. ITIMER Pin Discharge Current Across Temperature

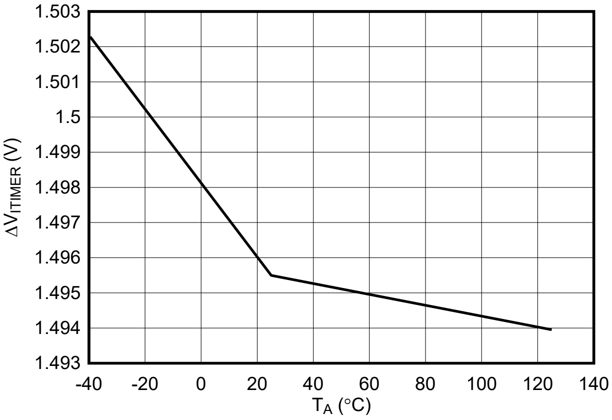


Figure 7-17. ITIMER Pin Discharge Differential Voltage Threshold Across Temperature

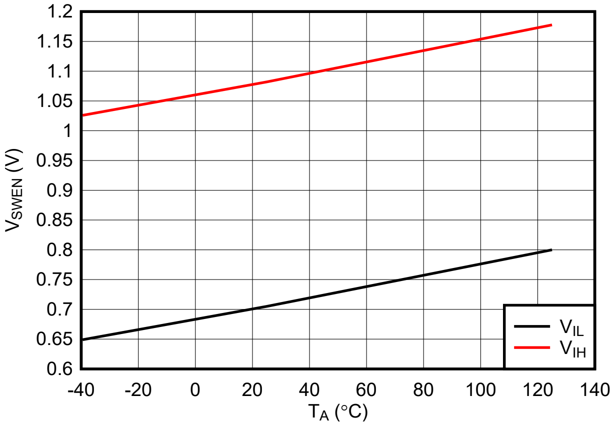


Figure 7-18. SWEN Pin Logic Thresholds Across Temperature

7.9 Typical Characteristics (continued)

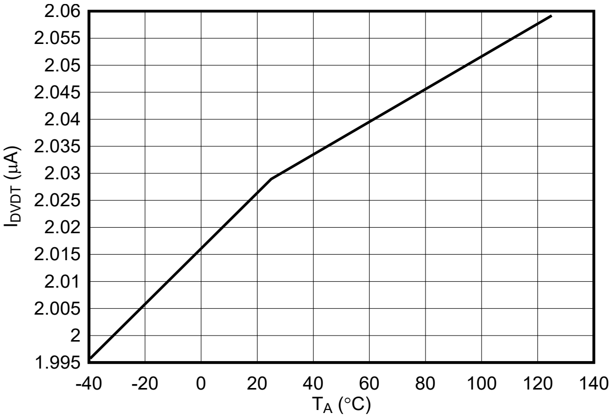


Figure 7-19. DVDT Charging Current Across Temperature

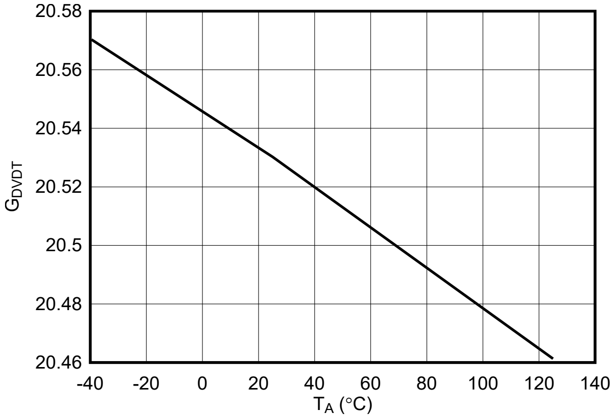


Figure 7-20. DVDT Gain Across Temperature

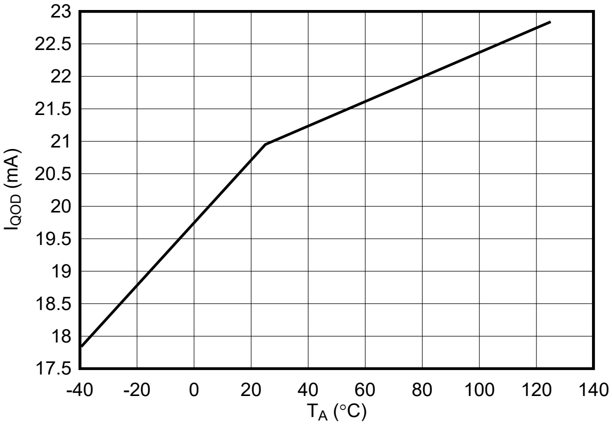


Figure 7-21. QOD Sink Current Across Temperature

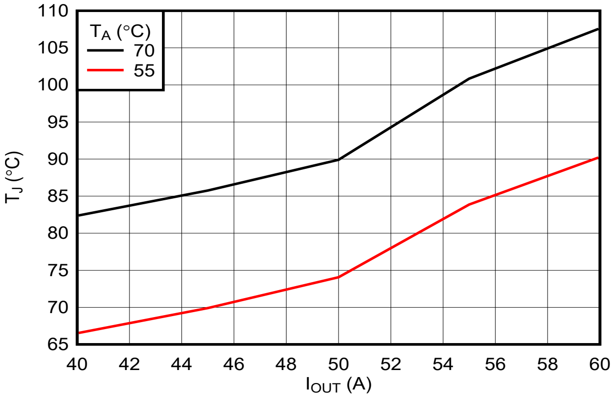


Figure 7-22. Junction Temperature vs Load Current (No Air-Flow)

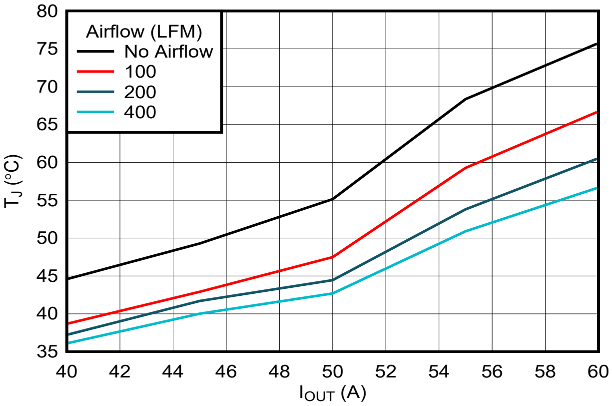
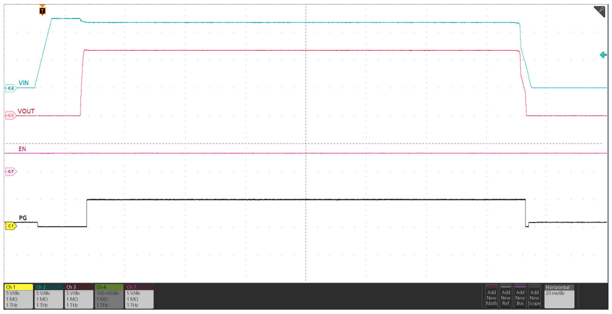


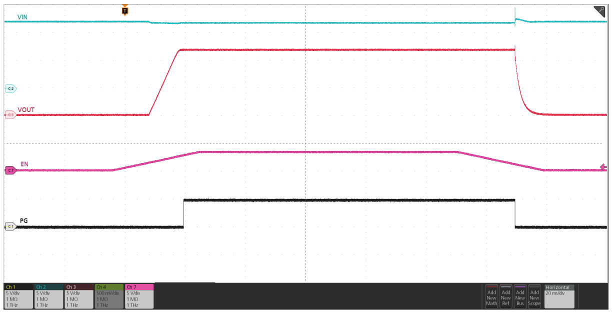
Figure 7-23. Junction Temperature vs Load Current (T_A = 25°C, With Air-Flow)



EN held high, input supply ramped up and down

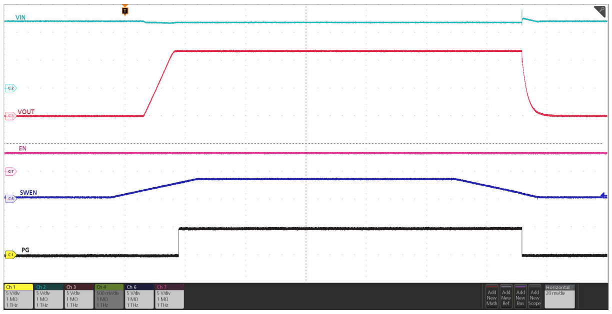
Figure 7-24. Power Up and Down Sequencing Using Input Supply

7.9 Typical Characteristics (continued)



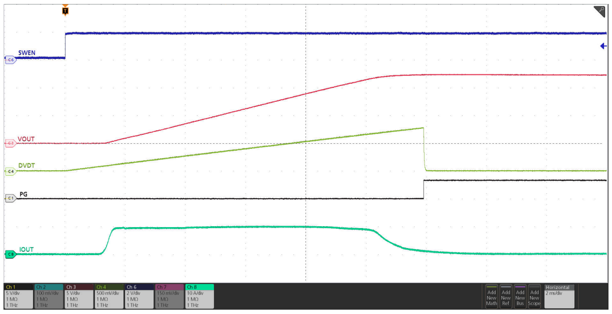
Input supply held steady, EN/UVLO pin toggled high and low

Figure 7-25. Power Up and Down Sequencing Using EN/UVLO Pin



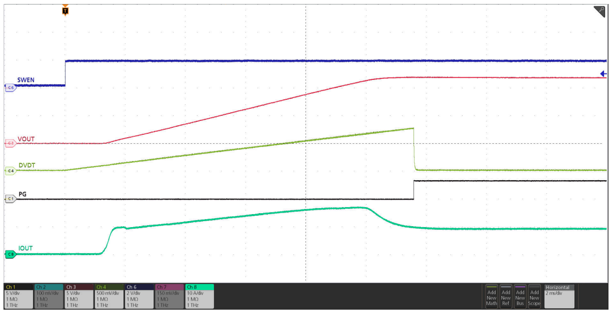
Input supply held steady, EN/UVLO pin held high, SWEN pin toggled high and low

Figure 7-26. Power Up and Down Sequencing Using SWEN Pin



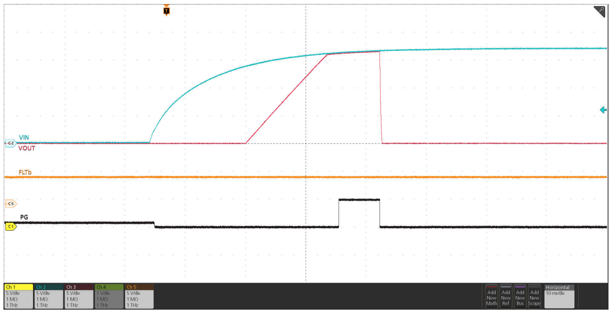
C_{OUT} = 6.8 mF, C_{dVdt} = 33 nF

Figure 7-27. Inrush Current Control with Capacitive Load



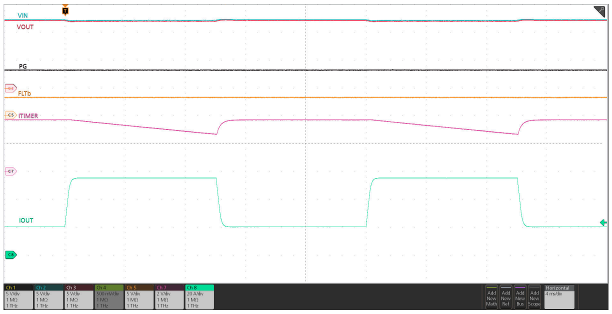
C_{OUT} = 6.8 mF, R_{OUT} = 1.2 Ω, C_{dVdt} = 33 nF

Figure 7-28. Inrush Current Control with Capacitive and Resistive Load



Input supply ramped up above 16.6 V

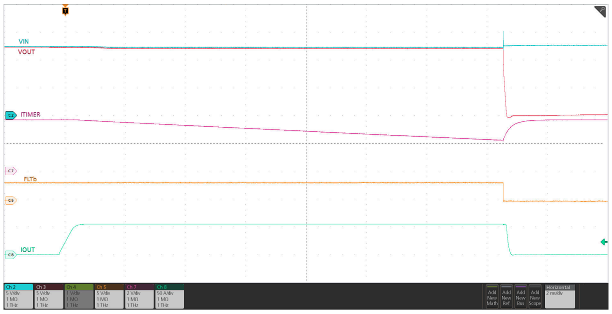
Figure 7-29. Input Overvoltage Protection Response



I_{OCP} = 50 A, t_{ITIMER} = 14 ms, I_{OUT} pulsed above the I_{OCP} threshold for short duration without triggering circuit-breaker response

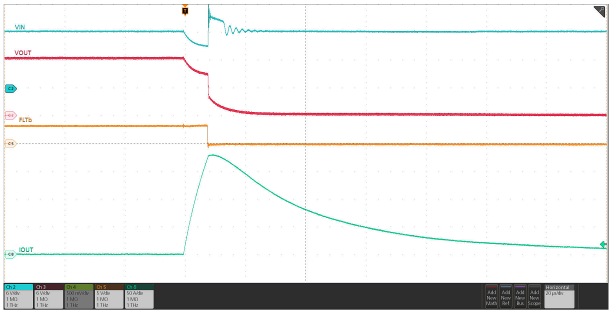
Figure 7-30. Peak Current Support Using Transient Overcurrent Blanking

7.9 Typical Characteristics (continued)



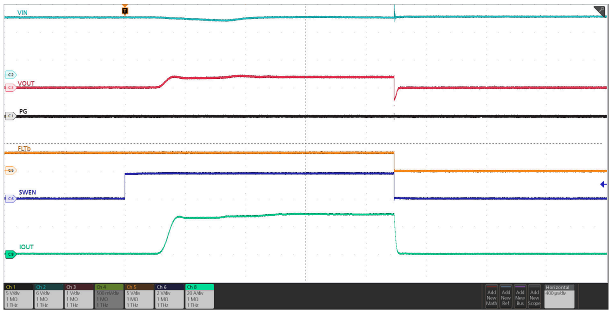
I_{OCP} = 50 A, t_{ITIMER} = 14 ms, I_{OUT} stays above the I_{OCP} threshold persistently to trigger circuit-breaker response

Figure 7-31. Overcurrent Protection Response (Circuit-Breaker)



I_{OCP} = 50 A, Output hard-short to GND while in steady. I_{OUT} rises above 2 × I_{OCP} triggers fast-trip response

Figure 7-32. Short-Circuit Protection Response



Device turned on using SWEN with output hard-short to GND. Device limits the current with foldback.

Figure 7-33. Power Up into Short-Circuit

8 Detailed Description

8.1 Overview

The TPS25985x is an eFuse with integrated power switch that is used to manage load voltage and load current. The device starts its operation by monitoring the VDD and IN bus. When V_{DD} and V_{IN} exceed the respective Undervoltage Protection (UVP) thresholds, the device waits for the insertion delay timer duration to allow the supply to stabilize before starting up. Next the device samples the EN/UVLO pin and SWEN pins. A high level on both these pins enables the internal MOSFET to start conducting and allow current to flow from IN to OUT. When either EN/UVLO or SWEN is held low, the internal MOSFET is turned off.

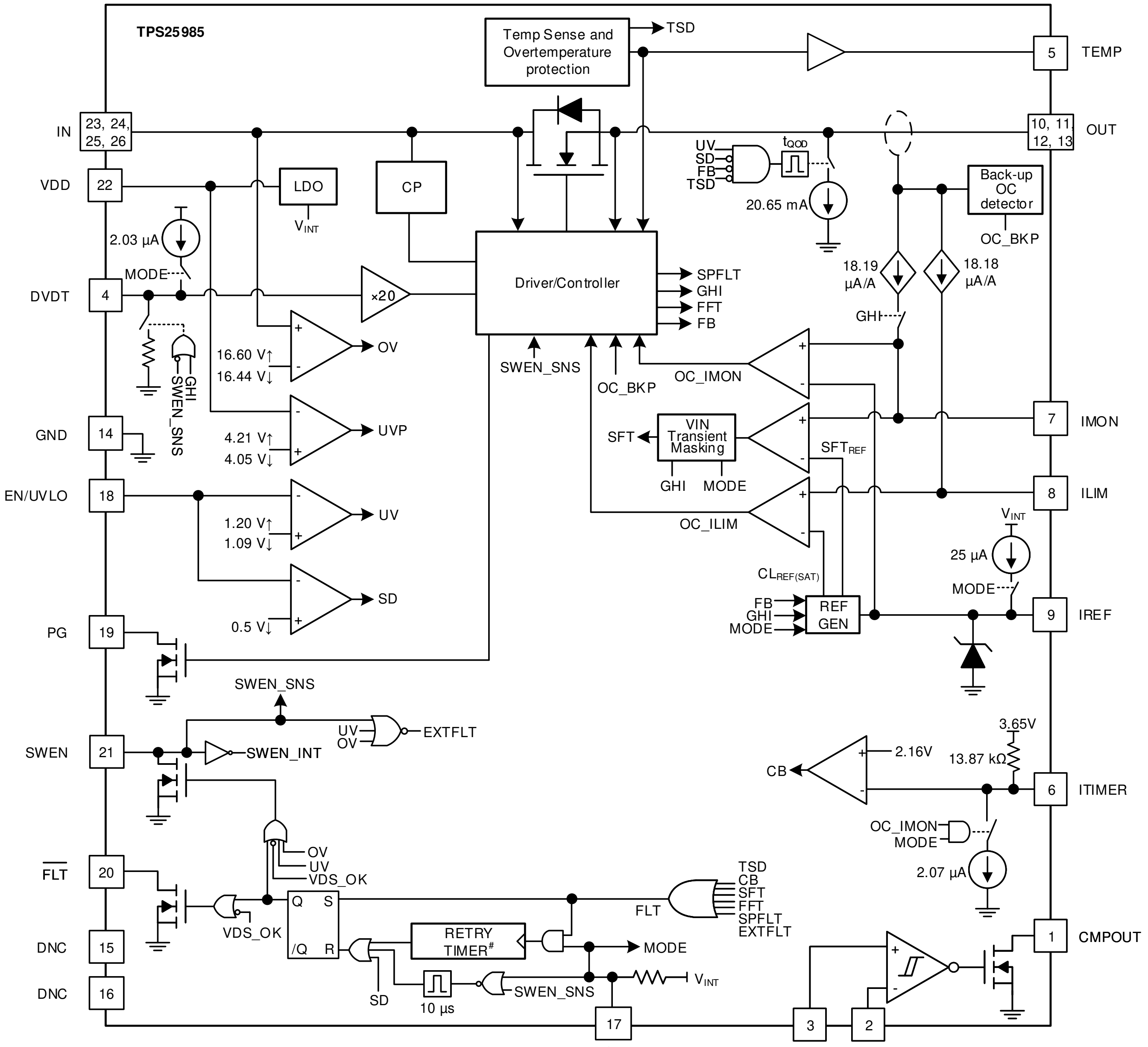
After a successful start-up sequence, the TPS25985x device now actively monitors its load current and input voltage, and controls the internal FET to ensure that the programmed overcurrent threshold is not exceeded and input overvoltage spikes are cut off. This action keeps the system safe from harmful levels of voltage and current. At the same time, a user-adjustable overcurrent blanking timer allows the system to pass transient peaks in the load current profile without tripping the eFuse. Similarly, voltage transients on the supply line are intelligently masked to prevent nuisance trips. This feature ensures a robust protection solution against real faults which is also immune to transients, thereby ensuring maximum system uptime.

The device has integrated high accuracy and high bandwidth analog load current monitor, which allows the system to precisely monitor the load current in steady state as well as during transients. This feature facilitates the implementation of advanced dynamic platform power management techniques such as Intel PSYS or PROCHOT# to maximize system power usage and throughput without sacrificing safety and reliability.

For systems needing higher load current support, multiple TPS25985x eFuses can be connected in parallel. All devices share current during start-up as well as steady-state to avoid over-stressing some of the devices more than others which can result in premature or partial shutdown of the parallel chain. The devices synchronize their operating states to ensure graceful startup, shutdown and response to faults. This makes the whole chain function as a single very high current eFuse rather than a bunch of independent eFuses operating asynchronously.

The device has integrated protection circuits to ensure device safety and reliability under recommended operating conditions. The internal FET SOA is protected at all times using the thermal shutdown mechanism, which turns off the FET whenever the junction temperature (T_J) becomes too high for the FET to operate safely.

8.2 Functional Block Diagram



\# Only for TPS259851 (auto-retry variant)

8.3 Feature Description

The TPS25985x eFuse is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults.

8.3.1 Undervoltage Protection

The TPS25985x implements undervoltage lockout on VDD and VIN in case the applied voltage becomes too low for the system or device to properly operate. The undervoltage lockout has a default internal threshold of V_{UVP} on VDD and V_{UVPIN} on VIN. Alternatively, the UVLO comparator on the EN/UVLO pin allows the undervoltage protection threshold to be externally adjusted to a user defined value. Figure 8-1 and Equation 1 show how a resistor divider can be used to set the UVLO set point for a given voltage supply.

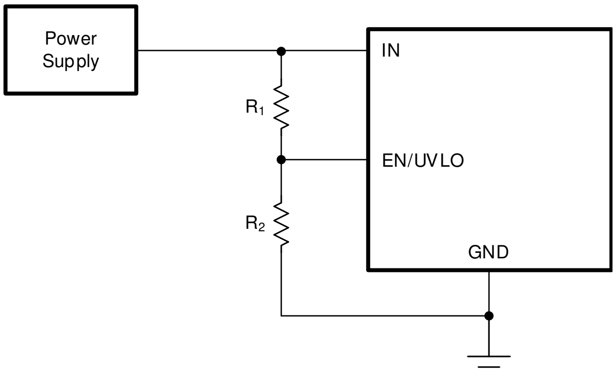


Figure 8-1. Adjustable Undervoltage Protection

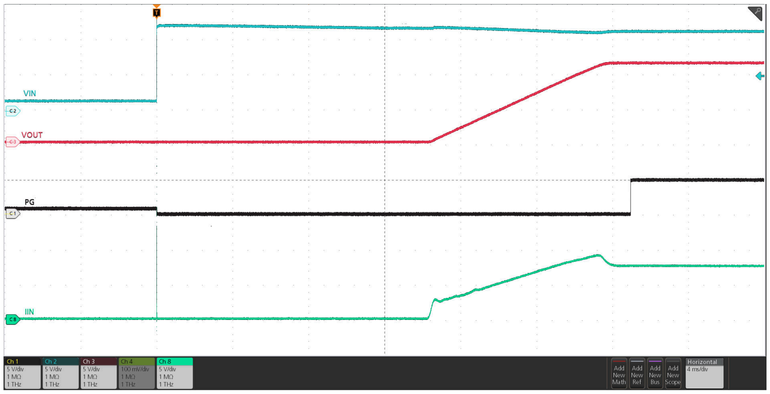
$$V_{IN(UV)} = V_{UVLO(R)} \frac{R_1 + R_2}{R_2} \quad (1)$$

The EN/UVLO pin implements a bi-level threshold.

1. $V_{EN} > V_{UVLO(R)}$: Device is fully ON.
2. $V_{SD(F)} < V_{EN} < V_{UVLO(F)}$: The FET along with most of the controller circuitry is turned OFF, except for some critical bias and digital circuitry. Holding the EN/UVLO pin in this state for > t_{QOD} activates the Output Discharge function.
3. $V_{EN} < V_{SD(F)}$: All active circuitry inside the part is turned OFF and it retains no digital state memory. It also resets any latched faults. In this condition, the device quiescent current consumption is minimal.

8.3.2 Insertion Delay

The TPS25985x implements insertion delay at start-up to ensure the supply has stabilized before the device tries to turn on the power to the load. The device initially waits for the VDD supply to rise above the UVP threshold and all the internal bias voltages to settle. After that, the device remains off for an additional delay of t_{INSDLY} irrespective of the EN/UVLO pin condition. This action helps to prevent any unexpected behavior in the system if the device tries to turn on before the card has made firm contact with the backplane or if there is any supply ringing or noise during start-up.



Input supply stepped up from 0 V to 12 V. Device waits for t_{INSDLY} for input supply to stabilize before it turns on the output.

Figure 8-2. Insertion Delay

8.3.3 Overvoltage Protection

The TPS25985x implements overvoltage lockout to protect the load from input overvoltage conditions. The OVP comparator on the IN pin uses a fixed internal overvoltage protection threshold. If the input voltage on IN exceeds the OVP rising threshold ($V_{OVP(R)}$), the power FET is turned OFF within t_{OVP}. After the voltage on IN falls below the OVP falling threshold ($V_{OVP(F)}$), the FET is turned ON in a dVdt controlled manner.

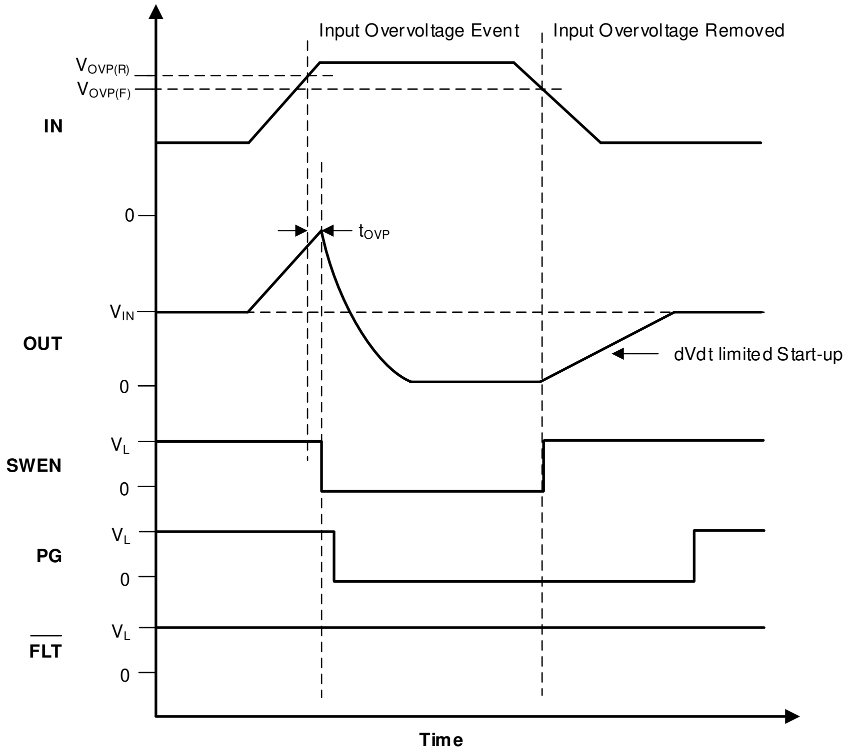


Figure 8-3. Input Overvoltage Protection Response

8.3.4 Inrush Current, Overcurrent, and Short-Circuit Protection

TPS25985x incorporates four levels of protection against overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control
2. Active current limit with an adjustable threshold (I_{LIM}) for overcurrent protection during start-up

3. Circuit-breaker with an adjustable threshold (I_{OCP}) and blanking timer (t_{ITIMER}) for overcurrent protection during steady-state
4. Fast-trip response to severe overcurrent faults with an adjustable threshold ($I_{SFT} = 2 \times I_{OCP}$) to quickly protect against severe short-circuits under all conditions, as well as a fixed threshold (I_{FFT}) during steady state

8.3.4.1 Slew rate (dVdt) and Inrush Current Control

During hot plug events or while trying to charge a large output capacitance, there can be a large inrush current. If the inrush current is not managed properly, the inrush current can damage the input connectors and cause the system power supply to droop. This action can lead to unexpected restarts elsewhere in the system. The inrush current during turn-on is directly proportional to the load capacitance and rising slew rate. Equation 2 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{LOAD}):

$$SR(V/ms) = \frac{I_{INRUSH}(A)}{C_{LOAD}(mF)} \tag{2}$$

A capacitor can be added to the DVDT pin to control the rising slew rate and lower the inrush current during turn-on. The required CdVdt capacitance to produce a given slew rate can be calculated using Equation 3.

$$C_{DVDT}(pF) = \frac{42000}{SR(V/ms)} \tag{3}$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

Note

1. High input slew rates in combination with high input power path inductance can result in oscillations during start-up. This can be mitigated using one or more of the following steps:
    a. Reduce the input inductance.
    b. Increase the capacitance on VIN pin.
    c. Increase the dVdt pin capacitance to reduce the slew rate or increase the start-up time. TI recommends using a minimum start-up time of 5 ms.

8.3.4.1.1 Start-Up Time Out

If the start-up is not completed, that is, the FET is not fully turned on within a certain timeout interval (t_{SU_TMR}) after SWEN is asserted, the device registers it as a fault. $\overline{\text{FLT}}$ is asserted low and the device goes into latch-off or auto-retry mode depending on the device configuration.

8.3.4.2 Steady-State Overcurrent Protection (Circuit-Breaker)

The TPS25985x responds to output overcurrent conditions during steady-state by performing a circuit-breaker action after a user-adjustable transient fault blanking interval. This action allows the device to support a higher peak current for a short user-defined interval but also ensures robust protection in case of persistent output faults.

The device constantly senses the output load current and provides an analog current output (I_{IMON}) on the IMON pin which is proportional to the load current, which in turn produces a proportional voltage (V_{IMON}) across the IMON pin resistor (R_{IMON}) as per Equation 4.

$$V_{IMON} = I_{OUT} \times G_{IMON} \times R_{IMON} \tag{4}$$

Where G_{IMON} is the current monitor gain ($I_{IMON} : I_{OUT}$)

The overcurrent condition is detected by comparing this voltage against the voltage on the IREF pin as a reference. The reference voltage (V_{IREF}) can be controlled in two ways, which sets the overcurrent protection threshold (I_{OCP}) accordingly.

- In the standalone or primary mode of operation, the internal current source interacts with the external IREF pin resistor (R_{IREF}) to generate the reference voltage. It is also possible to drive the IREF pin from an external low impedance reference voltage source as shown in Equation 5.

$$V_{IREF} = I_{IREF} \times R_{IREF} \tag{5}$$

- In a primary and secondary parallel configuration, the primary eFuse or controller drives the voltage on the IREF pin to provide an external reference (V_{IREF}) for all the secondary devices in the chain.

The overcurrent protection threshold during steady-state (I_{OCP}) can be calculated using Equation 6.

$$I_{OCP} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}} \tag{6}$$

Note

Maintain V_{IREF} within the recommended voltage range to ensure proper operation of the overcurrent detection circuit.

TI recommends to add a 150-pF capacitor from IREF pin to GND for improved noise immunity.

After an overcurrent condition is detected, that is the load current exceeds the programmed current limit threshold (I_{OCP}), but stays lower than the short-circuit threshold (2 × I_{OCP}), the device starts discharging the ITIMER pin capacitor using an internal 2.07-µA pulldown current. If the load current drops below the current limit threshold before the ITIMER capacitor discharges by ΔV_{ITIMER}, the ITIMER is reset by pulling it up to V_{INT} internally and the circuit-breaker action is not engaged. This action allows short overload transient pulses to pass through the device without tripping the circuit. If the overcurrent condition persists, the ITIMER capacitor continues to discharge and after it falls by ΔV_{ITIMER}, the circuit-breaker action turns off the FET immediately. At the same time, the ITIMER cap is charged up to V_{INT} again so that it is at its default state before the next overcurrent event. This action ensures the full blanking timer interval is provided for every overcurrent event. Equation 7 can be used to calculate the R_{IMON} value for the desired overcurrent threshold.

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP}} \tag{7}$$

The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. The transient overcurrent blanking interval can be calculated using Equation 8.

$$t_{ITIMER}(ms) = \frac{C_{ITIMER}(nF) \times \Delta V_{ITIMER}(V)}{I_{ITIMER}(\mu A)} \tag{8}$$

Note

1. Leave the ITIMER pin open to allow the part to break the circuit with the minimum possible delay. However, this makes the circuit-breaker response extremely sensitive to noise and can cause false tripping during load transients.
2. Shorting the ITIMER pin to ground results in minimum overcurrent response delay (similar to ITIMER pin open condition), but increases the quiescent current – not a recommended mode of operation.
3. Increasing the ITIMER cap value extends the overcurrent blanking interval. However, it also extends the time needed for the ITIMER cap to recharge up to V_{INT} before the next overcurrent event. If the next overcurrent event occurs before the ITIMER cap is recharged fully, it takes less time to discharge to the VITIMER threshold, thereby it provides a shorter blanking interval than intended.

Figure 8-4 illustrates the overcurrent response for TPS25985x eFuse. After the part shuts down due to a circuit-breaker fault, it either stays latched off (TPS259850 variant) or restarts automatically after a fixed delay (TPS259851 variant).

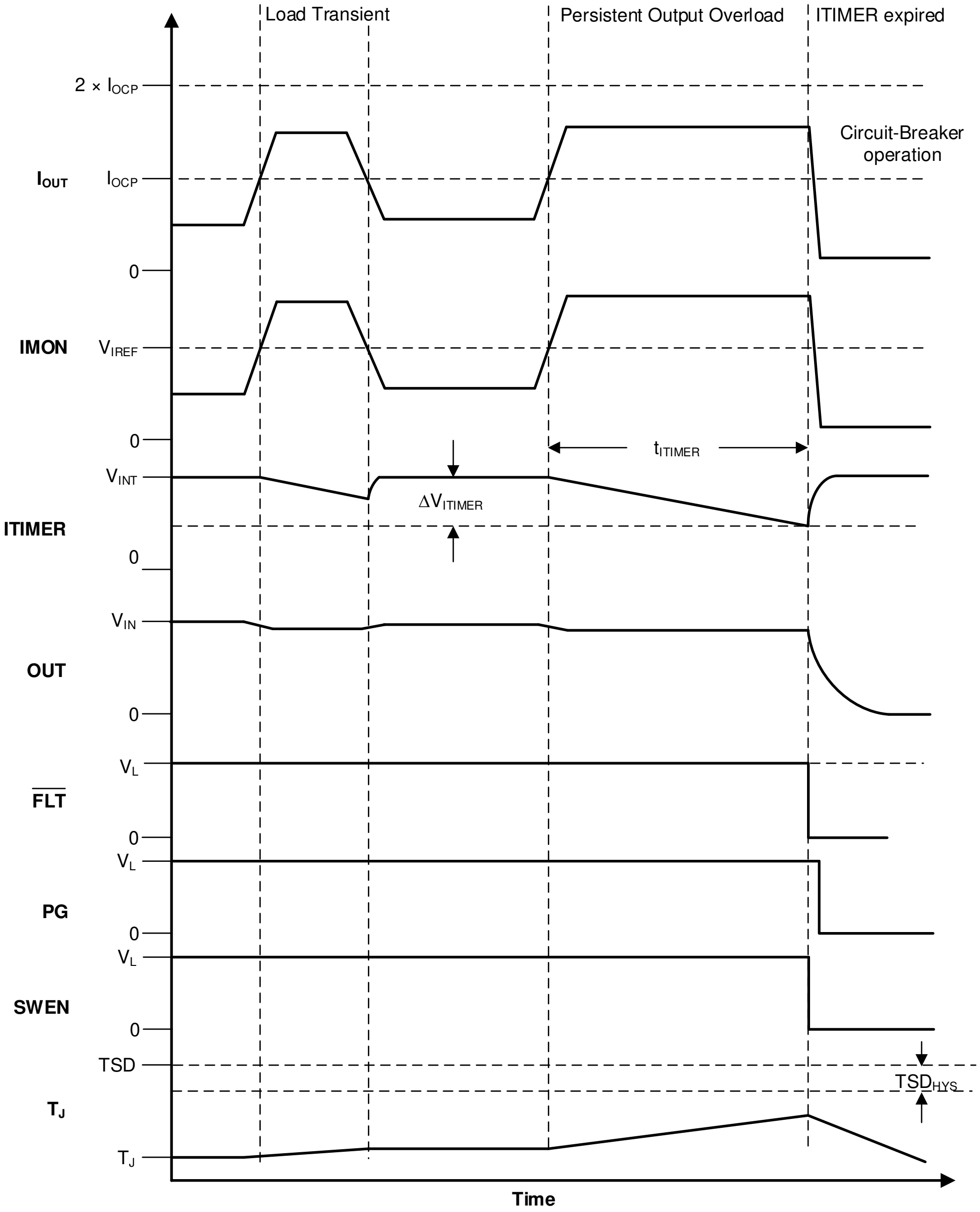


Figure 8-4. Steady-State Overcurrent (Circuit-Breaker) Response

8.3.4.3 Active Current Limiting During Start-Up

The TPS25985x responds to output overcurrent conditions during start-up by actively limiting the current. The device constantly senses the current flowing through each one (I_{DEVICE}) and provides an analog current output (I_{ILIM}) on the ILIM pin, which in turn produces a proportional voltage (V_{ILIM}) across the ILIM pin resistor (R_{ILIM}) as per Equation 9.

$$V_{ILIM} = I_{DEVICE} \times G_{ILIM} \times R_{ILIM} \tag{9}$$

Where G_{ILIM} is the current monitor gain (I_{ILIM} : I_{DEVICE})

The overcurrent condition is detected by comparing this voltage against a threshold which is a scaled voltage ($CLREF_{SAT}$) derived from the reference voltage (V_{IREF}) on the IREF pin as presented in Equation 10.

$$CLREF_{SAT} = \frac{0.7 \times V_{IREF}}{3} \tag{10}$$

The reference voltage (V_{IREF}) can be controlled in two ways, which sets the start-up current limit threshold (I_{LIM}) accordingly.

1. In the standalone mode of operation, the internal current source interacts with the external IREF pin resistor (R_{IREF}) to generate the reference voltage as shown in Equation 11.

$$V_{IREF} = I_{IREF} \times R_{IREF} \tag{11}$$

2. In a primary and secondary configuration, the primary eFuse or controller drives the voltage on the IREF pin to provide an external reference (V_{IREF}).

The active current limit (I_{LIM}) threshold during start-up can be calculated using Equation 12.

$$I_{ILIM} = \frac{CLREF_{SAT}}{G_{ILIM} \times R_{ILIM}} \tag{12}$$

When the load current during start-up exceeds I_{LIM}, the device tries to regulate and hold the load current at I_{LIM}.

During current regulation, the output voltage drops, resulting in increased device power dissipation across the FET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold (TSD), the FET is turned off. After the part shuts down due to a TSD fault, it either stays latched off (TPS259850 variants) or restarts automatically after a fixed delay (TPS259851 variants). See *Overtemperature protection* section for more details on device response to overtemperature.

Note

The active current limit block employs a foldback mechanism during start-up based on the output voltage (V_{OUT}). When V_{OUT} is below the foldback threshold (V_{FB}), the current limit threshold is further lowered.

8.3.4.4 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When an output short-circuit is detected, the internal fast-trip comparator triggers a fast protection sequence to prevent the current from building up further and causing any damage or excessive input supply droop. The fast-trip comparator employs a scalable threshold (I_{SFT}) which is equal to 2 × I_{OCP} (primary device) or 2.25 × I_{OCP} (secondary device) during steady-state and 1.5 × I_{LIM} during inrush. This action enables the user to adjust the fast-trip threshold as per system rating, rather than using a high fixed threshold which can not be suitable for all systems. After the current exceeds the fast-trip threshold, the TPS25985x turns off the FET within t_{SFT}. The device also employs a higher fixed fast-trip threshold (I_{FFT}) to provide fast protection against hard short-circuits during steady-state (FET in linear region). After the current exceeds I_{FFT}, the FET is turned off completely within t_{FFT}. Figure 8-5 illustrates the short-circuit response for TPS25985x eFuse.

In some of the systems, for example blade servers and telecom equipment which house multiple hot-pluggable blades or line cards connected to a common supply backplane, there can be transients on the supply due to switching of large currents through the inductive backplane. This can result in current spikes on adjacent cards which can potentially be large enough to trigger the fast-trip comparator of the eFuse. The TPS25985x uses a proprietary algorithm to avoid nuisance tripping in such cases thereby facilitating uninterrupted system operation.

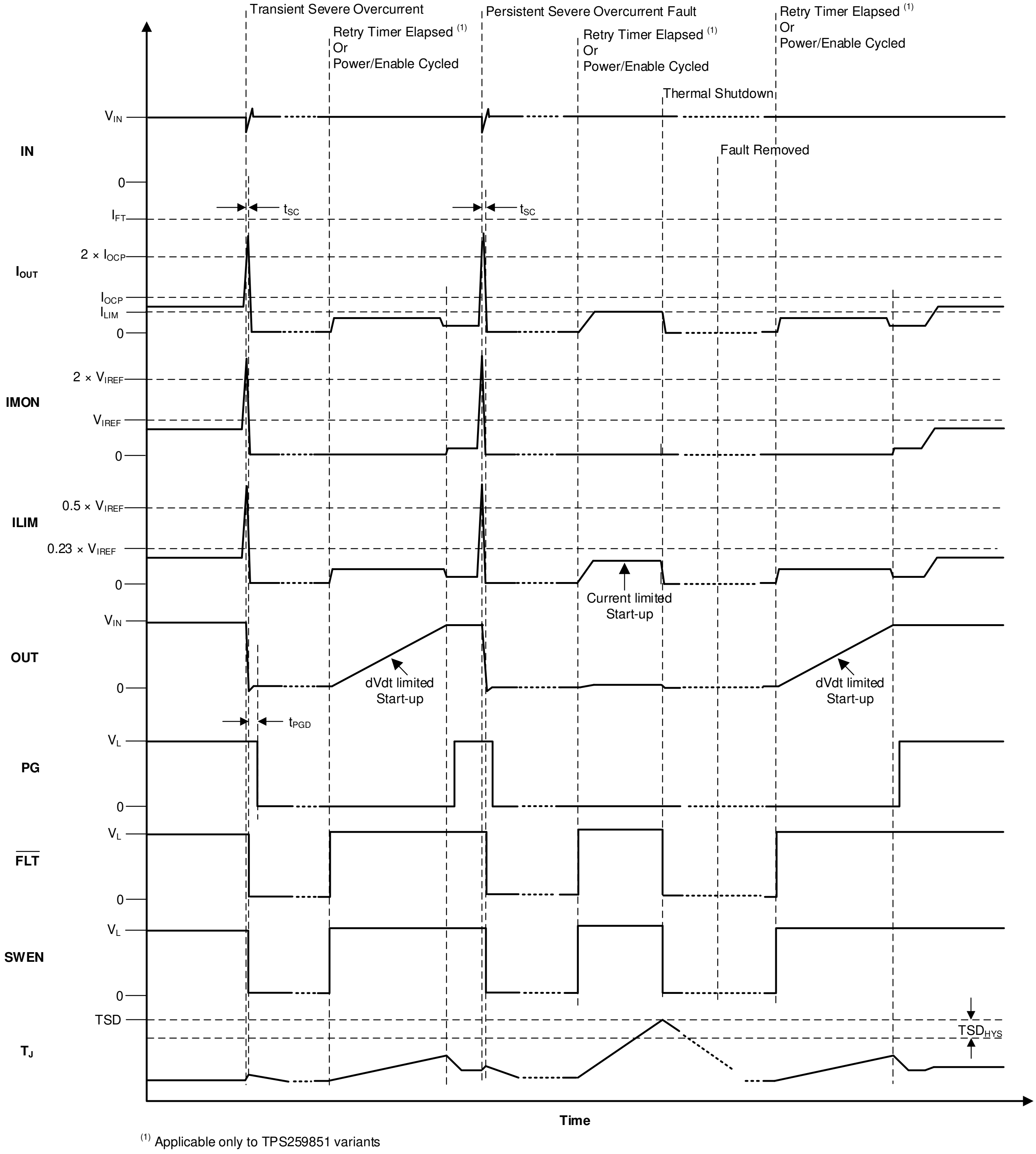


Figure 8-5. Short-Circuit Response

8.3.5 Analog Load Current Monitor (IMON)

The TPS25985x allows the system to monitor the output load current accurately by providing an analog current on the IMON pin which is proportional to the current through the FET. The benefit of having a current output is that the signal can be routed across a board without adding significant errors due to voltage drop or noise coupling from adjacent traces. The current output also allows the IMON pins of multiple TPS25985x devices to be tied together to get the total current in a parallel configuration. The IMON signal can be converted to a voltage by dropping it across a resistor at the point of monitoring. The user can sense the voltage (V_{IMON}) across the R_{IMON} to get a measure of the output load current using Equation 13.

$$I_{OUT} = \frac{V_{IMON}}{G_{IMON} \times R_{IMON}} \tag{13}$$

The TPS25985x IMON circuit is designed to provide high bandwidth and high accuracy across load and temperature conditions, irrespective of board layout and other system operating conditions. This design allows the IMON signal to be used for advanced dynamic platform power management techniques such as Intel PSYS or PROCHOT# to maximize system power usage and platform throughput without sacrificing safety or reliability.

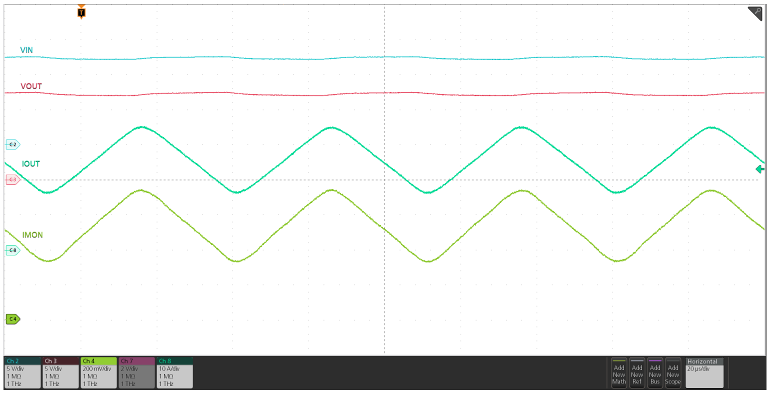


Figure 8-6. Analog Load Current Monitor Response

Note

1. The IMON pin provides load current monitoring information only during steady-state. During inrush, the IMON pin reports zero load current.
2. The ILIM pin reports the individual device load current at all times and can also be used as an analog load current monitor for each individual device.
3. Care must be taken to minimize parasitic capacitance on the IMON and ILIM pins to avoid any impact on the overcurrent and short-circuit protection timing.

8.3.6 Mode Selection (MODE)

This pin can be used to configure the TPS25985x as a primary device in a chain along with other TPS25985x eFuses, designated as secondary devices. This feature allows some of the TPS25985x pin functions to be changed to aid the primary + secondary parallel connection.

This pin is sampled at power up. Leaving the pin open configures it as a primary or standalone device. Connecting this pin to GND configures it as a secondary device.

The following functions are disabled in secondary mode and the device relies on the primary device to provide this functionality:

1. IREF internal current source
2. DVDT internal current source
3. Overcurrent detection in steady-state for circuit-breaker response
4. PG de-assertion (pulldown) after reaching steady-state
5. Latch-off after fault

In secondary mode, the following functions are still active:

1. Overtemperature protection
2. Start-up current limit based on ILIM
3. Active current sharing during inrush as well as steady-state
4. Analog current monitor (IMON) in steady state

5. Steady-state overcurrent detection based on IMON. This is indicated by pulling ITIMER pin low internally, but does not trigger circuit-breaker action on ITIMER expiry. Rather, it relies on the primary device to start its own ITIMER and then trigger the circuit-breaker action for the whole chain by pulling SWEN low after the ITIMER expiry. However, the secondary devices use an internal overcurrent timer as a backup in case the primary device fails to initiate circuit-breaker action for an extended period of time. Refer to *Single Point Failure Mitigation* section for details.
6. Each device still has individual scalable and fixed fast-trip thresholds to protect itself. The individual short-circuit protection threshold is set to maximum, that is 2.25 × I_{OCP} (steady-state) or 2 × I_{LIM} (start-up) in secondary mode so that the primary device can lower it further for the whole system.
7. Individual OVP is set to maximum in secondary device so that the primary can lower it further for the whole system.
8. $\overline{\text{FLT}}$ assertion based on individual device fault detection (except circuit-breaker).
9. PG de-assertion control during inrush and assertion control after device reaches steady state. However, after that in steady state, the secondary device no longer controls the de-assertion of the PG in case of faults.
10. SWEN assertion or de-assertion based on internal events as well as FET ON and OFF control based on SWEN pin status.

In secondary mode, the device behavior during short-circuit and fast-trip is also altered. More details are available in the *Short-Circuit Protection* section.

8.3.7 Parallel Device Synchronization (SWEN)

The SWEN pin is a signal which is driven high when the FET must be turned ON. When the SWEN pin is driven low (internally or externally), it signals the driver circuit to turn OFF the FET. This pin serves both as a control and handshake signal and allows multiple devices in a parallel configuration to synchronize their FET ON and OFF transitions.

Table 8-1. SWEN Summary

Device State	FET Driver Status	SWEN
Steady-state	ON	H
Inrush	ON	H
Overtemperature shutdown	OFF	L
Auto-retry timer running	OFF	L
Undervoltage (EN/UVLO)	OFF	L
Undervoltage (VDD UVP)	OFF	L
Undervoltage (VIN UVP)	OFF	L
Insertion delay	OFF	L
Overvoltage lockout (VIN OVP)	OFF	L
Transient overcurrent	ON	H
Circuit-breaker (persistent overcurrent followed by ITIMER expiry)	OFF	L
Fast-trip	OFF	L
Fault response mono-shot running (MODE = GND)	OFF	L
Fault response mono-shot expired (MODE = GND)	ON	H
ILM pin open (start-up)	OFF	L
ILM pin short (start-up)	OFF	L
ILM pin open (steady-state)	OFF	L
ILM pin short (steady-state)	OFF	L

Table 8-1. SWEN Summary (continued)

Device State	FET Driver Status	SWEN
FET health fault	OFF	L

The SWEN is an open-drain pin and must be pulled up to an external supply.

Note

1. The SWEN pullup supply must be powered up before the eFuse can be turned on. TI recommends to use a system standby rail which is derived from the input of the eFuse.
2. In some cases, it can be possible to use the ITIMER pin as a pullup rail for SWEN pin. Usse a weak pullup to ensure that the loading on the ITIMER is not high enough to affect the ITIMER charging and discharging time.

In a primary + secondary parallel configuration, the SWEN pin is used by the primary device to control the on and off transitions of the secondary devices. At the same time, it allows the secondary devices to communicate any faults or other condition which can prevent it from turning on to the primary device. Refer to *Fault Response and Indication ($\overline{FLT}$)* for more details.

To maintain state machine synchronization, the devices rely on SWEN level transitions as well as timing for handshakes. This ensures all the devices turn ON and OFF synchronously and in the same manner (for example, DVDT controlled or current limited start-up). There are also fail-safe mechanisms in the SWEN control and handshake logic to ensure the entire chain is turned off safely even if the primary device is unable to take control in case of a fault.

Note

TI recommends to keep the parasitic loading on the SWEN pin to a minimum to avoid synchronization timing issues.

8.3.8 Stacking Multiple eFuses for Unlimited Scalability

For systems needing higher current than supported by a single TPS25985x, multiple TPS25985x devices can be connected in parallel to deliver the total system current. Conventional eFuses can not share current equally between themselves during steady-state due to mismatches in their path resistances (which includes the individual device R_{DSON} variation from part to part, as well as the parasitic PCB trace resistance). This fact can lead to multiple problems in the system:

1. Some devices always carry higher current as compared to other devices, which can result in accelerated failures in those devices and an overall reduction in system operational lifetime.
2. As a result, thermal hotspots form on the board, devices, traces, and vias carrying higher current, leading to reliability concerns for the PCB. In addition, this problem makes thermal modeling and board thermal management more challenging for designers.
3. The devices carrying higher current can hit their individual circuit-breaker threshold prematurely even while the total system load current is lower than the overall circuit-breaker threshold. This action can lead to false tripping of the eFuse during normal operation. This has the effect of lowering the current-carrying capability of the parallel chain. In other words, the current rating of the parallel eFuse chain must be de-rated as compared to the sum of the current ratings of the individual eFuses. This de-rating factor is a function of the path resistance mismatch, the number of devices in parallel, and the individual eFuse circuit-breaker accuracy.

The need for de-rating has an adverse impact on the system design. The designer is forced to make one of these trade-offs:

1. Limit the operating load current of the system to below the derated current threshold of the eFuse chain. Essentially, it means lower platform capabilities than are supported by the power supply (PSU).

2. Increase the overall circuit-breaker threshold to allow the desired system load current to pass through without tripping. As a consequence, the power supply (PSU) must be oversized to deliver higher currents during faults to account for the de-grading of the overall circuit-breaker accuracy.

In either case, the system suffers from poor power supply utilization, which can mean sub-optimal system throughput or increased installation and operating costs, or both.

The TPS25985x uses a proprietary technique to address these problems and provide unlimited scalability of the solution by paralleling as many eFuses as needed. This is incorporated without unequal current sharing or any degradation in accuracy.

For this scheme to work correctly, the devices must be connected in the following manner:

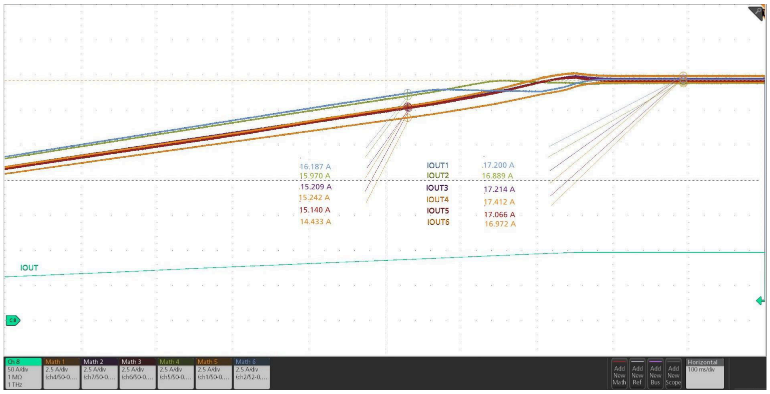
- The SWEN pins of all the devices are connected together.
- The IMON pins of all the devices must be connected together. The R_{IMON} resistor value on the combined IMON pin can be calculated using Equation 14.

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP(TOTAL)}} \tag{14}$$

- The R_{ILIM} for each individual eFuse must be selected based on Equation 15.

$$R_{ILIM} = \frac{1.1 \times N \times R_{IMON}}{3} \tag{15}$$

Where N = number of devices in parallel chain. Figure 8-7 illustrates the response of the active current sharing block in TPS25985 eFuse during steady-state.



Intentional skew is introduced between the power path resistances for six devices and the load current is ramped up slowly. Equal current distribution is seen between all devices after the current through each device exceeds the active current sharing threshold.

Figure 8-7. Active Current Sharing During Steady-State with Six TPS25985x eFuses in Parallel

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Note

The active current sharing scheme is engaged when the current through any eFuse while in steady-state exceeds the individual current sharing threshold set by the R_{ILIM} based on Equation 16.

$$R_{ILIM} = \frac{1.1 \times V_{IREF}}{3 \times G_{ILIM} \times I_{LIM(ACS)}} \tag{16}$$

The active current sharing scheme is disengaged when the total system current exceeds the system overcurrent (circuit-breaker) threshold ($I_{OCP(TOTAL)}$).

8.3.8.1 Current Balancing During Start-Up

The TPS25985x implements a proprietary current balancing mechanism during start-up, which allows multiple TPS25985x devices connected in parallel to share the inrush current and distribute the thermal stress across all the devices. This feature helps to complete a successful start-up with all the devices and avoid a scenario where some of the eFuses hit thermal shutdown prematurely. This in effect increases the inrush current capability of the parallel chain. The improved inrush performance makes it possible to support very large load capacitors on high current platforms without compromising the inrush time or system reliability.

8.3.9 Analog Junction Temperature Monitor (TEMP)

The device allows the system to monitor the junction temperature (T_J) accurately by providing an analog voltage on the TEMP pin which is proportional to the temperature of the die. This voltage can be connected to the ADC input of a host controller or eFuse with digital telemetry. In a multi-device parallel configuration, the TEMP outputs of all devices can be tied together. In this configuration, the TEMP signal reports the temperature of the hottest device in the chain.

Note

1. The TEMP pin voltage is used only for external monitoring and does not interfere with the overtemperature protection scheme of each individual device which is based purely on the internal temperature monitor.
2. TI recommends to add a capacitance of 22 pF on the TEMP pin to filter out glitches during system transients.
3. The current source on the TEMP pin of TPS25985x is internally clamped to a safe value to protect against overload, short circuit on this pin. This can lead to incorrect temperature reporting on the TEMP when the number of devices connected in parallel is higher than 6. This limitation can be overcome by connecting an external pull-resistance on the TEMP pin.

8.3.10 Overtemperature Protection

The TPS25985x employs an internal thermal shutdown mechanism to protect itself when the internal FET becomes too hot to operate safely. When the TPS259850 detects thermal overload, it shuts down and remains latched-off until the device is power cycled or re-enabled. When the TPS259851 detects thermal overload, it remains off until it has cooled down sufficiently. Thereafter, the device remains off for an additional delay of t_{RST} after which it automatically retries to turn on if it is still enabled.

Table 8-2. Overtemperature Protection Summary

Device	Enter TSD	Exit TSD
TPS259850 (Latch-Off)	$T_J \geq$ TSD	$T_J <$ TSD – TSD_{HYS} VDD cycled to 0 V and then above $V_{UVP(R)}$ or EN/UVLO toggled below $V_{SD(F)}$
TPS259851 (Auto-Retry)	$T_J \geq$ TSD	$T_J <$ TSD – TSD_{HYS} t_{RST} timer expired or VDD cycled to 0 V and then above $V_{UVP(R)}$ or EN/UVLO toggled below $V_{SD(F)}$

8.3.11 Fault Response and Indication ($\overline{\text{FLT}}$)

Table 8-3 summarizes the device response to various fault conditions.

Table 8-3. Fault Summary

Event or Condition	Device Response	Fault Latched Internally	$\overline{\text{FLT}}$ Pin Status	Delay
Steady-state	None	N/A	H	
Inrush	None	N/A	H	
Overtemperature	Shutdown	Y	L	
Undervoltage (EN/UVLO)	Shutdown	N	H	
Undervoltage (VDD UVP)	Shutdown	N	H	
Undervoltage (VIN UVP)	Shutdown	N	H	
Overvoltage (VIN OVP)	Shutdown	N	H	
Transient overcurrent	None	N	H	
Persistent overcurrent (steady-state)	Circuit-Breaker	Y	L	t_{ITIMER}
Persistent overcurrent (start-up)	Current Limit	N	L	
Short-circuit (primary mode)	Fast-trip	Y	L	t_{FT}
Short-circuit (secondary mode)	Fast-trip followed by current limited Start-up	N	H	
ILIM pin open (start-up)	Shutdown	Y	L	
ILIM pin short (start-up)	Shutdown (if I_{OUT} > I_{OC_BKP})	Y	L	
ILIM pin open (steady-state)	Active current sharing loop always active	N	H	
ILIM pin short (steady-state)	Active current sharing loop disabled	N	H	
IMON pin open (steady-state)	Shutdown	Y	L	
IMON pin short (steady-state)	Shutdown (If I_{OUT} > I_{OC_BKP})	Y	L	45 µs
IREF pin open (start-up)	Shutdown (If I_{OUT} > I_{OC_BKP})	Y	L	
IREF pin open (steady-state)	Shutdown (if I_{OUT} > I_{OC_BKP})	Y	L	t_{ITIMER}
IREF pin short (steady-state)	Shutdown	Y	L	
IREF pin short (start-up)	Shutdown	Y	L	
ITIMER pin forced to high voltage	Shutdown (if I_{OUT} > I_{OCP} or I_{OUT} > I_{OC_BKP})	Y	L	t_{SPFAIL_TMR}
Start-up timeout	Shutdown	Y	L	t_{SU_TMR}
FET health fault (G-S)	Shutdown	Y	L	10 µs
FET health fault (G-D)	Shutdown	Y	L	
FET health fault (D-S)	Shutdown	N	L	t_{SU_TMR}

Table 8-3. Fault Summary (continued)

Event or Condition	Device Response	Fault Latched Internally	$\overline{FLT}$ Pin Status	Delay
External fault (SWEN pulled low externally while device is not in UV or OV)	Shutdown	Y	L	

$\overline{FLT}$ is an open-drain pin and must be pulled up to an external supply.

The device response after a fault varies based on the mode of operation:

1. During standalone or primary mode of operation (MODE = OPEN), the device latches a fault and follows the auto-retry or latch-off response as per the device selection. When the device turns on again, it follows the usual DVDT limited start-up sequence.
2. During the secondary mode of operation (MODE = GND), if the device detects any fault, it pulls the SWEN pin low momentarily to signal the event to the primary device and thereafter relies on the primary to take control of the fault response. However, if the primary device fails to register the fault, there i a failsafe mechanism in the secondary device to turn off the entire chain and enter a latch-off condition. Thereafter, the device can be turned on again only by power cycling VDD below $V_{UVP(F)}$ or by cycling EN/UVLO pin below $V_{SD(F)}$.

For faults that are latched internally, power cycling the part or pulling the EN/UVLO pin voltage below $V_{SD(F)}$ clears the fault and the pin is de-asserted. This action also clears the t_{RST} timer (auto-retry variants only). Pulling the EN/UVLO just below the UVLO threshold has no impact on the device in this condition. This is true for both latch-off and auto-retry variants.

8.3.12 Power Good Indication (PG)

Power Good indication is an active high output which is asserted high to indicate when the device is in steady-state and capable of delivering maximum power.

Table 8-4. PG Indication Summary

Event or Condition	FET Status	PG Pin Status	PG Delay
Undervoltage ($V_{EN} < V_{UVLO}$)	OFF	L	t_{PGD}
$V_{IN} < V_{UVP}$	OFF	L	
$V_{DD} < V_{UVP}$	OFF	L	
Overvoltage ($V_{IN} > V_{OVP}$)	OFF	L	t_{PGD}
Steady-state	ON	H	t_{PGA}
Inrush	ON	L	t_{PGA}
Transient overcurrent	ON	H	N/A
Circuit-breaker (persistent overcurrent followed by ITIMER expiry)	OFF	L (MODE = H) H (MODE = L)	t_{PGD} N/A
Fast-trip	OFF	L (MODE = H) H (MODE = L)	t_{PGD} N/A
ILM pin open	OFF	L (MODE = H) H (MODE = L)	$t_{ITIMER} + t_{PGD}$ N/A
ILM pin short	OFF	L (MODE = H) H(MODE = L)	t_{PGD} N/A
Overtemperature	Shutdown	L (MODE = H) H (MODE = L)	t_{PGD} N/A

After power up, PG is pulled low initially. The device initiates an inrush sequence in which the gate driver circuit starts charging the gate capacitance from the internal charge pump. When the FET gate voltage reaches the full overdrive indicating that the inrush sequence is complete and the device is capable of delivering full power, the PG pin is asserted HIGH after a de-glitch time (t_{PGA}).

The PG is de-asserted if the FET is turned off at any time during normal operation. The PG de-assertion de-glitch time is t_{PGD}.

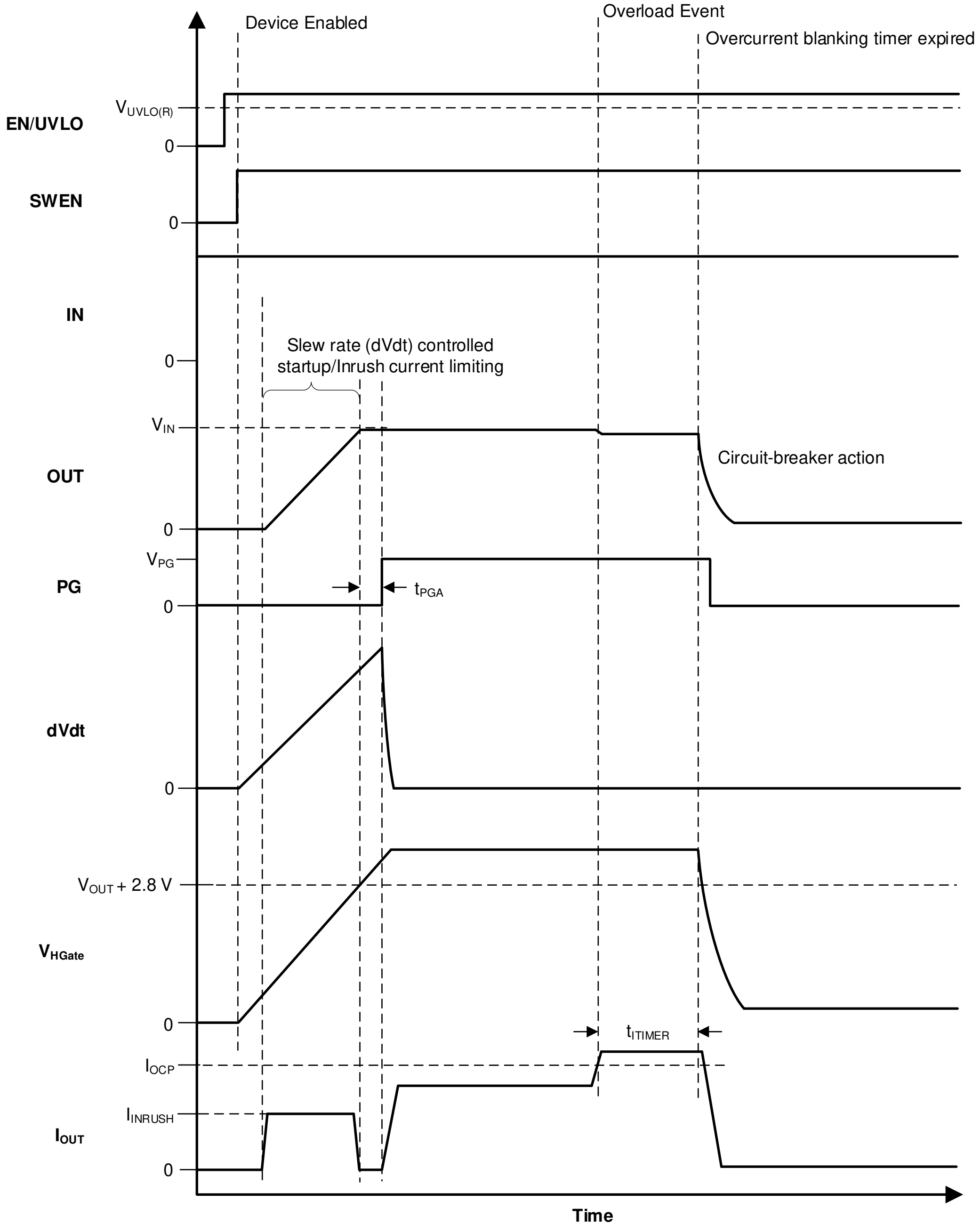


Figure 8-8. TPS25985x PG Timing Diagram

The PG is an open-drain pin and must be pulled up to an external supply.

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pulldown in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pullup supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

When the device is used in secondary mode (MODE = GND) in conjunction with another TPS25985 device as a primary device in a parallel chain, it controls the PG assertion during start-up, but after the device reaches steady-state, it no longer has control over the PG de-assertion. Refer to the *Mode Selection (MODE)* for more details.

8.3.13 Output Discharge

The device has an integrated output discharge function which discharges the capacitors on the OUT pin using an internal constant current (I_{QOD}) to GND. The output discharge function is activated when the EN/UVLO is held low ($V_{SD(F)} < V_{EN} < V_{UVLO(F)}$) for a minimum interval (t_{QOD}). The output discharge function helps to rapidly remove the residual charge left on large output capacitors and prevents the bus from staying at some undefined voltage for extended periods of time. The output discharge is disengaged when $V_{OUT} < V_{FB}$ or if the device detects a fault.

The output discharge function can result in excessive power dissipation inside the device leading to an increase in junction temperature (T_J). The output discharge is disabled if the junction temperature (T_J) crosses TSD to avoid long-term degradation of the part.

Note

In a primary+secondary parallel configuration, TI recommends to hold EN/UVLO voltage below the $V_{UVLO(F)}$ threshold of the secondary device to activate output discharge for all the devices in the chain.

8.3.14 General Purpose Comparator

The device has a spare general purpose comparator whose inputs (CMPP, CMPM) and output (CMPOUT) are not connected to any internal logic, thereby allowing the user complete flexibility to use this comparator as per the system needs.

The comparator can be used for various purposes. Here are a few examples:

- **Adjustable fast overcurrent detect (PROCHOT#):** IMON pin is connected to CMPM input and an appropriate reference voltage is connected to CMPP input. CMPOUT is connected to the PROCHOT# pin of the processor. When the load current crosses the set threshold, the CMPOUT goes low and signals the processor to throttle down immediately.

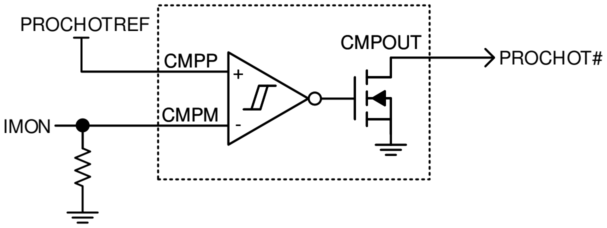


Figure 8-9. Adjustable Fast Overcurrent (PROCHOT#) Detect Using Internal Comparator

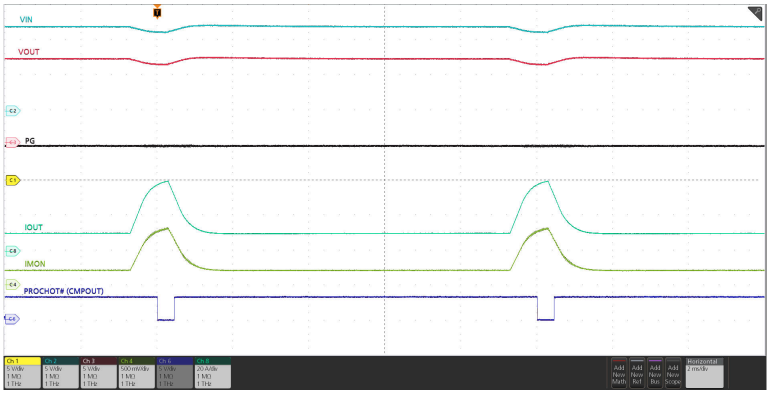


Figure 8-10. PROCHOT# Response Using Internal Comparator

- **Fast overvoltage protection with adjustable threshold:** Input supply is connected to CMPM input through a resistor divider and an appropriate reference voltage is connected to CMPP input. CMPOUT is connected to the EN/UVLO pin. When the input supply crosses the set threshold, the CMPOUT goes low and turns off the part.

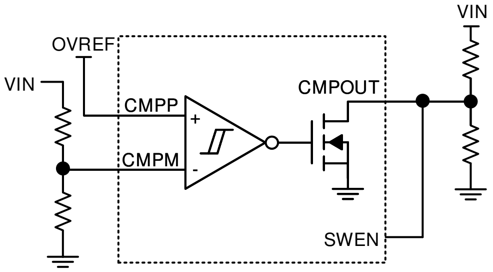


Figure 8-11. Fast Overvoltage Protection with Adjustable Threshold Using Internal Comparator

- **Load handshake or detect timer:** An R-C network from VOUT supply is connected to CMPM input through a resistor divider and an appropriate reference voltage is connected to the CMPP input. CMPOUT is connected to the EN/UVLO pin. After the device turns on, the R-C on VOUT starts charging and after it crosses the threshold, CMPOUT goes low to pull down the EN/UVLO and turn off the device, unless the downstream circuit indicates it has powered up successfully by driving the CMPM input low within the expected amount of time determined by the R-C time constant.

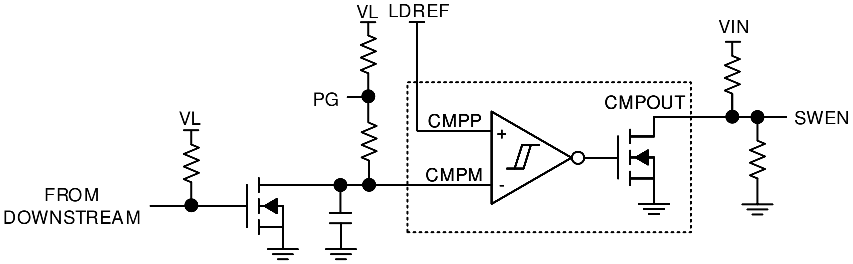


Figure 8-12. Load Handshake or Detect Timer Using Internal Comparator

8.3.15 FET Health Monitoring

The TPS25985x can detect and report certain conditions which are indicative of a failure of the power path FET. If undetected or unreported, these conditions can compromise system performance by not providing power to the load correctly or by not providing the necessary level of protection. After a FET failure is detected, the TPS25985x tries to turn off the internal FET by pulling the gate low and asserts the $\overline{\text{FLT}}$ pin.

- **D-S short:** D-S short can result in a constant uncontrolled power delivery path formed from source to load, either due to a board assembly defect or due to internal FET failure. This condition is detected at start-up by checking if $V_{IN\text{-}OUT} < V_{DSFLT}$ before the FET is turned ON. If yes, the device engages the internal output discharge to try and discharge the output. If the V_{OUT} does not discharge below V_{FB} within a certain allowed interval, the device asserts the $\overline{FLT}$ pin.

- **G-D short:** The TPS25985x detects this kind of FET failure at all times by checking if the gate voltage is close to V_{IN} even when the internal control logic is trying to hold the FET in OFF condition.
- **G-S short:** The TPS25985x detects this kind of FET failure during start-up by checking if the FET G-S voltage fails to reach the necessary overdrive voltage within a certain timeout period (t_{SU_TMR}) after the gate driver is turned ON. While in steady-state, if the G-S voltage becomes low before the controller logic has signaled to the gate driver to turn off the FET, it is latched as a fault.

8.3.16 Single Point Failure Mitigation

The TPS25985x relies on the proper component connections and biasing on the IMON, ILIM, IREF, and ITIMER pins to provide overcurrent and short-circuit protection under all circumstances. As an added safety measure, the device uses the following mechanisms to ensure that the device provides some form of overcurrent protection even if any of these pins are not connected correctly in the system or the associated components have a failure in the field.

8.3.16.1 IMON Pin Single Point Failure

- **IMON pin open:** In this case, the IMON pin voltage is internally pulled up to a higher voltage and exceeds the threshold (V_{IREF}), causing the part to perform a circuit-breaker action even if there is no significant current flowing through the device.
- **IMON pin shorted to GND directly or through a very low resistance:** In this case, the IMON pin voltage is held at a low voltage and is not allowed to exceed the threshold (V_{IREF}) even if there is significant current flowing through the device, thereby rendering the primary overcurrent protection mechanism ineffective. The device relies on an internal overcurrent sense mechanism to provide some protection as a backup. If the device detects that the backup current sense threshold (I_{OC_BKP}) is exceeded but at the same time the primary overcurrent detection on IMON pin fails, it triggers single point failure detection and latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted.

8.3.16.2 ILIM Pin Single Point Failure

- **ILIM pin open:** In this case, the ILIM pin voltage is internally pulled up to a higher voltage and exceeds the V_{IREF} threshold, causing the part to engage the current limit even if there is no significant current flowing through the device.
- **ILIM pin shorted to GND directly or through a very low resistance:** In this case, the ILIM pin voltage is held at a low voltage and is not allowed to exceed the start-up current limit threshold even if there is significant current flowing through the device, thereby rendering the primary current limit mechanism ineffective during start-up. The device relies on an internal overcurrent detection mechanism to provide some protection as a backup. If the device detects that the backup overcurrent threshold (IOC_BKP) is exceeded but at the same time the primary overcurrent detection on ILIM pin fails, it triggers single point failure detection and latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted.

8.3.16.3 IREF Pin Single Point Failure

- **IREF pin open or forced to higher voltage:** In this case, the IREF pin (V_{IREF}) is pulled up internally or externally to a voltage which is higher than the target value as per the recommended I_{OCP} or I_{LIM} calculations, preventing the primary circuit-breaker, active current limit, and short-circuit protection from getting triggered even if there is significant current flowing through the device. The device relies on an internal overcurrent detection mechanism to provide some protection as a backup. If the device detects that the backup overcurrent threshold is exceeded but at the same the primary overcurrent or short-circuit detection on ILIM or IMON pin fails, it triggers single point failure detection and latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted.
- **IREF pin shorted to GND:** In this case, the V_{IREF} threshold is set to 0 V, causing the part to perform active current limit or circuit-breaker action even if there is no significant current flowing through the device.

8.3.16.4 ITIMER Pin Single Point Failure

- **ITIMER pin open or short to GND:** In this case, the ITIMER pin is already discharged below $V_{ITIMERTHR}$ and hence indicates overcurrent blanking timer expiry instantaneously after an overcurrent event and triggers a circuit-breaker action without any delay.
- **ITIMER pin forced to some voltage higher than $V_{ITIMERTHR}$:** In this case, the ITIMER pin is unable to discharge below $V_{ITIMERTHR}$ and hence fails to indicate overcurrent blanking timer expiry, thereby rendering the primary circuit-breaker mechanism ineffective. The device relies on a backup overcurrent timer mechanism to provide some protection as a backup. If the device detects an overcurrent event on either the IMON pin or the backup overcurrent detection circuit, the device engages the internal backup time and after the timer expires ($t_{SPFLTMR}$), it latches a fault. The FET is turned off and the $\overline{FLT}$ pin is asserted.

8.4 Device Functional Modes

The features of the device depend on the operating mode. Table 8-5 and Table 8-6 summarize the device functional modes.

Table 8-5. Device Functional Modes Based on EN/UVLO Pin

Pin: EN/UVLO	Device State	Output Discharge
$> V_{UVLO(R)}$	Fully ON	Disabled
$> V_{SD(F)}$, $< V_{UVLO(F)}$ ($< t_{QOD}$)	FET OFF	Disabled
$> V_{SD(F)}$, $< V_{UVLO(F)}$ ($> t_{QOD}$)	FET OFF	Enabled
$< V_{SD(F)}$	Shutdown	Disabled

Table 8-6. Device Functional Modes Based on MODE Pin

Pin: MODE	Device Configuration
Open	Primary or standalone
GND	Secondary

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS25985x is a high-current eFuse that is typically used for power rail protection applications. The device operates from 4.5 V to 16 V with input overvoltage and adjustable undervoltage protection. The device provides ability to control inrush current and offers protection against overcurrent and short-circuit conditions. The device can be used in a variety of systems such as server motherboards, add-on cards, graphics cards, accelerator cards, enterprise switches, routers, and so forth. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirements. Additionally, a spreadsheet design tool, *TPS25985x Design Calculator* is available in the web product folder.

9.1.1 Single Device, Standalone Operation

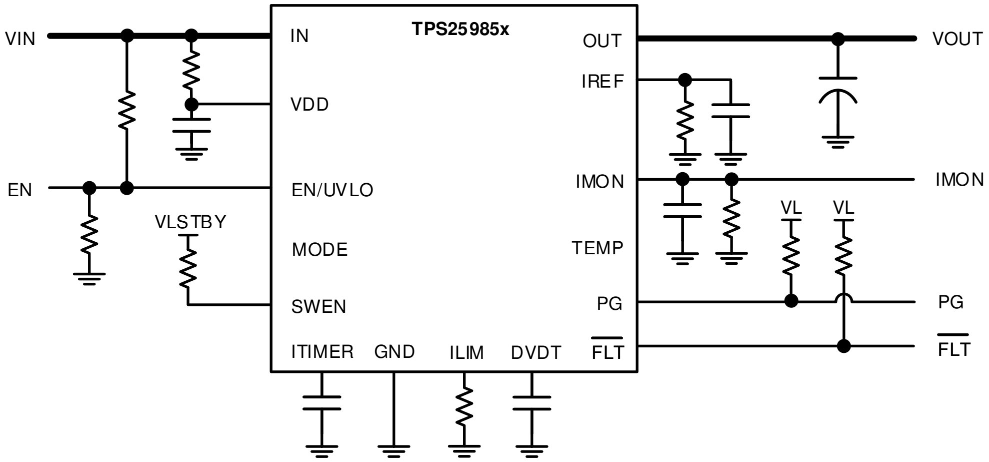


Figure 9-1. Single Device, Standalone Operation

Note

The MODE pin is left OPEN to configure for standalone operation.

Other variations:

1. The IREF pin can be driven from an external reference voltage source.
2. In a host MCU controlled system, EN/UVLO can be connected to a GPIO pin to control the device. IMON pin voltage can be monitored using an ADC. The host MCU can use a DAC to drive IREF to change the current limit threshold dynamically.
3. The device can be used as a simple high current load switch without adjustable overcurrent or fast-trip protection by tying the ILIM and IMON pins to GND and leaving the IREF pin open. The inrush current protection, fixed fast-trip and internal fixed overcurrent protection are still active in this condition.
4. The CMPP, CMPM, and CMPOUT pins can be used to implement adjustable OVP or PG thresholds or PROCHOT# or Load Handshake timer functionality as described in the *General Purpose Comparator* section.

9.1.2 Multiple Devices, Parallel Connection

Applications which need higher current capability can use two or more TPS25985x devices connected in parallel as shown in Figure 9-2.

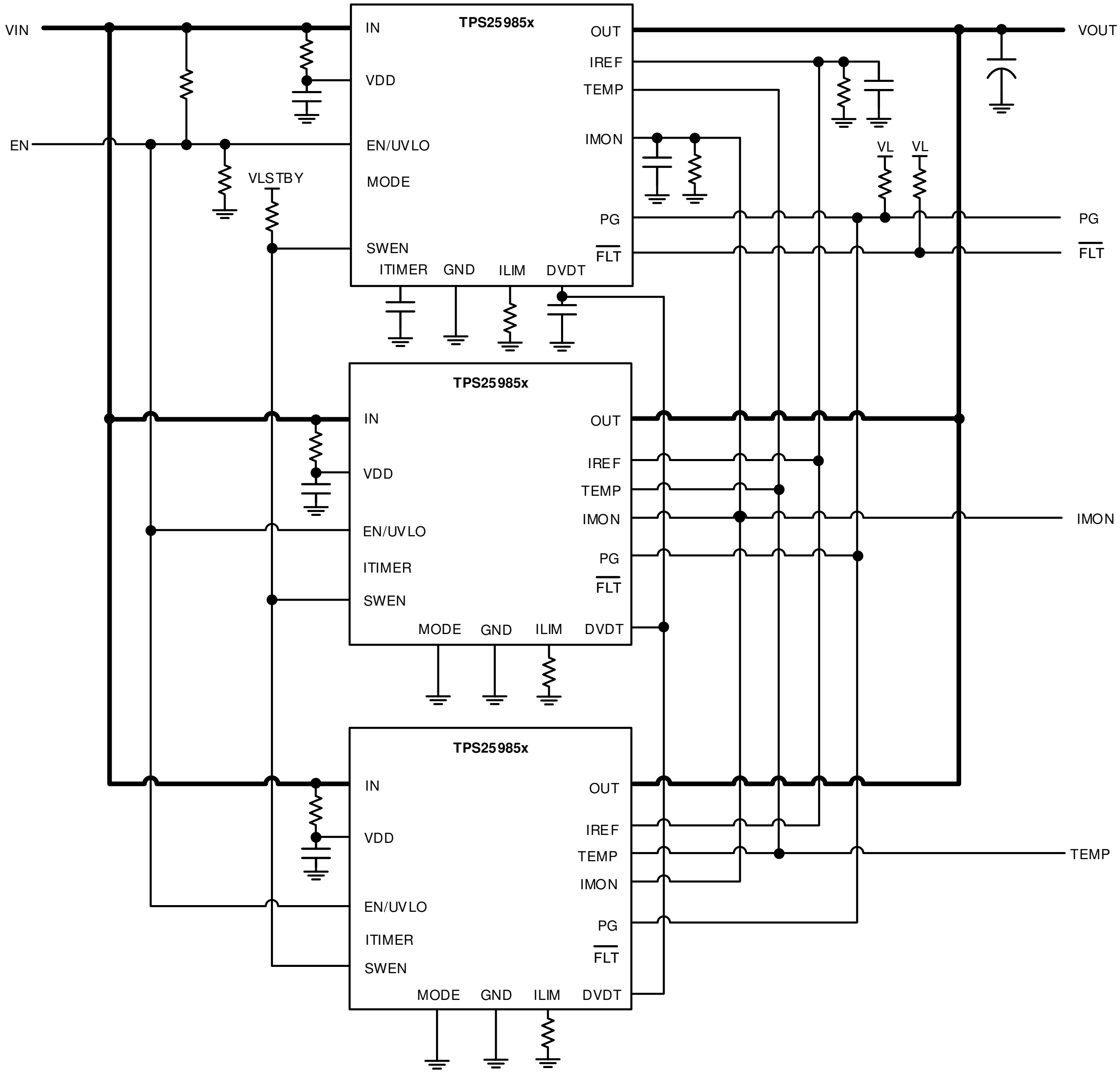


Figure 9-2. Devices Connected in Parallel for Higher Current Capability

In this configuration, one TPS25985x device is designated as the primary device and controls the other TPS25985x devices in the chain which are designated as secondary devices. This configuration is achieved by connecting the primary device as follows:

1. VDD is connected to IN through an R-C filter.
2. MODE pin is left OPEN.
3. ITIMER is connected through capacitor to GND.
4. DVDT is connected through capacitor to GND.
5. IREF is connected through resistor to GND.

6. IMON is connected through resistor to GND.
7. ILIM is connected through resistor to GND.
8. SWEN is pulled up to a 3.3-V to 5-V standby rail. This rail must be powered up independent of the eFuse.

The secondary devices must be connected in the following manner:

1. VDD is connected to IN through a R-C filter.
2. MODE pin is connected to GND.
3. ITIMER pin is left OPEN.
4. ILIM is connected through resistor to GND.

The following pins of all devices must be connected together:

1. IN
2. OUT
3. EN/UVLO
4. DVDT
5. SWEN
6. PG
7. IMON
8. IREF

In this configuration, all the devices are powered up and enabled simultaneously.

Power up: After power up or enable, all devices initially hold their SWEN low till the internal blocks are biased and initialized correctly. After that, each device releases its own SWEN. After all devices have released their SWEN, the combined SWEN goes high and the devices are ready to turn on their respective FETs at the same time.

Inrush: During inrush, because the DVDT pins are tied together to a single DVDT capacitor all the devices turn on the output with the same slew rate (SR). Choose the common DVDT capacitor (C_{DVDT}) as per the following Equation 17 and Equation 18.

$$SR(V/ms) = \frac{I_{INRUSH}(A)}{C_{LOAD}(mF)} \tag{17}$$

$$C_{DVDT}(pF) = \frac{42000}{SR(V/ms)} \tag{18}$$

In this condition, the internal balancing circuit ensures that the load current is shared among all devices during start-up. This action prevents a situation where some devices turn on faster than others and experience more thermal stress as compared to other devices. This can potentially result in premature or partial shutdown of the parallel chain, or even SOA damage to the devices. The current balancing scheme ensures the inrush capability of the chain scales according to the number of devices connected in parallel, thereby ensuring successful start-up with larger output capacitances or higher loading during start-up.

All devices hold their respective PG signals low during start-up. After the output ramps up fully and reaches steady-state, each device releases its own PG pulldown. Because the DVDT pins of all devices are tied together, the internal gate high detection of all devices is synchronized. There can be some threshold or timing mismatches between devices leading to PG assertion in a staggered manner. However, since the PG pins of all devices are tied together, the combined PG signal becomes high only after all devices have released their PG pulldown. This signal is sent to the downstream loads to allow power to be drawn.

Steady-state: During steady-state, all devices share current equally using the active current sharing mechanism which actively regulates the respective device R_{DSON} to evenly distribute current across all the devices in the parallel chain.

Overcurrent during steady-state: The circuit-breaker threshold for the parallel chain is based on the total system current rather than the current flowing through individual devices. This is done by connecting the IMON pins of all the devices together. Similarly, the IREF pins of all devices are tied together and connected to a single R_{IREF} (or an external V_{IREF} source) to generate a common reference for the overcurrent protection block in all the devices. This action helps minimize the contribution of I_{IREF} variation and R_{IREF} tolerance to the overall mismatch in overcurrent threshold between devices. In this case, choose the combined R_{IMON} as per the following Equation 19:

$$R_{IMON} = \frac{I_{IREF} \times R_{IREF}}{G_{IMON} \times I_{OCP(TOTAL)}} \tag{19}$$

The R_{ILIM} value for each individual eFuse must be selected based on the following Equation 20.

$$R_{ILIM} = \frac{1.1 \times N \times R_{IMON}}{3} \tag{20}$$

Where N = number of devices in parallel chain.

Other variations:

The IREF pin can be driven from an external voltage reference (V_{IREF}).

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP(TOTAL)}} \tag{21}$$

During an overcurrent event, the overcurrent detection of all the devices is triggered simultaneously. This in turn triggers the overcurrent blanking timer (ITIMER) on each device. However, only the primary device uses the ITIMER expiry event as a trigger to pull the SWEN low for all the devices, thereby initiating the circuit-breaker action for the whole chain. This mechanism ensures that mismatches in the current distribution, overcurrent thresholds and ITIMER intervals among the devices do not degrade the accuracy of the circuit-breaker threshold of the complete parallel chain or the overcurrent blanking interval.

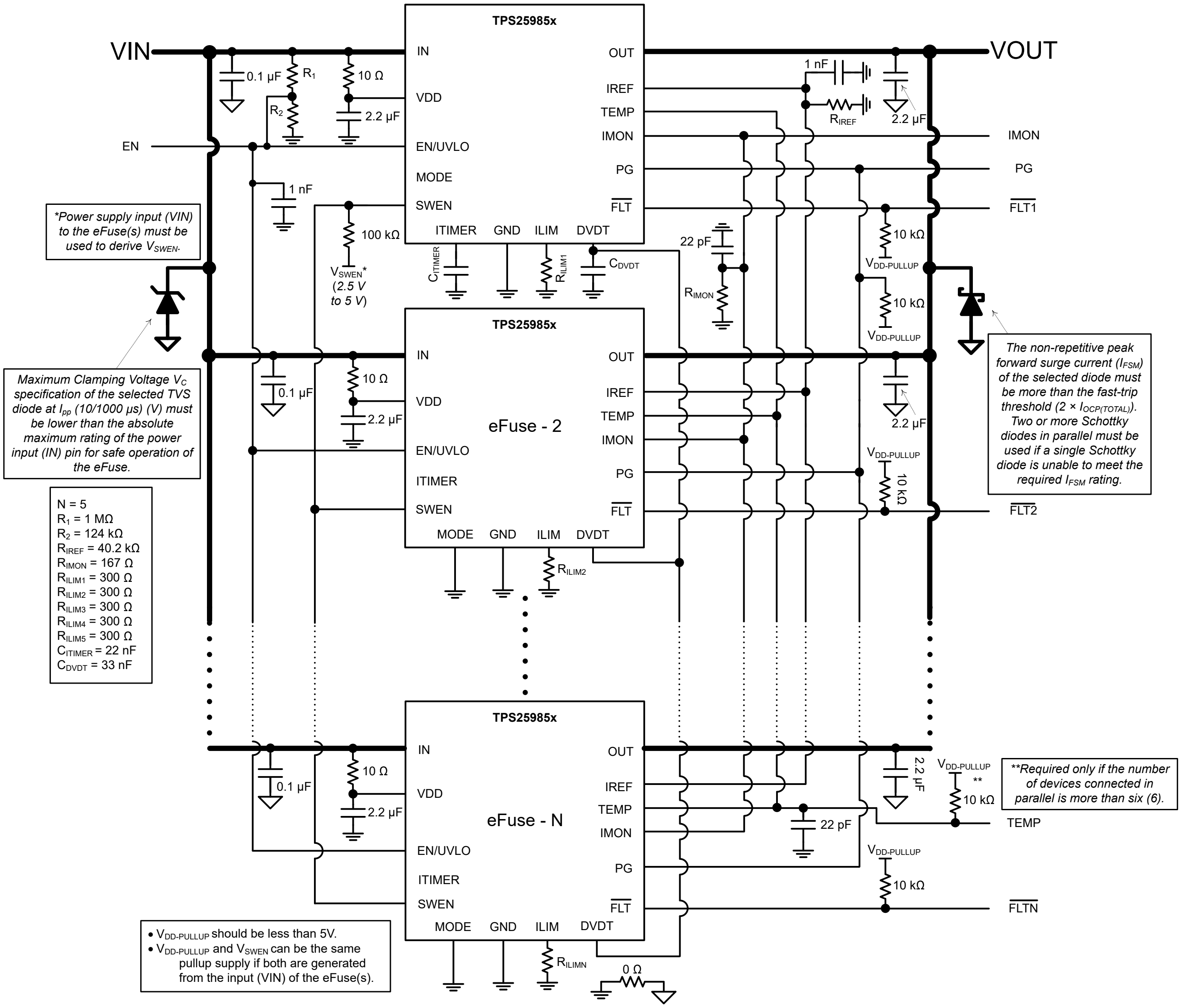
However, the secondary devices also start their backup overcurrent timer and can trigger the shutdown of the whole chain if the primary device fails to do so within a certain interval.

Severe overcurrent (short-circuit): If there is a severe fault at the output (for example, output shorted to ground with a low impedance path) during steady-state operation, the current builds up rapidly to a high value and triggers the fast-trip response in each device. The devices use two thresholds for fast-trip protection – a user-adjustable threshold (I_{SFT} = 2 × I_{OCP} in steady-state or I_{SFT} = 2 × I_{LIM} during inrush) as well as a fixed threshold (I_{FFT} only during steady-state). After the fast-trip, the devices enter into a latch-off fault condition till the device is power cycled or re-enabled or expires the auto-retry timer (only for auto-retry variants).

9.2 Typical Application: 12-V, 3.6-kW Power Path Protection in Datacenter Servers

9.2.1 Application

This design example considers a 12-V system operating voltage with a tolerance of ±10%. The maximum steady-state load current is 300 A. If the load current exceeds 330 A, the eFuse circuit must allow transient overload currents up to a 16-ms interval. For persistent overloads lasting longer than that, the eFuse circuit must break the circuit and then latch-off. The eFuse circuit must charge a bulk capacitance of 55 mF and support approximately 12% of the steady-state load during start-up. Figure 9-3 shows the application schematic for this design example.



*Power supply input (VIN) to the eFuse(s) must be used to derive V_{SWEN}.

Maximum Clamping Voltage V_C specification of the selected TVS diode at I_{pp} (10/1000 µs) (V) must be lower than the absolute maximum rating of the power input (IN) pin for safe operation of the eFuse.

N = 5
R_1 = 1 MΩ
R_2 = 124 kΩ
R_{IREF} = 40.2 kΩ
R_{IMON} = 167 Ω
R_{ILIM1} = 300 Ω
R_{ILIM2} = 300 Ω
R_{ILIM3} = 300 Ω
R_{ILIM4} = 300 Ω
R_{ILIM5} = 300 Ω
C_{ITIMER} = 22 nF
C_{DVDT} = 33 nF

The non-repetitive peak forward surge current (I_{FSM}) of the selected diode must be more than the fast-trip threshold (2 × $I_{OCP(TOTAL)}$). Two or more Schottky diodes in parallel must be used if a single Schottky diode is unable to meet the required I_{FSM} rating.

**Required only if the number of devices connected in parallel is more than six (6).

- $V_{DD-PULLUP}$ should be less than 5V.
- $V_{DD-PULLUP}$ and V_{SWEN} can be the same pullup supply if both are generated from the input (VIN) of the eFuse(s).

Figure 9-3. Application Schematic for a 12-V, 3.6-kW Power Path Protection Circuit

9.2.2 Design Requirements

Table 9-1 shows the design parameters for this application example.

Table 9-1. Design Parameters

PARAMETER	VALUE
Input voltage range (V_{IN})	10.8 V – 13.2 V
Maximum DC load current ($I_{OUT(max)}$)	300 A
Maximum output capacitance (C_{LOAD})	55 mF
Are all the loads off until the PG is asserted?	No
Load at start-up ($R_{LOAD(Startup)}$)	0.33 Ω (equivalent to approximately 12% of the maximum steady-state load)
Maximum ambient temperature	55°C
Transient overload blanking timer	16 ms
Output voltage slew rate	1.2 V/ms
Need to survive a “hot-short” on output condition ?	Yes
Need to survive a “power up into short” condition?	Yes
Can a board be hotplugged in or power cycled?	Yes
Load current monitoring needed?	Yes
Fault response	Latch-off

9.2.3 Detailed Design Procedure

- **Determining the number of eFuse devices to be used in parallel**

  By factoring in a small variation in the junction to ambient thermal resistance ($R_{θJA}$), a single TPS25985x eFuse is rated at a maximum steady state DC current of 60 A with a maximum junction temperature of less than 125°C. Therefore, Equation 22 can be used to calculate the number of devices (N) to be in parallel to support the maximum steady state DC load current ($I_{LOAD(max)}$), for which the solution must be designed.

  $$N \geq \frac{I_{OUT(max)}\,(A)}{60\ A} \tag{22}$$

  According to Table 9-1, $I_{OUT(max)}$ is 300 A. Therefore, five (5) TPS25985 eFuses are connected in parallel.
- **Setting up the primary and secondary devices in a parallel configuration**

  The MODE pin is used to configure one TPS25985x eFuse as the primary device in a parallel chain along with the other TPS25985x eFuses as the secondary devices. As a result, some of the TPS25985 pin functionalities can be changed to facilitate primary and secondary configuration as described in *Multiple Devices, Parallel Connection*.

  Leaving the pin open configures the corresponding device as the primary one. For the secondary devices, this pin must be connected to GND.
- **Selecting the C_{DVDT} capacitor to control the output slew rate and start-up time**

  For a robust design, the junction temperature of the device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Typically, dynamic power stresses are orders of magnitude greater than static stresses, so it is crucial to establish the right start-up time and inrush current limit for the capacitance in the system and the associated loads to avoid thermal shutdown during start-up.

Table 9-2 summarizes the formulas for calculating the average inrush power loss on the eFuses in the presence of different loads during start-up if the power-good (PG) signal is not used to turn on all the downstream loads.

Table 9-2. Calculation of Average Power Loss During Inrush

Type of Loads During Start-Up	Expressions to Calculate the Average Inrush Power Loss
Only output capacitor of C_{LOAD} (µF)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{SS}}$ (23)
Output capacitor of C_{LOAD} (µF) and constant resistance of $R_{LOAD(Startup)}$ (Ω) with turn-ON threshold of V_{RTH} (V)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{SS}} + \frac{V_{IN}^2}{R_{LOAD(Startup)}}\left[\frac{1}{6} - \left\{\frac{1}{2}\left(\frac{V_{RTH}}{V_{IN}}\right)^2\right\} + \left\{\frac{1}{3}\left(\frac{V_{RTH}}{V_{IN}}\right)^3\right\}\right]$ (24)
Output capacitor of C_{LOAD} (µF) and constant current of $I_{LOAD(Startup)}$ (A) with turn-ON threshold of V_{CTH} (V)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{SS}} + V_{IN} I_{LOAD(Startup)}\left[\frac{1}{2} - \left(\frac{V_{CTH}}{V_{IN}}\right) + \left\{\frac{1}{2}\left(\frac{V_{CTH}}{V_{IN}}\right)^2\right\}\right]$ (25)
Output capacitor of C_{LOAD} (µF) and constant power of $P_{LOAD(Startup)}$ (W) with turn-ON threshold of V_{PTH} (V)	$\frac{V_{IN}^2 C_{LOAD}}{2T_{SS}} + P_{LOAD(Startup)}\left[\ln\left(\frac{V_{PTH}}{V_{IN}}\right) + \left(\frac{V_{PTH}}{V_{IN}}\right) - 1\right]$ (26)

Where V_{IN} is the input voltage and T_{ss} is the start-up time.

With the different combinations of loads during start-up, the total average inrush power loss (P_{INRUSH}) can be calculated using the formulas described in Table 9-2. For a successful start-up, the system must satisfy the condition stated in Equation 27.

$$P_{INRUSH}(W)\sqrt{T_{SS}(s)} < 12 \times N \tag{27}$$

Where N denotes the number of eFuses in parallel and 12 W√s is the SOA limit of a single TPS25985x eFuse. This equation can be used to obtain the maximum allowed T_{ss}.

Note

TI recommends to use a T_{ss} in the range of 5 ms to 120 ms to prevent start-up issues.

A capacitor (C_{DVDT}) must be added at the DVDT pin to GND to set the required value of T_{ss} as calculated above. Equation 28 is used to compute the value of C_{DVDT}. The DVDT pins of all the eFuses in a parallel chain must be connected together.

$$C_{DVDT}(pF) = \frac{42000}{V_{IN}(V)/T_{SS}(ms)} \tag{28}$$

In this design example, C_{LOAD} = 55 mF, $R_{LOAD(Startup)}$ = 0.33 Ω, V_{RTH} = 0 V, V_{IN} = 12 V, and T_{ss} = 10 ms. P_{INRUSH} is calculated to be 469 W using the equations provided in the Table 9-2. It is verified that the system satisfies condition state in Equation 27 and therefore capable of having a successful start-up. If Equation 27 does not hold true, start-up loads or T_{ss} must be tuned to prevent chances of thermal shutdown during start-up. Using V_{IN} = 12 V, T_{ss} = 10 ms and Equation 28, the required C_{DVDT} value can be calculated to be 35 nF. The closest standard value of C_{DVDT} is 33 nF with 10% tolerance and DC voltage rating of 25 V.

Note

In some systems, there can be active load circuits (for example, DC-DC converters) with low turn-on threshold voltages which can start drawing power before the eFuse has completed the inrush sequence. This action can cause additional power dissipation inside the eFuse during start-up and can lead to thermal shutdown. TI recommends using the Power Good (PG) pin of the eFuse to enable and disable the load circuit. This action ensures that the load is turned on only when the eFuse has completed its start-up and is ready to deliver full power without the risk of hitting thermal shutdown.

- **Selecting the R_{IREF} resistor to set the reference voltage for overcurrent protection and active current sharing**

  In this parallel configuration, the IREF internal current source (I_{IREF}) of the primary eFuse interacts with the external IREF pin resistor (R_{IREF}) to generate the reference voltage (V_{IREF}) for the overcurrent protection and active current sharing blocks. When the voltage at the IMON pin (V_{IMON}) is used as an input to an ADC to monitor the system current or to implement the Platform Power Control (Intel PSYS) functionality inside the VR controller, V_{IREF} must be set to half of the maximum voltage range of the ISYS_IN input of the controller. This action provides the necessary headroom and dynamic range for the system to accurately monitor the load current up to the fast-trip threshold (2 × I_{OCP}). Equation 29 is used to calculate the value of R_{IREF}.

  $$V_{IREF} = I_{IREF} \times R_{IREF} \tag{29}$$

  In this design example, V_{IREF} is set at 1 V. With I_{IREF} = 25 μA (typical), we can calculate the target R_{IREF} to be 40 kΩ. The closest standard value of R_{IREF} is 40.2 kΩ with 0.1% tolerance and power rating of 100 mW. For improved noise immunity, place a 1-nF ceramic capacitor from the IREF pin to GND.

Note

Maintain V_{IREF} within the recommended voltage to ensure proper operation of overcurrent detection circuit.

- **Selecting the R_{IMON} resistor to set the overcurrent (circuit-breaker) and fast-trip thresholds during steady-state**

  TPS25985x eFuse responds to the output overcurrent conditions during steady-state by turning off the output after a user-adjustable transient fault blanking interval. This eFuse continuously senses the total system current (I_{OUT}) and produces a proportional analog current output (I_{IMON}) on the IMON pin. This generates a voltage (V_{IMON}) across the IMON pin resistor (R_{IMON}) in response to the load current, which is defined as Equation 30.

  $$V_{IMON} = I_{OUT} \times G_{IMON} \times R_{IMON} \tag{30}$$

  G_{IMON} is the current monitor gain (I_{IMON} : I_{OUT}), whose typical value is 18.18 μA/A. The overcurrent condition is detected by comparing the V_{IMON} against the V_{IREF} as a threshold. The circuit-breaker threshold during steady-state (I_{OCP}) can be calculated using Equation 31.

  $$I_{OCP(TOTAL)} = \frac{V_{IREF}}{G_{IMON} \times R_{IMON}} \tag{31}$$

  In this design example, $I_{OCP(TOTAL)}$ is considered to be 1.1 times $I_{OUT(max)}$. Hence, $I_{OCP(TOTAL)}$ is set at 330 A, and R_{IMON} can be calculated to be 166.67 Ω with G_{IMON} as 18.19 μA/A and V_{IREF} as 1 V. The nearest value of R_{IMON} is 167 Ω with 0.1% tolerance and power rating of 100 mW. For noise reduction, place a 22-pF ceramic capacitor across the IMON pin and GND.

Note

A system output current (I_{OUT}) must be considered when selecting R_{IMON}, not the current carried by each device.

- **Selecting the R_{ILIM} resistor to set the current limit and fast-trip thresholds during start-up and the active sharing threshold during steady-state**

  R_{ILIM} is used in setting up the active current sharing threshold during steady-state and the overcurrent limit during startup among the devices in a parallel chain. Each device continuously monitors the current flowing through it (I_{DEVICE}) and outputs a proportional analog output current on its own ILIM pin. This in turn produces a proportional voltage (V_{ILIM}) across the respective ILIM pin resistor (R_{ILIM}), which is expressed as Equation 32.

  $$V_{ILIM} = I_{DEVICE} \times G_{ILIM} \times R_{ILIM} \tag{32}$$

  G_{ILIM} is the current monitor gain (I_{ILIM} : I_{DEVICE}), whose typical value is 18.18 µA/A.

  – ***Active current sharing during steady-state***: This mechanism operates only after the device reaches steady-state and acts independently by comparing its own load current information (V_{ILIM}) with the Active Current Sharing reference ($CLREF_{LIN}$) threshold, defined as Equation 33.

  $$CLREF_{LIN} = \frac{1.1 \times V_{IREF}}{3} \tag{33}$$

  Therefore, R_{ILIM} must be calculated using Equation 34 to define the active current sharing threshold as $I_{OCP(TOTAL)}$/N, where N is the number of devices in parallel. Using N = 5, R_{IMON} = 167 Ω, and Equation 34, R_{ILIM} can be calculated to be 306.2 Ω. The closest standard value of 300 Ω with 0.1% tolerance and power rating of 100 mW resistances are selected as R_{ILIM} for each device.

  $$R_{ILIM} = \frac{1.1 \times N \times R_{IMON}}{3} \tag{34}$$

  Note

  To determine the value of R_{ILIM}, Equation 35 must be used if a different threshold for active current sharing ($I_{LIM(ACS)}$) than I_{OCP}/N is desired.

  $$R_{ILIM} = \frac{1.1 \times V_{IREF}}{3 \times G_{ILIM} \times I_{LIM(ACS)}} \tag{35}$$

  When computing the current limit threshold during start-up in the next sub-section, ensure to use this R_{ILIM} value.

  – ***Overcurrent limit during start-up***: During inrush, the overcurrent condition for each device is detected by comparing its own load current information (V_{ILIM}) with a scaled reference voltage as depicted in Equation 36.

  $$CLREF_{SAT} = \frac{0.7 \times V_{IREF}}{3} \tag{36}$$

  The current limit threshold during start-up can be calculated using Equation 37.

  $$I_{ILIM(Startup)} = \frac{CLREF_{SAT}}{G_{ILIM} \times R_{ILIM}} \tag{37}$$

  By using a R_{ILIM} value of 300 Ω for each device, the start-up current is limited to ~43 A for each device and the $I_{LIM(ACS)}$ is set at ~67 A.

  Note

  The active current limit block employs a foldback mechanism during start-up based on V_{OUT}. When V_{OUT} is below the foldback threshold (V_{FB}) of 1.99 V, the current limit threshold is further lowered.

- **Selecting the C_{ITIMER} capacitor to set the overcurrent blanking timer**

  An appropriate capacitor must be connected at the ITIMER pin to ground of the primary or standalone device to adjust the duration for which the load transients above the circuit-breaker threshold are allowed. The transient overcurrent blanking interval can be calculated using Equation 38.

$$t_{ITIMER}(ms) = \frac{C_{ITIMER}(nF) \times \Delta V_{ITIMER}(V)}{I_{ITIMER}(\mu A)} \tag{38}$$

Where t_{ITIMER} is the transient overcurrent blanking timer and C_{ITIMER} is the capacitor connected between ITIMER pin of the primary device and GND. I_{ITIMER} = 2.07 µA (typical) and ΔV_{ITIMER} = 1.5 V (typical). A 22-nF capacitor with 10% tolerance and DC voltage rating of 25 V is used as the C_{ITIMER} for the primary device in this design, which results in 16.5 ms of t_{ITIMER}. The ITIMER pin for all the secondary devices should be left open.

- **Selecting the resistors to set the undervoltage lockout threshold**

  The undervoltage lockout (UVLO) threshold is adjusted by employing the external voltage divider network of R_1 and R_2 connected between IN, EN/UVLO, and GND pins of the device as described in Undervoltage protection section. The resistor values required for setting up the UVLO threshold are calculated using Equation 39.

$$V_{IN(UV)} = V_{UVLO(R)} \frac{R_1 + R_2}{R_2} \tag{39}$$

  To minimize the input current drawn from the power supply, TI recommends using higher resistance values for R_1 and R_2. The current drawn by R_1 and R_2 from the power supply is $I_{R12} = V_{IN} / (R_1 + R_2)$. However, the leakage currents due to external active components connected to the resistor string can add errors to these calculations. So, the resistor string current, I_{R12} must be 20 times greater than the leakage current at the EN/UVLO pin (I_{ENLKG}). From the device electrical specifications, I_{ENLKG} is 0.1 µA (maximum) and UVLO rising threshold $V_{UVLO(R)}$ = 1.2 V. From the design requirements, V_{INUVLO} = 10.8 V. First choose the value of R_1 = 1 MΩ and use Equation 39 to calculate R_2 = 125 kΩ. Use the closest standard 1 % resistor values: R_1 = 1 MΩ and R_2 = 124 kΩ. For noise reduction, place a 1-nF ceramic capacitor across the EN/UVLO pin and GND.

- **Selecting the R-C filter between VIN and VDD**

  VDD pin is intended to power the internal control circuitry of the eFuse with a filtered and stable supply, not affected by system transients. Therefore, use an R (10 Ω) – C (2.2 µF) filter from the input supply (IN pin) to the VDD pin. This helps to filter out the supply noises and to hold up the controller supply during severe faults such as short-circuit at the output. In a parallel chain, this R-C filter must be employed for each device.

- **Selecting the pullup resistors and power supplies for SWEN, PG, $\overline{\text{FLT}}$, and CMPOUT pins**

  $\overline{\text{FLT}}$, PG, and CMPOUT are the open drain outputs. If these logic signals are used, the corresponding pins must be pulled up to an appropriate supply rail voltage through 10-kΩ pullup resistances.

> SWEN pin must be pulled up to a voltage in the range of 2.5 V to 5 V through a 100-kΩ resistance. This pullup power supply must be generated from the input (VIN) to the eFuse and available before the eFuse is enabled, without which the eFuse cannot start up.

- **Selection of TVS diode at input and Schottky diode at output**

  In the case of a short circuit and overload current limit when the device interrupts a large amount of current instantaneously, the input inductance generates a positive voltage spike on the input, whereas the output inductance creates a negative voltage spike on the output. The peak amplitudes of these voltage spikes (transients) are dependent on the value of inductance in series with the input or output of the device. Such transients can exceed the absolute maximum ratings of the device and eventually lead to failures due to electrical overstress (EOS) if appropriate steps are not taken to address this issue. Typical methods for addressing this issue include:

  1. Minimize lead length and inductance into and out of the device.
  2. Use a large PCB GND plane.
  3. Addition of the Transient Voltage Suppressor (TVS) diodes to clamp the positive transient spike at the input.
  4. Using Schottky diodes across the output to absorb negative spikes.

Refer to *TVS Clamping in Hot-Swap Circuits* and *Selecting TVS Diodes in Hot-Swap and ORing Applications* for details on selecting an appropriate TVS diode and the number of TVS diodes to be in parallel to effectively clamp the positive transients at the input below the absolute maximum ratings of the IN pin (20 V). These TVS diodes also help to limit the transient voltage at the IN pin during the Hot Plug event. Four (4) SMDJ12A are used in parallel in this design example.

Note

Maximum Clamping Voltage V_C specification of the selected TVS diode at I_{pp} (10/1000 µs) (V) must be lower than the absolute maximum rating of the power input (IN) pin for safe operation of the eFuse.

Selection of the Schottky diodes must be based on the following criteria:

- The non-repetitive peak forward surge current (I_{FSM}) of the selected diode must be more than the fast-trip threshold (2 × $I_{OCP(TOTAL)}$). Two or more Schottky diodes in parallel must be used if a single Schottky diode is unable to meet the required I_{FSM} rating. Equation 40 calculates the number of Schottky diodes ($N_{Schottky}$) that must be in parallel.

$$N_{Schottky} > \frac{2 \times I_{OCP(TOTAL)}}{I_{FSM}} \tag{40}$$

- Forward Voltage Drop (V_F) at near to I_{FSM} must be as small as possible. Ideally, the negative transient voltage at the OUT pin must be clamped within the absolute maximum rating of the OUT pin (–1 V).
- DC Blocking Voltage (V_{RM}) must be more than the maximum input operating voltage.
- Leakage current (I_R) must be as small as possible.

Three (3) SBR10U45SP5 are used in parallel in this design example.

- **Selecting C_{IN} and C_{OUT}**

TI recommends to add ceramic bypass capacitors to help stabilize the voltages on the input and output. The value of C_{IN} must be kept small to minimize the current spike during hot-plug events. For each device, 0.1 µF of C_{IN} is a reasonable target. Because C_{OUT} does not get charged during hot-plug, a larger value such as 2.2 µF can be used at the OUT pin of each device.

9.2.4 Application Performance Plots

All the waveforms below are captured on an evaluation setup with five (5) TPS25985 eFuses in parallel. All the pullup supplies are derived from a separate standby rail.

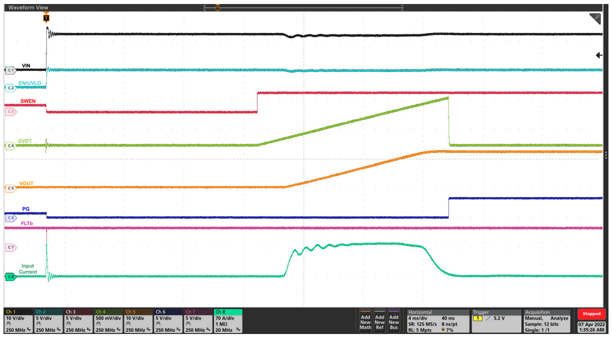


Figure 9-4. Input Hot Plug: V_{IN} Stepped Up from 0 V to 12 V, C_{LOAD} = 55 mF, C_{DVDT} = 33 nF, R_{IREF} = 40.2 kΩ, and R_{ILIM} on Each Device = 300 Ω

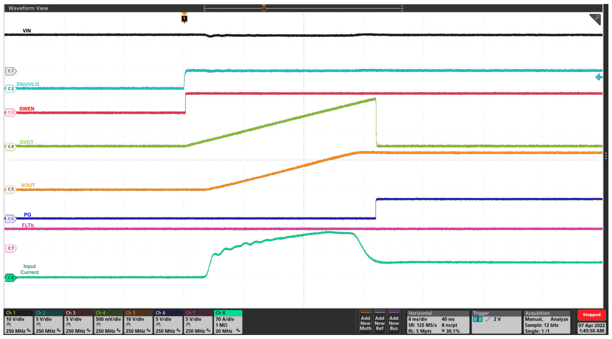


Figure 9-5. Start-up with EN/UVLO: V_{IN} = 12 V, EN/UVLO Stepped Up From 0 V to 3 V, C_{LOAD} = 55 mF, $R_{LOAD(Start-up)}$ = 0.33 Ω, C_{DVDT} = 33 nF, R_{IREF} = 40.2 kΩ, and R_{ILIM} on Each Device = 300 Ω

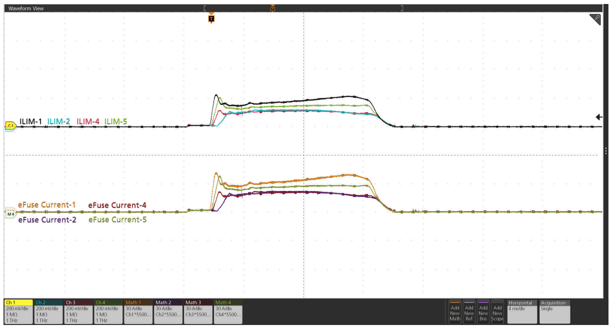


Figure 9-6. Start-up with EN/UVLO (Current distribution among five devices in parallel): V_{IN} = 12 V, EN/UVLO Stepped Up From 0 V to 3 V, C_{LOAD} = 55 mF, C_{DVDT} = 33 nF, R_{IREF} = 40.2 kΩ, and R_{ILIM} on Each Device = 300 Ω

Figure 9-7. Power Up into Short: V_{IN} = 12 V, EN/UVLO Stepped Up From 0 V to 3 V, R_{IREF} = 40.2 kΩ, R_{ILIM} on Each Device = 300 Ω, and OUT Shorted to GND

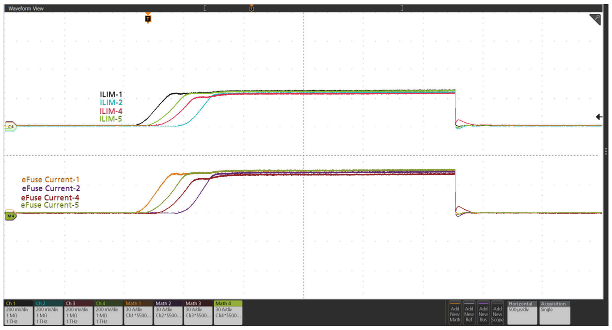


Figure 9-8. Power Up into Short (Current distribution among five devices in parallel): V_{IN} = 12 V, EN/UVLO Stepped Up From 0 V to 3 V, R_{IREF} = 40.2 kΩ, R_{ILIM} on Each Device = 300 Ω, and OUT Shorted to GND

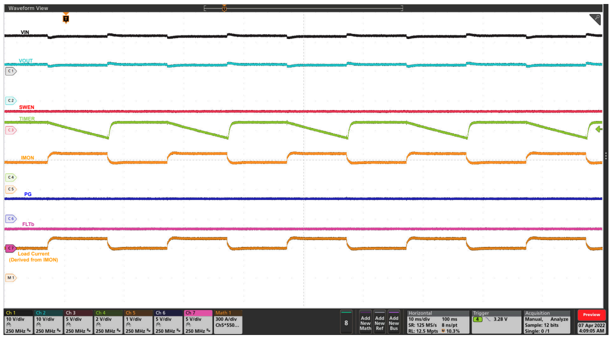


Figure 9-9. Transient Overload: V_{IN} = 12 V, C_{ITIMER} = 22 nF, C_{LOAD} = 55 mF, R_{IMON} = 167 Ω, R_{IREF} = 40.2 kΩ, and Load Current Stepped from 300 A to 400 A then 300 A within 10 ms

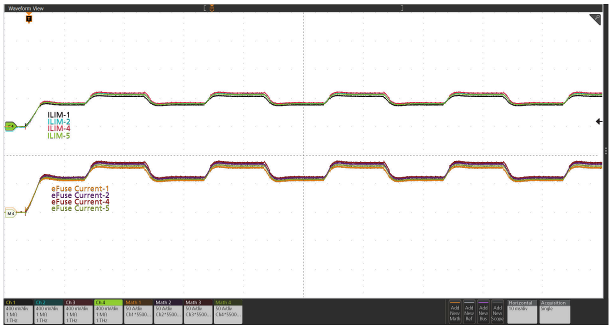


Figure 9-10. Transient Overload (Current distribution among five devices in parallel): V_{IN} = 12 V, C_{ITIMER} = 22 nF, C_{LOAD} = 55 mF, R_{IMON} = 167 Ω, R_{IREF} = 40.2 kΩ, and Load Current Stepped from 300 A to 450 A then 300 A within 8.5 ms

Figure 9-11. Circuit-Breaker Response: V_{IN} = 12 V, C_{ITIMER} = 22 nF, C_{LOAD} = 55 mF, R_{IMON} = 167 Ω, R_{IREF} = 40.2 kΩ, and Load Current Stepped up From 300 A to 500 A for > 20 ms

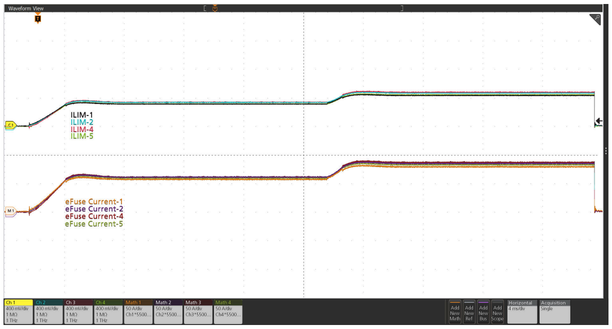


Figure 9-12. Circuit-Breaker Response (Current distribution among five devices in parallel): V_{IN} = 12 V, C_{ITIMER} = 22 nF, C_{LOAD} = 55 mF, R_{IMON} = 167 Ω, R_{IREF} = 40.2 kΩ, and Load Current Stepped up From 300 A to 475 A for > 20 ms

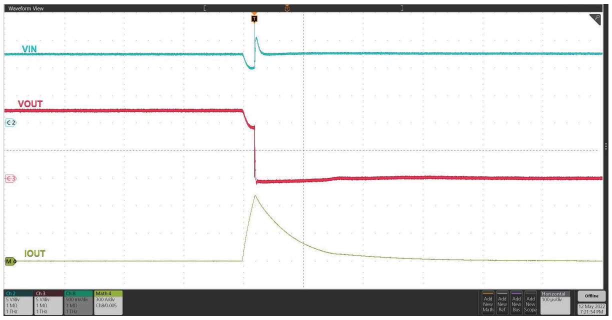


Figure 9-13. Output Hot-Short Response: V_{IN} = 12 V, R_{IMON} = 167 Ω, R_{IREF} = 40.2 kΩ, and OUT Shorted to GND

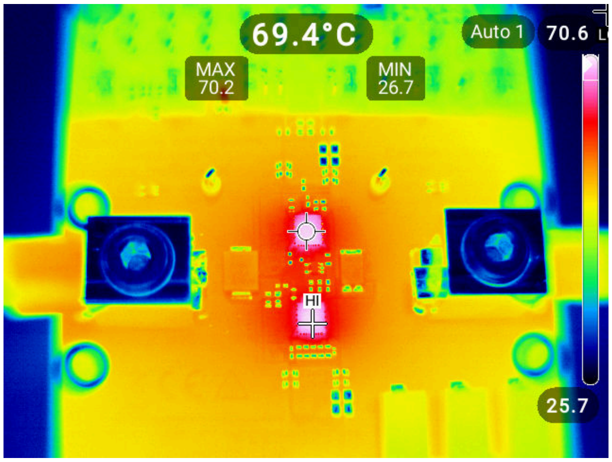


Figure 9-14. Two (2) TPS25985x eFuses in Parallel: Temperature Rise with 100-A DC Current at Room Temperature (No Air-Flow)

9.3 Multiple eFuses, Parallel Connection with PMBus®

Applications which need higher current input protection along with digital interface for telemetry, control, configurability can use one or more TPS25985x device(s) in parallel with TPS25990x as shown in Figure 9-15

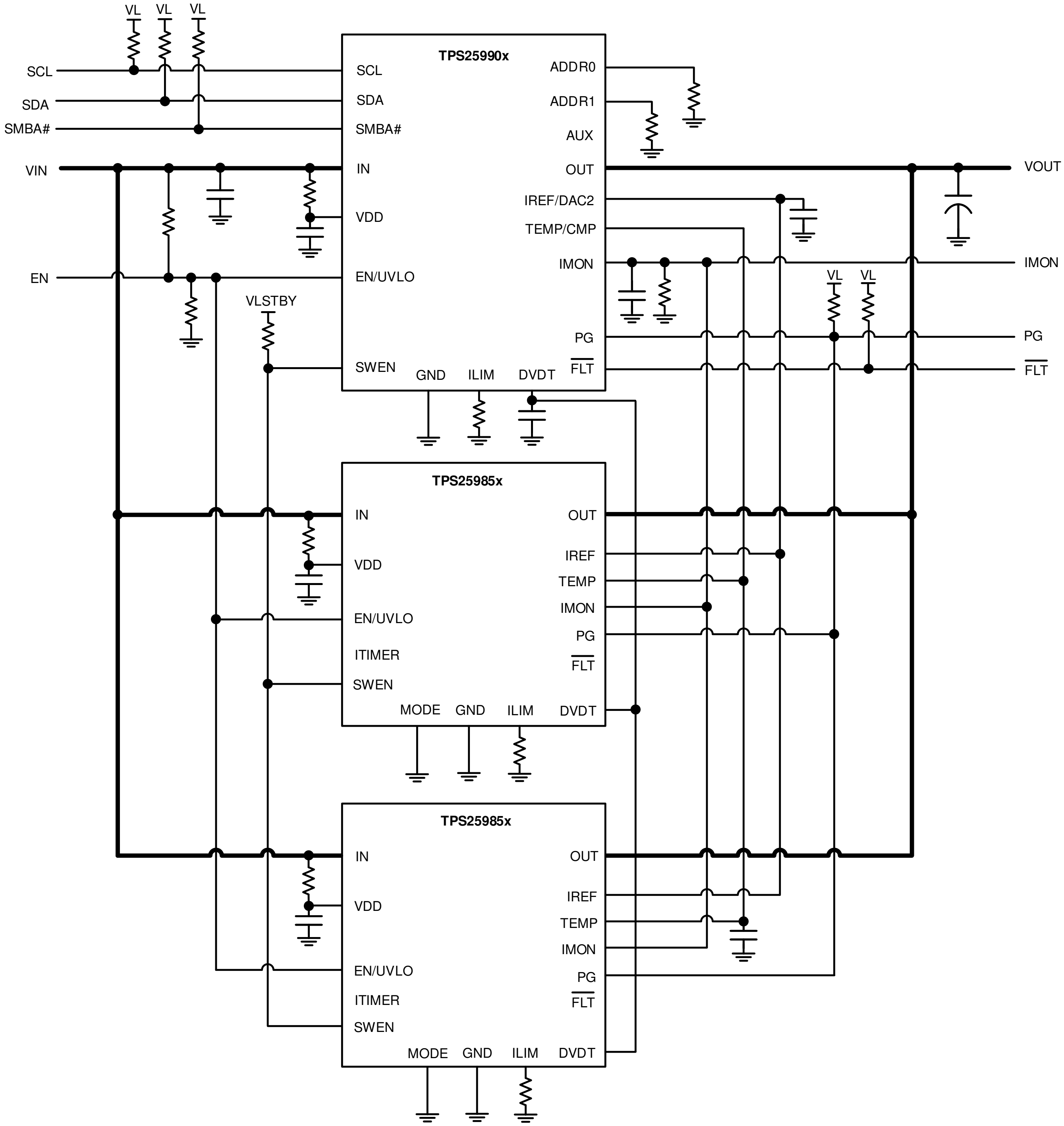


Figure 9-15. TPS25990x Connected in Parallel with TPS25985x For Higher Current Support With PMBus®

TPS25990x is a 60-A integrated eFuse with PMBus Telemetry interface.

In this configuration, the TPS25990x acts as the primary device and controls the other TPS25985x devices in the chain which are designated as secondary devices. This configuration is achieved by connecting the primary device as follows:

1. VDD is connected to IN through an R-C filter.
2. DVDT is connected through capacitor to GND.
3. IREF is connected through capacitor to GND.
4. IMON is connected through resistor to GND.
5. ILIM is connected through resistor to GND.

SWEN is pulled up to a 3.3-V to 5-V standby rail. This rail must be powered up independent of the eFuse ON/OFF status.

The secondary devices must be connected in the following manner:

1. VDD is connected to IN through a R-C filter.
2. MODE pin is connected to GND.
3. ITIMER pin is left OPEN.
4. ILIM is connected through resistor to GND.

The following pins of all devices must be connected together:

1. IN
2. OUT
3. EN/UVLO
4. DVDT
5. SWEN
6. PG
7. IMON
8. IREF
9. TEMP

In this configuration, all the devices are powered up and enabled simultaneously.

- The TPS25990x monitors the combined VIN, VOUT, IMON, TEMP and reports it over the PMBus telemetry interface.
- THE OVLO threshold is set to max value in all devices by default. For TPS25985x devices, the OV threshold is fixed in hardware and cannot be changed. The TPS25990x OV threshold can be lowered through PMBus writes to the VIN_OV_FAULT register. In this case, the TPS25990x uses the SWEN pin to turn off the TPS25985x devices during OV conditions.
- The UVLO threshold for all devices is set by the external resistor divider from IN to GND on the EN/UVLO pin. The TPS25990x UV threshold can be changed through PMBus writes to the VIN_UV_FAULT register. In this case, the TPS25990x uses the SWEN pin to turn off the TPS25985x devices during UV conditions.
- During inrush, the output of all the devices are ramped together based on the DVDT cap. However, the TPS25990x DVDT sourcing current can be configured through the PMBus to change the inrush behavior of the whole chain. The TPS25990x controls the DVDT ramp rate for the whole chain and secondary devices simply follow the ramp rate.
- Due to the inherent difference in Rdson, the current carried by the TPS25990x is lower than the TPS25985x devices. Accordingly, the start-up current limit threshold and active current sharing threshold for the TPS25990x has to be set to a relatively lower value as compared to all the TPS25985x devices by connecting a proportionately higher ILIM resistor.
- The TPS25990x controls the overall overcurrent threshold of the parallel chain by setting the VIREF threshold voltage using its internal DAC. The VIREF voltage can be programmed through PMBus to change the overcurrent threshold.
- The TPS25990x controls the transient overcurrent blanking interval (t_{OC_TIMER}) for the whole system through PMBus writes to the OC_TIMER register. After the digital timer expires, the TPS25990x pulls the SWEN pin low to signal all devices to break the circuit simultaneously.
- The system Power Good (PG) indication is a combination of all the individual device PG indications. All the devices hold their respective PG pins low till their power FET is fully turned on. After all devices have reached steady-state, they release their respective PG pin pulldown and the PG signal for the whole chain is asserted high. The TPS25985x secondary devices have control over the system PG assertion only during startup. After in steady state, only the TPS25990x controls the de-assertion of the PG based on the VOUT_PGTH register setting.

- The fault indication ($\overline{\text{FLT}}$) for the whole system is provided by TPS25990x. However, each secondary device also asserts its own $\overline{\text{FLT}}$ independently.

Power up: After power up or enable, all the eFuse devices initially hold their SWEN low till the internal blocks are biased and initialized correctly. After that, each device releases its own SWEN. After all devices have released their SWEN, the combined SWEN goes high and the devices are ready to turn on their respective FETs at the same time.

Inrush: During inrush, because the DVDT pins are tied together to a single DVDT capacitor all the devices turn on the output with the same slew rate (SR). Choose the common DVDT capacitor (C_{DVDT}) as per Equation 41 and Equation 42.

$$SR\left(\frac{V}{ms}\right) = \frac{I_{INRUSH}\,(mA)}{C_{OUT}\,(\mu F)} \tag{41}$$

$$C_{dVdt}\,(pF) = \frac{42000\ \times\ k}{SR\left(\frac{V}{ms}\right)} \tag{42}$$

Refer to *TPS25990x* for more details.

The internal balancing circuits ensure that the load current is shared among all devices during start-up. This action prevents a situation where some devices turn on faster than others and experience more thermal stress as compared to other devices. This can potentially result in premature or partial shutdown of the parallel chain, or even SOA damage to the devices. The current balancing scheme ensures the inrush capability of the chain scales according to the number of devices connected in parallel, thereby ensuring successful start-up with larger output capacitances or higher loading during start-up. All devices hold their respective PG signals low during start-up. After the output ramps up fully and reaches steady-state, each device releases its own PG pulldown. Because the DVDT pins of all devices are tied together, the internal gate high detection of all devices is synchronized. There can be some threshold or timing mismatches between devices leading to PG assertion in a staggered manner. However, because the PG pins of all devices are tied together, the combined PG signal becomes high only after all devices have released their PG pulldown. This signals the downstream load that it is okay to draw power.

Steady-state: During steady-state, all devices share current nearly equally using the active current sharing mechanism which actively regulates the respective device RDSON to evenly distribute current across all the devices in the parallel chain. After PG is asserted, de-assertion is controlled only by TPS25990x and based on VOUT_PGTH register setting.

Note

The TPS25990x current can be slightly higher as compared to TPS25985x higher owing to its higher on-resistance. This current is fine as long as the steady-state current does not exceed the recommended maximum continuous rating for the device.

Overcurrent during steady-state: The circuit-breaker threshold for the parallel chain is based on the total system current rather than the current flowing through individual devices. This is done by connecting the IMON pins of all the devices together to a single resistor (R_{IMON}) to GND. Similarly, the IREF pins of all devices are tied together and TPS25990x uses internal programmable DAC (VIREF) to generate a common reference for the overcurrent protection block in all the devices. This action helps minimize the contribution of V_{IREF} variation to the overall mismatch in overcurrent threshold between devices.

In this case, choose the R_{IMON} as per the following Equation 16:

$$R_{IMON} = \frac{V_{IREF}}{G_{IMON} \times I_{OCP(TOTAL)}} \tag{43}$$

The start-up current limit and active current sharing threshold for each device is set independently using the ILIM pin. The R_{ILIM} value for the TPS25990x should be selected based on the following equation:

$$R_{ILIM}(25990) = \frac{1.1 \times (4N - 1) \times R_{IMON}}{9} \quad (44)$$

The R_{ILIM} value for each TPS25985x must be selected based on the following equation:

$$R_{ILIM}(25985) = \frac{1.1 \times (4N - 1) \times R_{IMON}}{12} \quad (45)$$

Where N = number of devices in parallel chain (1 × TPS25990x + (N - 1) × TPS25985x)

Other variations: The IREF pin can be driven from an external precision voltage reference.

During an overcurrent event, the overcurrent detection of all the devices is triggered simultaneously. This in turn triggers the overcurrent blanking timer (OC_TIMER) in TPS25990x. The TPS25990x uses the OC_TIMER expiry event as a trigger to pull the SWEN low for all the devices, thereby initiating the circuit-breaker action for the whole chain at the same time. This mechanism ensures that mismatches in the current distribution, overcurrent thresholds and OC_TIMER intervals among the devices do not degrade the accuracy of the circuit-breaker threshold of the complete parallel chain or the overcurrent blanking interval. However, the secondary devices also maintain their backup overcurrent timer and can trigger the shutdown of the whole chain if the primary device fails to do so within a certain interval.

Severe overcurrent (short-circuit): If there is a severe fault at the output (for example, output shorted to ground with a low impedance path), the current builds up rapidly to a high value and triggers the fast-trip response in each device. The devices use two thresholds for fast-trip protection – a user-adjustable threshold (I_{SFT} = 2 × I_{OCP} in steady-state or I_{SFT} = 1.5 × I_{LIM} during inrush) as well as a fixed threshold (I_{FFT} only during steady-state). After the fast-trip, the TPS25990x relies on the SC_RETRY config bit in the DEVICE_CONFIG register to determine if the whole chain enters a latched fault or performs a fast recovery by restarting in current limit manner. If it enters a latched fault, the devices remain latched off till the device is power cycled or re-enabled, or auto-retry with a delay based on the RETRY_CONFIG register setting.

9.4 Digital Telemetry Using External Microcontroller

Systems which need digital telemetry, control, and configurability along with high current eFuse functionality can use one or more TPS25985x devices in conjunction with a general purpose microcontroller as shown in Figure 9-16.

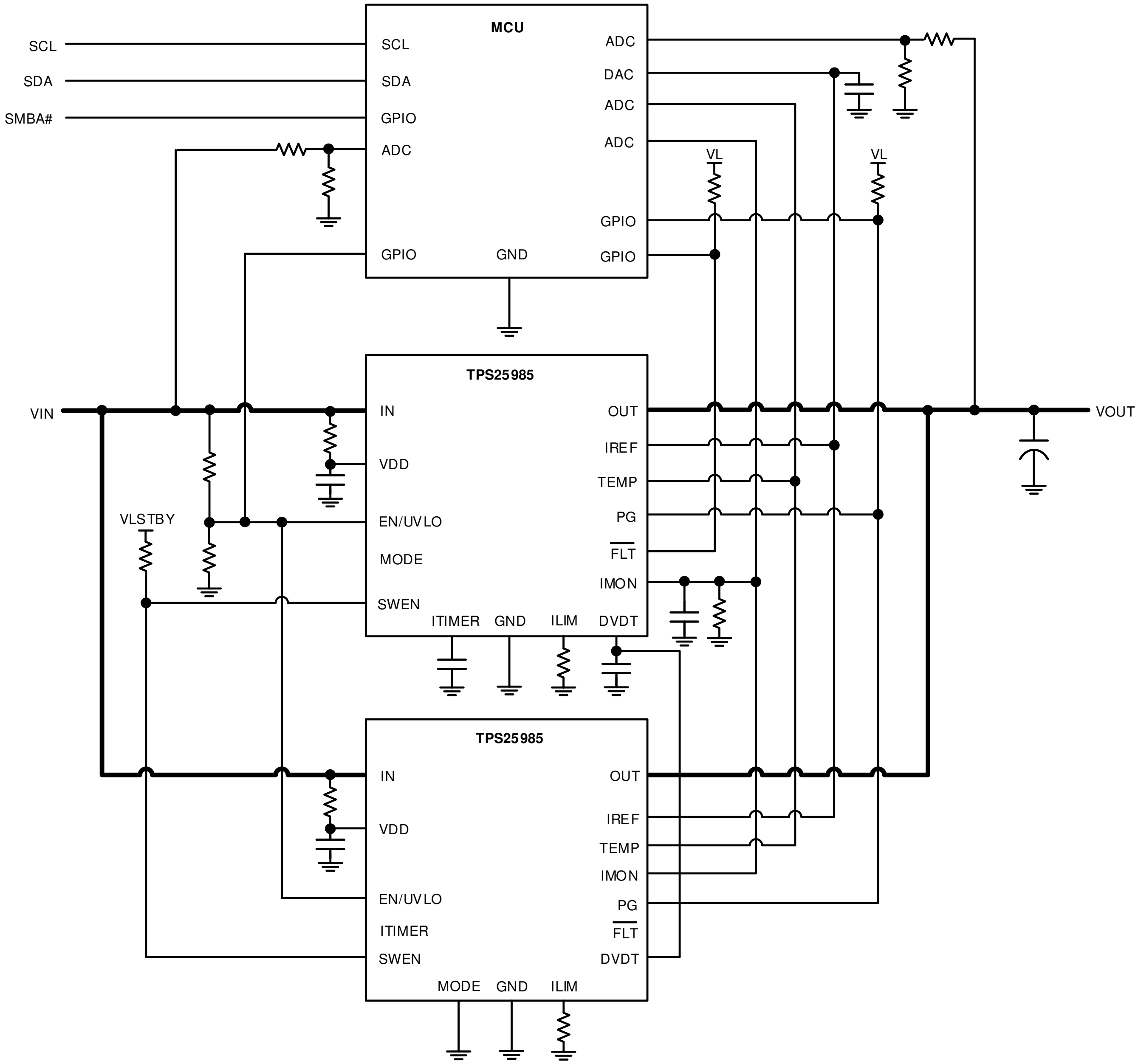


Figure 9-16. Digital Telemetry Using External Microcontroller

The basic circuit connections for the eFuses are the same for the single or multiple parallel device configuration. In addition, the following connections can be made to the microcontroller:

- IMON is connected to an ADC input of microcontroller for monitoring the load current.
- EN/UVLO is connected to GPIO of microcontroller to allow digital ON and OFF control of the eFuse.
- PG and $\overline{\text{FLT}}$ pins are connected to GPIO of microcontroller to allow digital monitoring of the eFuse status.
- VIN and VOUT rails are connected to the ADC inputs of microcontroller (through resistor ladder to appropriately step down the voltage) for monitoring the bus voltages.
- TEMP is connected to an ADC input of microcontroller for monitoring the eFuse die temperature.

- IREF can be optionally connected to a DAC output of the microcontroller to dynamically change the reference voltage for overcurrent and short-circuit current thresholds.

9.5 What to Do and What Not to Do

TPS25985x needs the SWEN pin to be pulled up to a supply rail which is powered up before the device is enabled. Failing this, the device is not able to turn on the output. The SWEN pullup supply must not be derived from the output of the eFuse. Use one of the following options to derive the pullup supply rail for SWEN.

1. Use an existing standby rail in the system, which is derived from the main power input and comes up before the eFuse is turned on.
2. Use an LDO (3.3 V or 5 V) powered from the main power input.

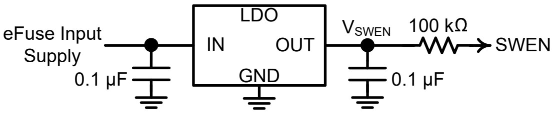


Figure 9-17. LDO Used as Pullup Supply for SWEN

3. Use a Zener regular powered from the main power input.

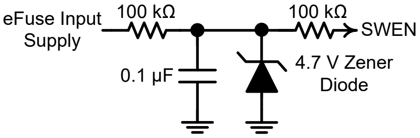


Figure 9-18. Zener Regulator Used as Pullup Supply for SWEN

4. Use the ITIMER pin of the primary eFuse. Ensure the ITIMER pin does not have excess loading which can interfere with the normal overcurrent blanking timer functionality.

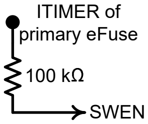


Figure 9-19. ITIMER Pin Used as Pullup Supply for SWEN

The ground connections for the various components around the TPS25985 eFuses must be wired directly to each other and the GND pins of respective eFuses. This must be followed by connecting them to the system ground at one point. For more details, refer to *TPS25985EVM eFuse Evaluation Board*. Do not connect the various component grounds through the high current system ground line.

10 Power Supply Recommendations

The TPS25985x devices are designed for a supply voltage in the range of 4.5 V to 16 V on the IN and VDD pins. TI recommends using a minimum capacitance of 0.1 µF on the IN pin of each device in parallel chain to avoid coupling of high slew rates during hot plug events. TI also recommends using an R-C filter from the input supply to the VDD pin on each device in parallel chain to filter out supply noise and to hold up the controller supply during severe faults such as short-circuit.

10.1 Transient Protection

In the case of a short-circuit or circuit-breaker event when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor of 2.2 µF or higher at the OUT pin very close to the device.
- Connect a ceramic capacitor C_{IN} = 0.1 µF or higher at the IN pin very close to the device to dampen the rise time of input transients. The capacitor voltage rating must be at least twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

The approximate value of input capacitance can be estimated with Equation 46.

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \tag{46}$$

where

V_{IN} is the nominal supply voltage.

I_{LOAD} is the load current.

L_{IN} equals the effective inductance seen looking into the source.

C_{IN} is the capacitance present at the input.

- Some applications can require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

The circuit implementation with optional protection components is shown in Figure 10-1.

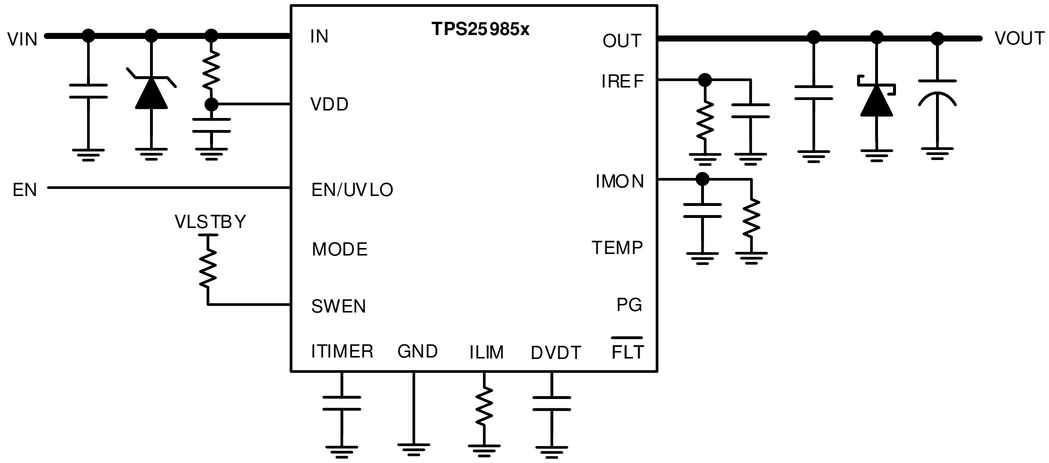


Figure 10-1. Circuit Implementation with Optional Protection Components

10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

11 Layout

11.1 Layout Guidelines

- For all applications, TI recommends a ceramic decoupling capacitor of 0.1 µF or greater between the IN terminal and GND terminal.
- For all applications, TI recommends a ceramic decoupling capacitor of 2.2 µF or greater between the OUT terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure below for a PCB layout example.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground must be a copper plane or island on the board.
- The IN and OUT pins are used for Heat Dissipation. Connect to as much copper area as possible with thermal vias.
- Locate the following support components close to their connection pins:
  - R_{ILIM}
  - R_{IMON}
  - C_{IMON}
  - R_{IREF}
  - C_{IREF}
  - C_{dVdT}
  - C_{ITIMER}
  - C_{IN}
  - C_{OUT}
  - C_{VDD}
  - Resistors for the EN/UVLO pin
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the C_{IN}, C_{OUT}, C_{VDD}, R_{IREF}, C_{IREF}, R_{ILIM}, R_{IMON}, C_{IMON}, C_{ITIMER} and C_{dVdt} components to the device must be as short as possible to reduce parasitic effects on the current limit, overcurrent blanking interval and soft-start timing. These traces must not have any coupling to switching signals on the board.
- Because the IMON, ILIM, IREF and ITIMER pins directly control the overcurrent protection behavior of the device, the PCB routing of these nodes must be kept away from any noisy (switching) signals.
- TI recommends to keep the parasitic loading on SWEN pin to a minimum to avoid synchronization issues.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, TI recommends a protection Schottky diode to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.

11.2 Layout Example

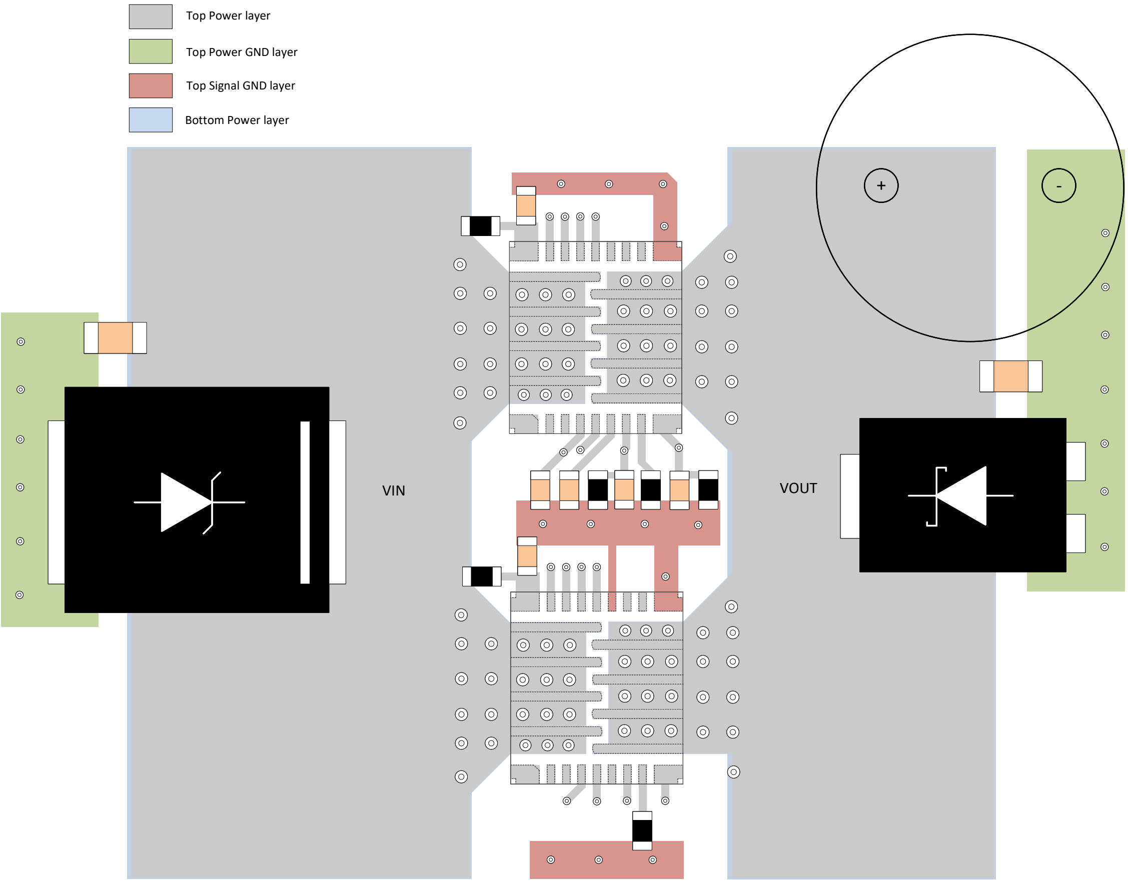


Figure 11-1. TPS25985x Two Parallel Devices Layout Example

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS25985EVM eFuse Evaluation Board*
- Texas Instruments, *TPS25985x Design Calculator*
- Texas Instruments, *TPS25990 Datasheet*

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS259850RQPR	ACTIVE	VQFN-HR	RQP	26	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TP9850 Z2	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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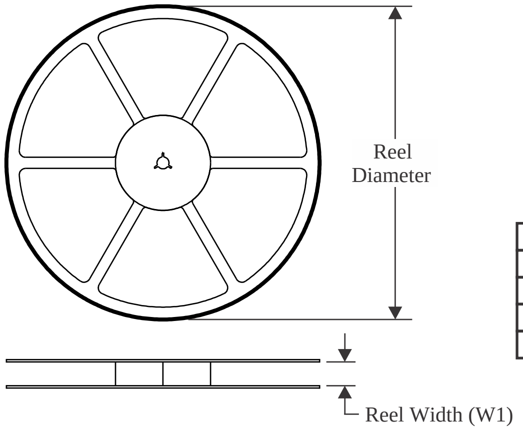
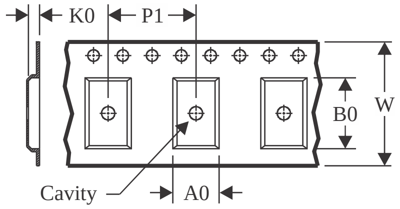
TAPE AND REEL INFORMATION

REEL DIMENSIONS

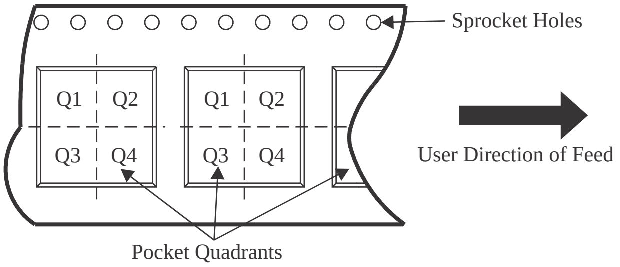


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

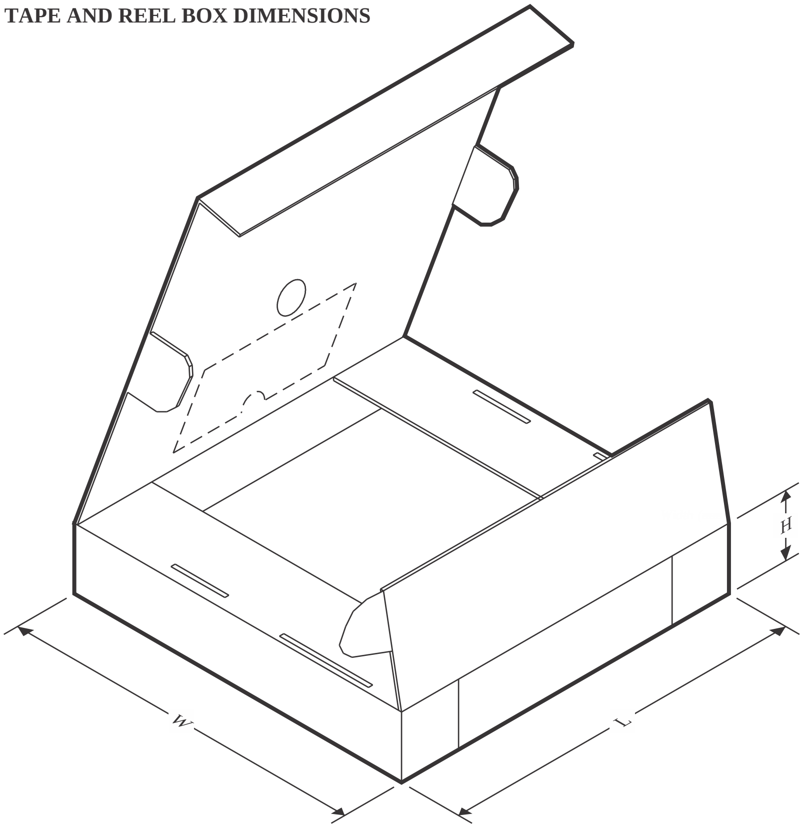
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

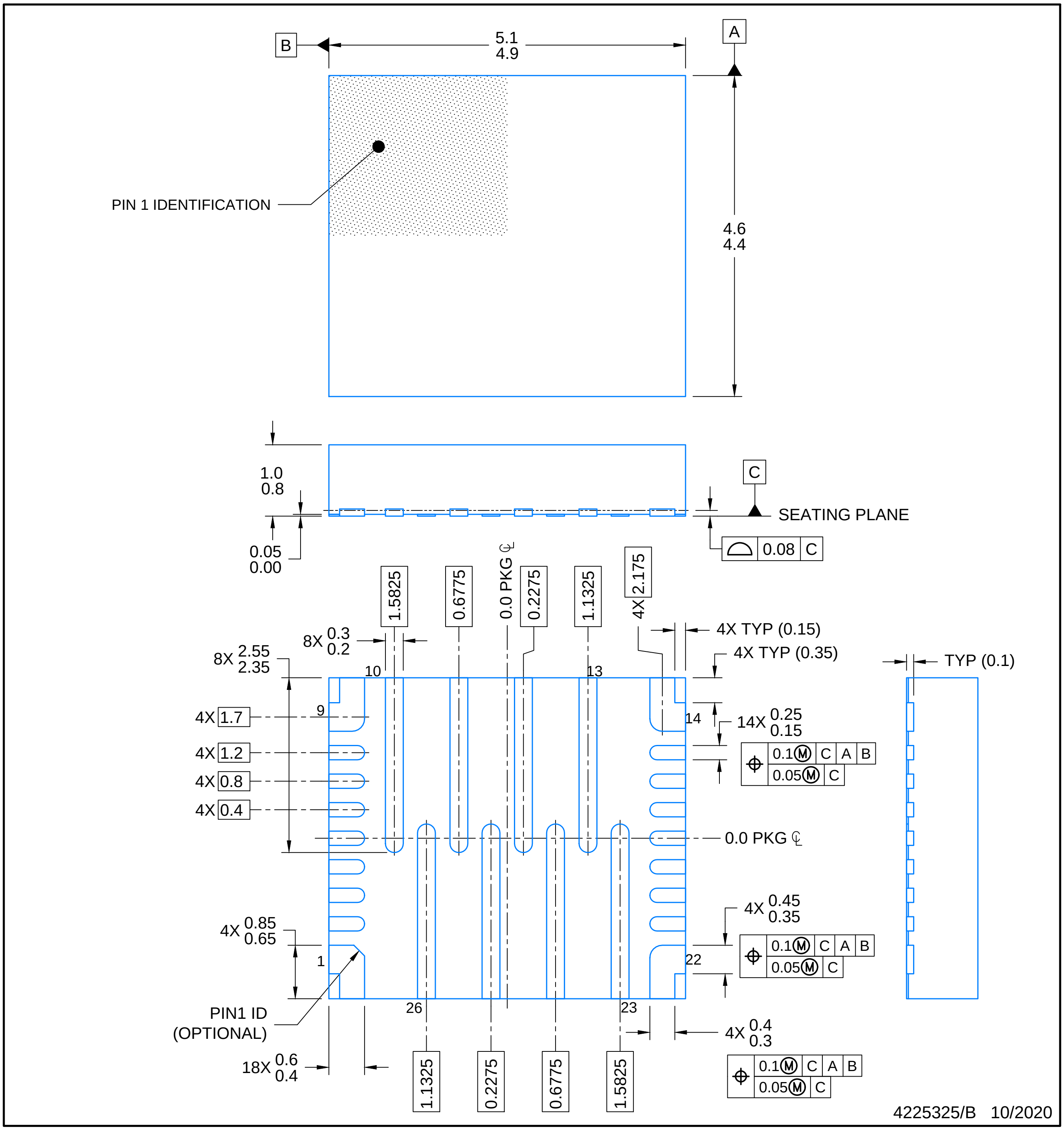
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS259850RQPR	VQFN-HR	RQP	26	3000	330.0	12.4	4.8	5.3	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



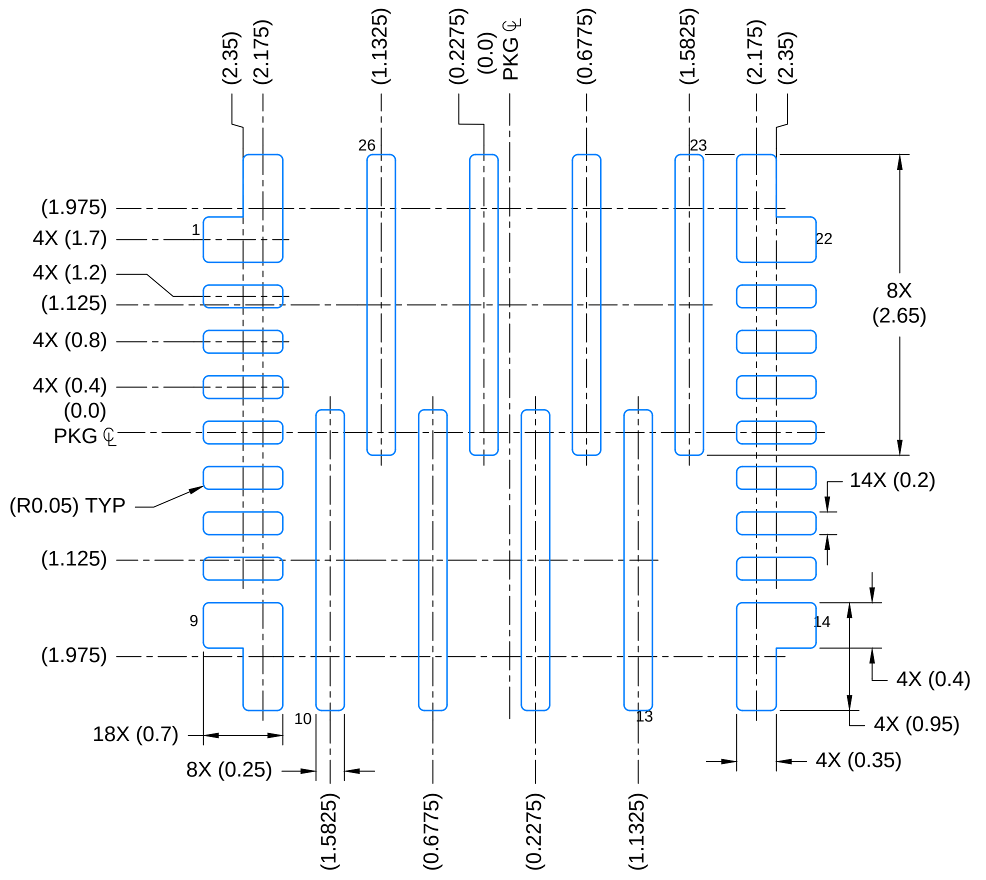
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS259850RQPR	VQFN-HR	RQP	26	3000	360.0	360.0	36.0

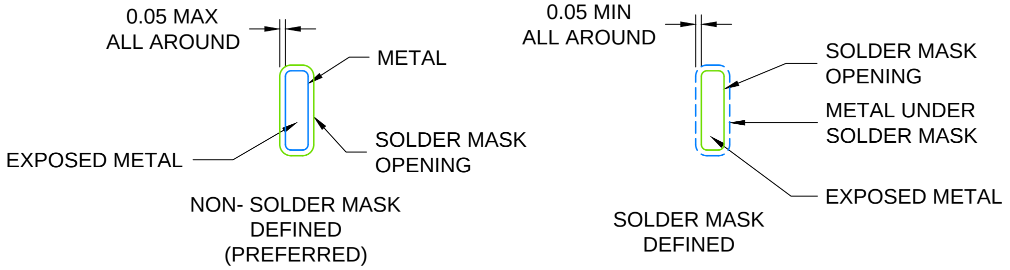


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON- SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

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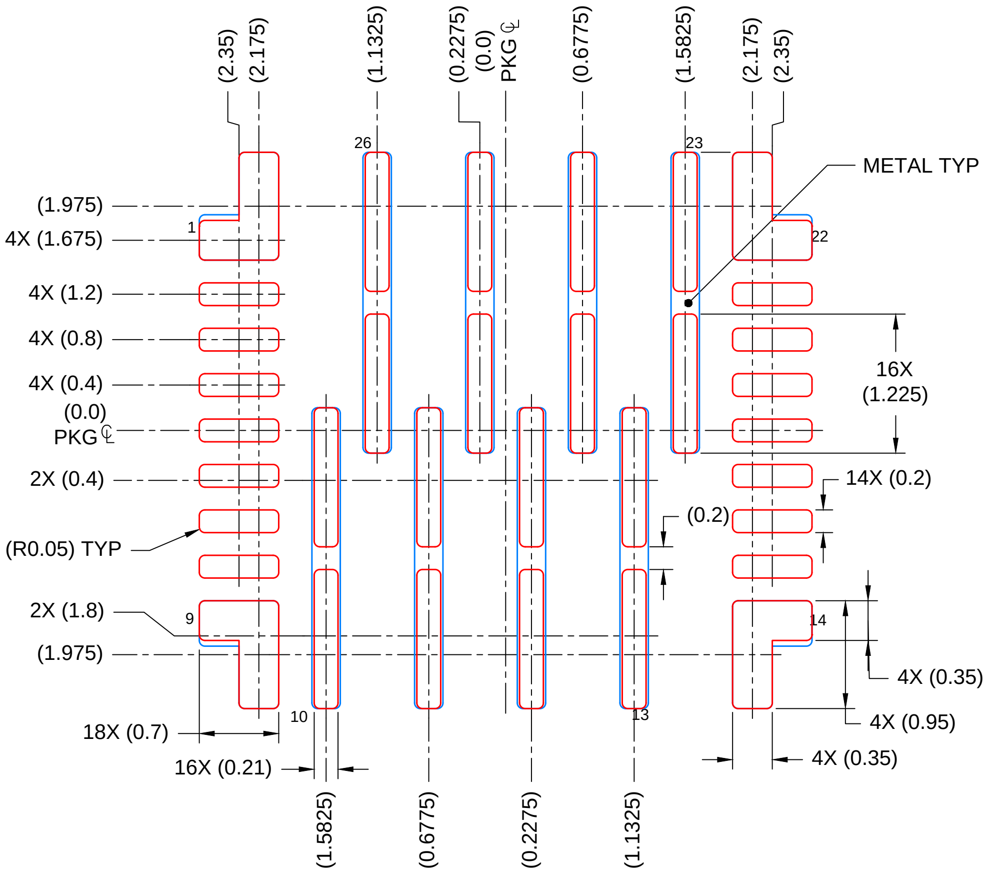
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

PIN 1,9,14 & 22: 96%; PIN 10-13 & 23-26: 77%
SCALE: 15X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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