

Motion SPM[®] 45 Series

FND43060T2

General Description

FND43060T2 is an advanced Motion SPM 45 module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, over-current shutdown, thermal monitoring, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's robust short-circuit-rated IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

Features

- UL Certified No. E209204 (UL1557)
- 600 V – 30 A 3-Phase IGBT Inverter with Integral Gate Drivers and Protection
- Low Thermal Resistance Using Ceramic Substrate
- Low-Loss, Short-Circuit Rated IGBTs
- Built-In Bootstrap Diodes and Dedicated Vs Pins Simplify PCB Layout
- Built-In NTC Thermistor for Temperature Monitoring
- Separate Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- Single-Grounded Power Supply
- Isolation Rating: 4000 V_{rms}/min
- Remove Dummy Pin

Applications

- Motion Control – Home Appliance/Industrial Motor

Related Resources

- [AN-9084](#) – Smart Power Module, Motion SPM[®] 45 H V3 Series User's Guide
- [AN-9072](#) – Smart Power Module, Motion SPM[®] in SPM45H Thermal Performance Information
- [AN-9071](#) – Smart Power Module Motion SPM[®] in SPM45H Mounting Guidance
- [AN-9760](#) – PCB Design Guidance for SPM[®]

Integrated Power Functions

- 600 V–30 A IGBT inverter for three-phase DC/AC power conversion (Refer to Figure 3)



ON Semiconductor[®]

www.onsemi.com



SPMAA-C26
CASE MODFC

Figure 1. Package Overview
(Click to Activate 3D Content)

MARKING DIAGRAM

XXXXXXXXXX
ZZZ ATYWW
NNNNNNN

XXXX = Specific Device Code
ZZZ = Lot ID
AT = Assembly and Test Location
Y = Year
WW = Work Week
NNN = Serial Number

ORDERING INFORMATION

Device	Package	Shipping
FND43060T2	SPMAA-J26	12 Units/Rail

FND43060T2

Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: gate drive circuit, high-voltage isolated high-speed level shifting control circuit Under-Voltage Lock-Out (UVLO) protection
- For inverter low-side IGBTs: gate drive circuit, Short-Circuit Protection (SCP) control supply circuit, Under-Voltage Lock-Out (UVLO) protection
- Fault signaling: corresponding to UVLO (low-side supply) and SC faults
- Input interface: active-HIGH interface, works with 3.3/5 V logic, Schmitt-trigger input

PIN CONFIGURATION

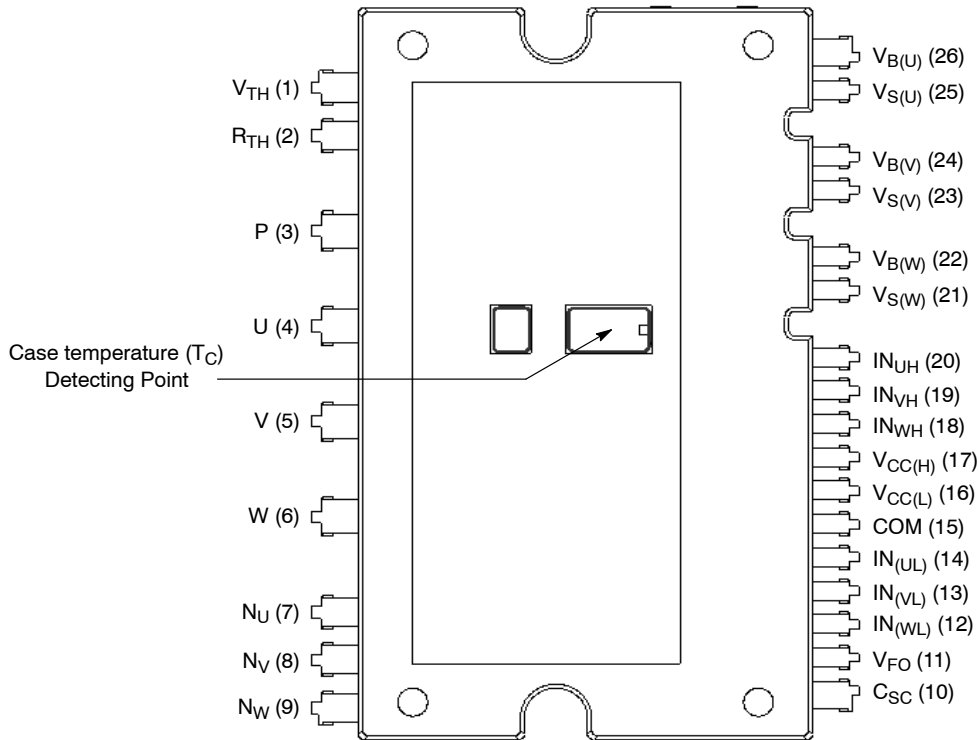


Figure 2. Top View

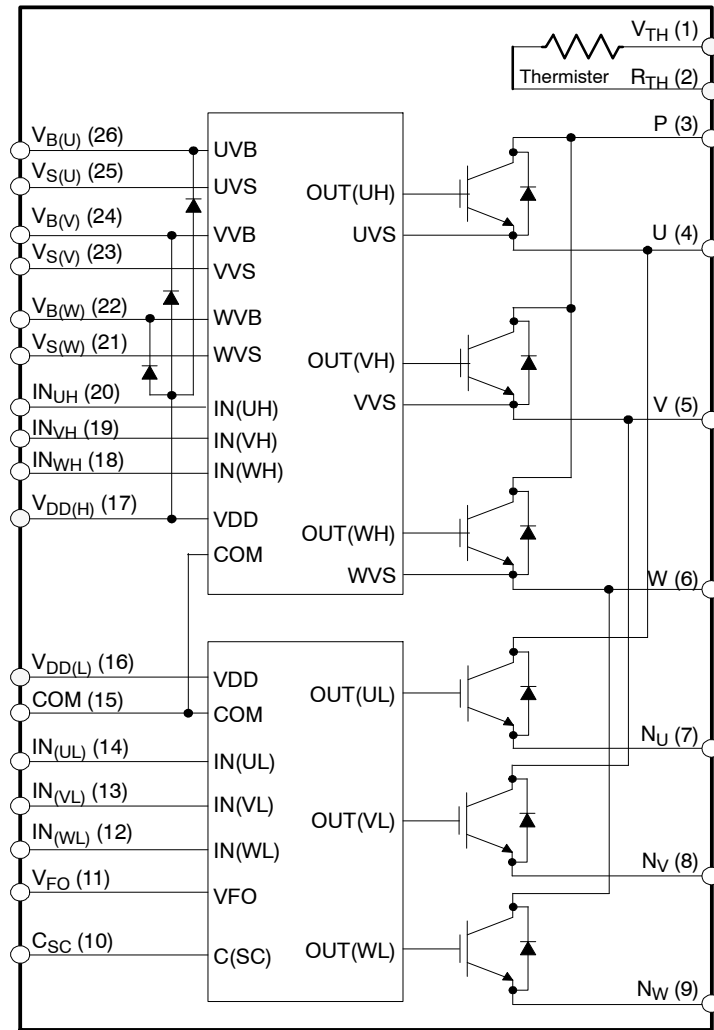
FND43060T2

PIN DESCRIPTIONS

Pin Number	Pin Name	Pin Description
1	V_{TH}	Thermistor Bias Voltage
2	R_{TH}	Series Resistor for the Use of Thermistor (Temperature Detection)
3	P	Positive DC-Link Input
4	U	Output for U-Phase
5	V	Output for V-Phase
6	W	Output for W-Phase
7	N_U	Negative DC-Link Input for U-Phase
8	N_V	Negative DC-Link Input for V-Phase
9	N_W	Negative DC-Link Input for W-Phase
10	C_{SC}	Capacitor (Low-Pass Filter) for Short-circuit Current Detection Input
11	V_{FO}	Fault Output
12	$IN_{(WL)}$	Signal Input for Low-Side W-Phase
13	$IN_{(VL)}$	Signal Input for Low-Side V-Phase
14	$IN_{(UL)}$	Signal Input for Low-Side U-Phase
15	COM	Common Supply Ground
16	$V_{DD(L)}$	Low-Side Common Bias Voltage for IC and IGBTs Driving
17	$V_{DD(H)}$	High-Side Common Bias Voltage for IC and IGBTs Driving
18	$IN_{(WH)}$	Signal Input for High-Side W-Phase
19	$IN_{(VH)}$	Signal Input for High-Side V-Phase
20	$IN_{(UH)}$	Signal Input for High-Side U-Phase
21	$V_{S(W)}$	High-Side Bias Voltage Ground for W-Phase IGBT Driving
22	$V_{B(W)}$	High-Side Bias Voltage for W-Phase IGBT Driving
23	$V_{S(V)}$	High-Side Bias Voltage Ground for V-Phase IGBT Driving
24	$V_{B(V)}$	High-Side Bias Voltage for V-Phase IGBT Driving
25	$V_{S(U)}$	High-Side Bias Voltage Ground for U-Phase IGBT Driving
26	$V_{B(U)}$	High-Side Bias Voltage for U-Phase IGBT Driving

FND43060T2

INTERNAL EQUIVALENT CIRCUIT AND INPUT/OUTPUT PINS



NOTES:

1. Inverter high-side is composed of three IGBTs, freewheeling diodes, and one control IC for each IGBT.
2. Inverter low-side is composed of three IGBTs, freewheeling diodes, and one control IC for each IGBT. It has gate drive and protection functions.
3. Inverter power side is composed of four inverter DC-link input terminals and three inverter output terminals.

Figure 3. Internal Block Diagram

FND43060T2

ABSOLUTE MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Rating	Unit
INVERTER PART				
V_{PN}	Supply Voltage	Applied between P-N _U , N _V , N _W	450	V
$V_{PN(\text{Surge})}$	Supply Voltage (Surge)	Applied between P-N _U , N _V , N _W	500	V
V_{CES}	Collector-Emitter Voltage		600	V
$\pm I_C$	Each IGBT Collector Current	$T_C = 25^\circ\text{C}$, $T_J < 150^\circ\text{C}$	30	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	$T_C = 25^\circ\text{C}$, $T_J < 150^\circ\text{C}$, Under 1 ms Pulse Width (Note 1)	60	A
P_C	Collector Dissipation	$T_C = 25^\circ\text{C}$ per One Chip (Note 1)	59	W
T_J	Operating Junction Temperature		-40 ~ 150	$^\circ\text{C}$

CONTROL PART

V_{DD}	Control Supply Voltage	Applied between $V_{DD(H)}$, $V_{DD(L)} - \text{COM}$	20	V
V_{BS}	High-Side Control Bias Voltage	Applied between $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)} - \text{COM}$	-0.3 ~ $V_{DD}+0.3$	V
V_{FO}	Fault Output Supply Voltage	Applied between $V_{FO} - \text{COM}$	-0.3 ~ $V_{DD}+0.3$	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} pin	1	mA
V_{SC}	Current Sensing Input Voltage	Applied between $C_{SC} - \text{COM}$	-0.3 ~ $V_{DD}+0.3$	V

BOOTSTRAP DIODE PART

V_{RRM}	Maximum Repetitive Reverse Voltage		600	V
I_F	Forward Current	$T_C = 25^\circ\text{C}$, $T_J < 150^\circ\text{C}$	0.50	A
I_{FP}	Forward Current (Peak)	$T_C = 25^\circ\text{C}$, $T_J < 150^\circ\text{C}$, Under 1 ms Pulse Width (Note 1)	2.0	A
T_J	Operating Junction Temperature		-40 ~ 150	$^\circ\text{C}$

TOTAL SYSTEM

$V_{PN(\text{PROT})}$	Self-Protection Supply Voltage Limit (Short-Circuit Protection Capability)	$V_{DD} = V_{BS} = 13.5\text{ V} \sim 16.5\text{ V}$ $T_J = 150^\circ\text{C}$, Non-repetitive, $< 2\ \mu\text{s}$	400	V
T_C	Module Case Operation Temperature	See Figure 2	-40 ~ 125	$^\circ\text{C}$
T_{STG}	Storage Temperature		-40 ~ 125	$^\circ\text{C}$
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, AC 1 minute, Connect Pins to Heat Sink Plate (Note 3)	4000	V_{rms}

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance (Note 2)	Inverter IGBT Part (per 1/6 module)	-	-	2.1	$^\circ\text{C}/\text{W}$
$R_{th(j-c)F}$		Inverter FWDi Part (per 1/6 module)	-	-	2.8	$^\circ\text{C}/\text{W}$

1. These values had been made an acquisition by the calculation considered to design factor.
2. For the measurement point of case temperature (T_C), please refer to Figure 2.
3. For Recommended Heat-Sink Design, please see Figure 11. If do not follow Recommended, Viso is 2000 V_{rms} .

FND43060T2

ELECTRICAL CHARACTERISTICS – INVERTER PART ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{CE(SAT)}$	Collector – Emitter Saturation Voltage	$V_{DD} = V_{BS} = 15\text{ V}$, $V_{IN} = 5\text{ V}$	–	1.65	2.25	V
V_F	FWDi Forward Voltage	$V_{IN} = 0\text{ V}$	–	2.00	2.60	V
HS	t_{ON}	Switching Times $V_{PN} = 300\text{ V}$, $V_{DD} = V_{BS} = 15\text{ V}$, $I_C = 30\text{ A}$, $T_J = 25^\circ\text{C}$ $V_{IN} = 0\text{ V} \leftrightarrow 5\text{ V}$, Inductive Load (Note 4)	0.45	0.85	1.35	μs
			–	0.20	0.50	μs
			–	0.70	1.20	μs
			–	0.15	0.45	μs
			–	0.10	–	μs
LS	t_{ON}	$V_{PN} = 300\text{ V}$, $V_{DD} = V_{BS} = 15\text{ V}$, $I_C = 30\text{ A}$, $T_J = 25^\circ\text{C}$ $V_{IN} = 0\text{ V} \leftrightarrow 5\text{ V}$, Inductive Load (Note 4)	0.5	0.90	1.40	μs
			–	0.30	0.60	μs
			–	0.80	1.30	μs
			–	0.15	0.45	μs
			–	0.15	–	μs
I_{CES}	Collector–Emitter Leakage Current	$V_{CE} = V_{CES}$	–	–	1	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. t_{ON} and t_{OFF} include the propagation delay of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 4.

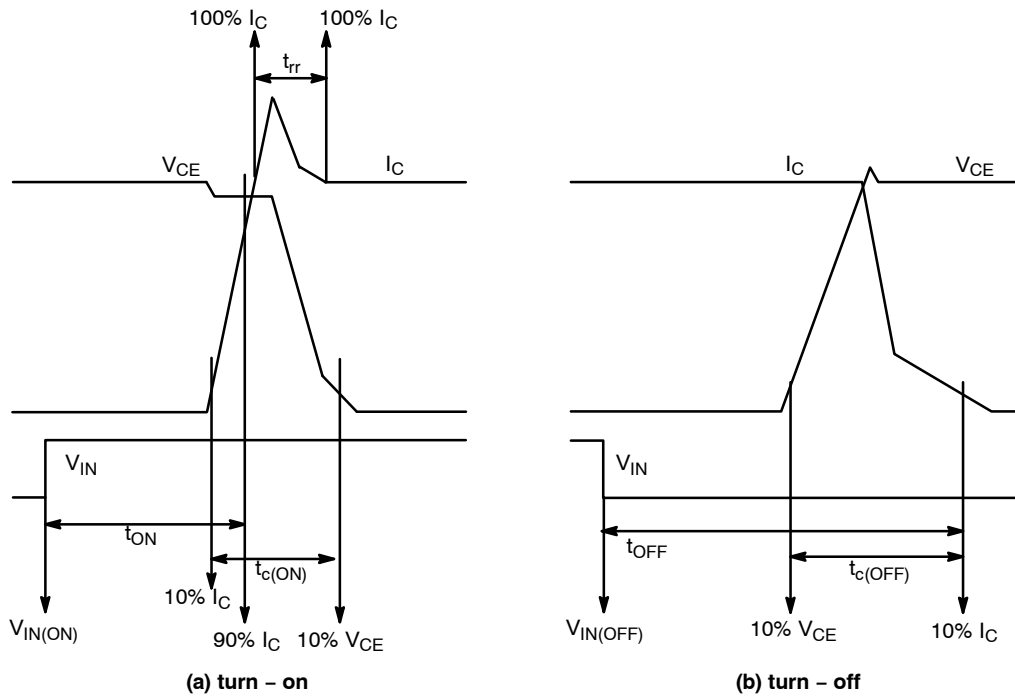


Figure 4. Switching Time Definition

FND43060T2

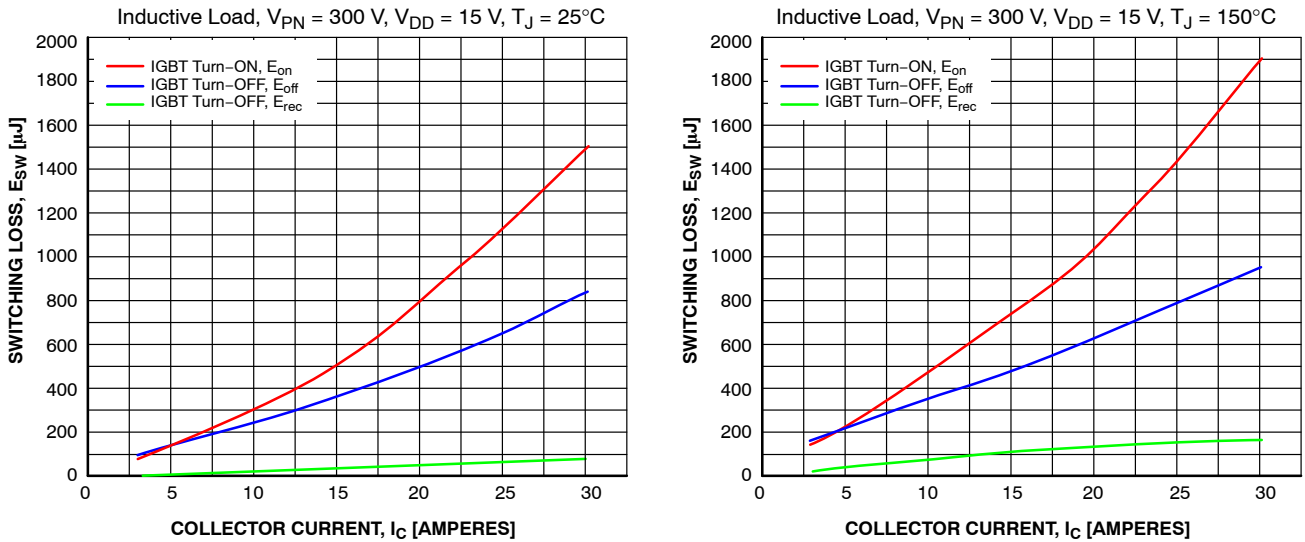


Figure 5. Switching Loss Characteristics (Typical)

CONTROL PART

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
I_{QDDH}	Quiescent V_{DD} Supply Current	$V_{DD(H)} = 15\text{ V}$, $I_{N(UH,VH,WH)} = 0\text{ V}$	$V_{DD(H)} - \text{COM}$	-	-	0.10	mA
I_{QDDL}		$V_{DD(L)} = 15\text{ V}$, $I_{N(UL,VL,WL)} = 0\text{ V}$	$V_{DD(L)} - \text{COM}$	-	-	2.65	mA
I_{PDDH}	Operating V_{DD} Supply Current	$V_{DD(H)} = 15\text{ V}$, $f_{PWM} = 20\text{ kHz}$, duty = 50%, Applied to one PWM Signal Input for High-Side	$V_{DD(H)} - \text{COM}$	-	-	0.15	mA
I_{PDDL}		$V_{DD(L)} = 15\text{ V}$, $f_{PWM} = 20\text{ kHz}$, duty = 50%, Applied to one PWM Signal Input for Low-Side	$V_{DD(L)} - \text{COM}$	-	-	4.00	mA
I_{QBS}	Quiescent V_{BS} Supply Current	$V_{BS} = 15\text{ V}$, $I_{N(UH,VH,WH)} = 0\text{ V}$	$V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$	-	-	0.30	mA
I_{PBS}	Operating V_{BS} Supply Current	$V_{DD} = V_{BS} = 15\text{ V}$, $f_{PWM} = 20\text{ kHz}$, duty = 50%, Applied to one PWM Signal Input for High-Side	$V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$	-	-	2.00	mA
V_{FOH}	Fault Output Voltage	$V_{SC} = 0\text{ V}$, V_{FO} Circuit: 4.7 k Ω to 5 V Pull-up		4.5	-	-	V
V_{FOL}		$V_{SC} = 1\text{ V}$, V_{FO} Circuit: 4.7 k Ω to 5 V Pull-up		-	-	0.5	V
$V_{SC(ref)}$	Short Circuit Trip Level	$V_{DD} = 15\text{ V}$ (Note 5)	$C_{SC} - \text{COM}$	0.45	0.50	0.55	V
UV_{DDD}	Supply Circuit Under-Voltage Protection	Detection Level		10.5	-	13.0	V
UV_{DDR}		Reset Level		11.0	-	13.5	V
UV_{BSD}		Detection Level		10.0	-	12.5	V
UV_{BSR}		Reset Level		10.5	-	13.0	V
t_{FOD}	Fault-Out Pulse Width			30	-	-	μs
$V_{IN(ON)}$	ON Threshold Voltage	Applied between $I_{N(UH)}$, $I_{N(VH)}$, $I_{N(WH)}$, $I_{N(UL)}$, $I_{N(VL)}$, $I_{N(WL)} - \text{COM}$		-	-	2.6	V
$V_{IN(OFF)}$	OFF Threshold Voltage			0.8	-	-	V
R_{TH}	Resistance of Thermistor	@ $T_{TH} = 25^\circ\text{C}$ (Note 6)		-	47	-	k Ω
		@ $T_{TH} = 100^\circ\text{C}$		-	2.9	-	k Ω

5. Short-circuit current protection is functioning only at the low-sides.

6. T_{TH} is the temperature of thermistor itself. To know case temperature (T_C), please make the experiment considering your application.

FND43060T2

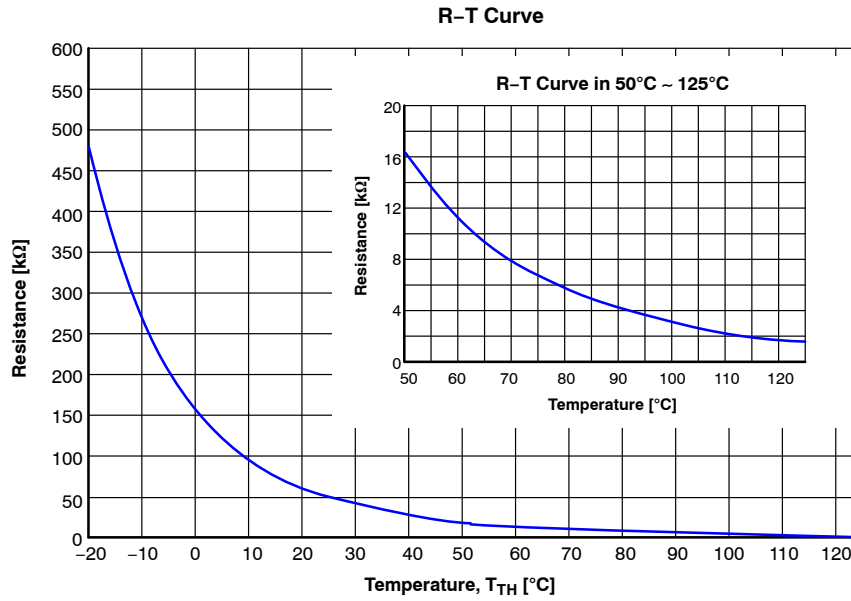
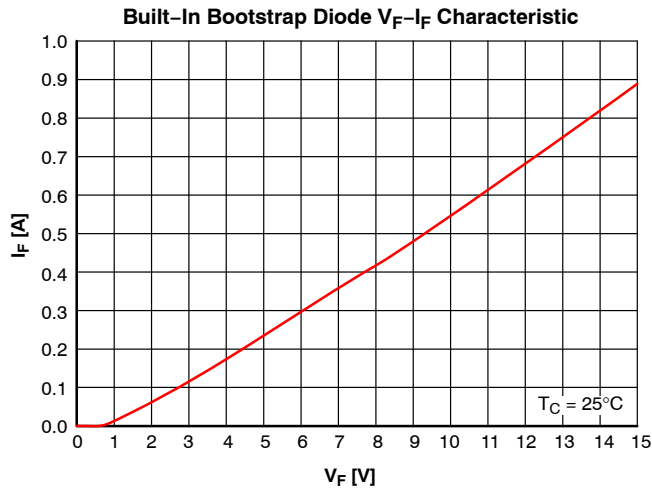


Figure 6. R-T Curve of the Built-In Thermistor

BOOTSTRAP DIODE PART

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_F	Forward Voltage	$I_F = 0.1 \text{ A}$, $T_C = 25^\circ\text{C}$	-	2.5	-	V
t_{rr}	Reverse-Recovery Time	$I_F = 0.1 \text{ A}$, $dI_F/dt = 50 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$	-	80	-	ns



NOTE: Built-in bootstrap diode includes around 15 Ω resistance characteristic.

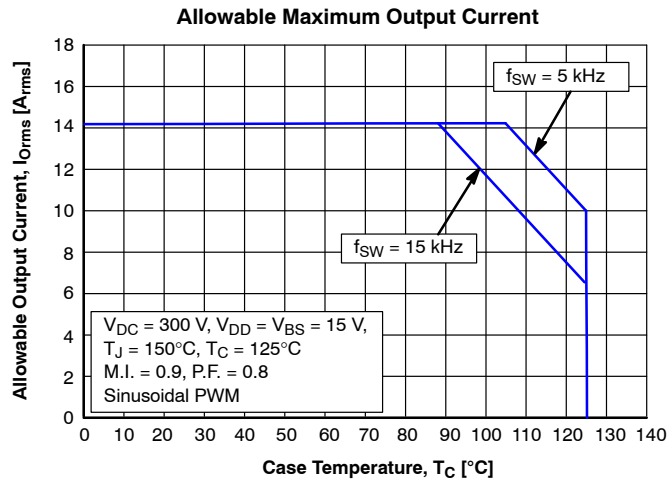
Figure 7. Built-In Bootstrap Diode Characteristics

FND43060T2

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{PN}	Supply Voltage	Applied between P – N_U , N_V , N_W	–	300	400	V
V_{DD}	Control Supply Voltage	Applied between $V_{DD(H)}$ – COM, $V_{DD(L)}$ – COM	13.5	15.0	16.5	V
V_{BS}	High-Side Bias Voltage	Applied between $V_{B(U)}$ – $V_{S(U)}$, $V_{B(V)}$ – $V_{S(V)}$, $V_{B(W)}$ – $V_{S(W)}$	13.0	15.0	18.5	V
dV_{DD}/dt , dV_{BS}/dt	Control Supply Variation		–1	–	1	V/ μ s
t_{dead}	Blanking Time for Preventing Arm-Short	For Each Input Signal	1.0	–	–	μ s
f_{PWM}	PWM Input Signal	$-40^{\circ}\text{C} \leq T_C \leq 150^{\circ}\text{C}$, $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$	–	–	20	kHz
V_{SEN}	Voltage for Current Sensing	Applied between N_U , N_V , N_W – COM (Including Surge Voltage)	–4	–	4	V
$PW_{IN(ON)}$	Minimum Input Pulse Width	$V_{DD} = V_{BS} = 15\text{ V}$, $I_C \leq 60\text{ A}$, Wiring Inductance between N_U , N_V , N_W and DC Link N < 10 nH (Note 7)	1.2	–	–	μ s
$PW_{IN(OFF)}$			1.2	–	–	
T_J	Junction Temperature		–40	–	150	$^{\circ}\text{C}$

7. This product might not make response if input pulse width is less than the recommended value.



NOTE: This allowable output current value is the reference data for the safe operation of this product. This may be different from the actual application and operating condition

Figure 8. Allowable Maximum Output Current

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Conditions	Value			Unit	
		Min.	Typ.	Max.		
Device Flatness	See Figure 9	0	–	+120	μm	
Mounting Torque	Mounting Screw: M3 See Figure 10	Recommended 0.7 N•m	0.6	0.7	0.8	N•m
		Recommended 7.1 kg•cm	6.2	7.1	8.1	kg•cm
Weight		–	11.00	–	g	

FND43060T2

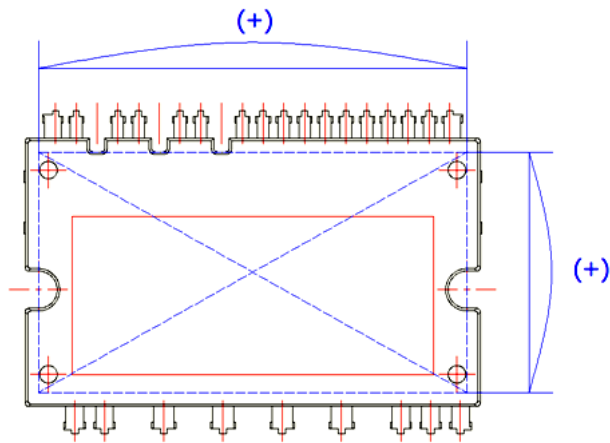


Figure 9. Flatness Measurement Position

Pre-Screwing: 1 à 2
Final Screwing: 2 à 1

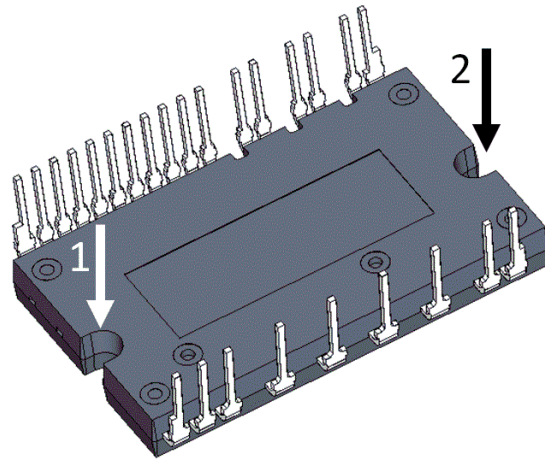


Figure 10. Mounting Screws Torque Order

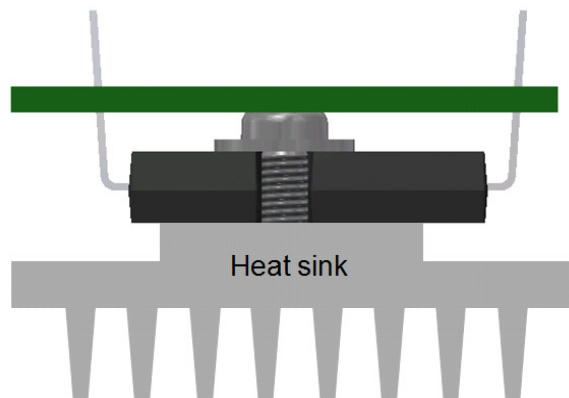


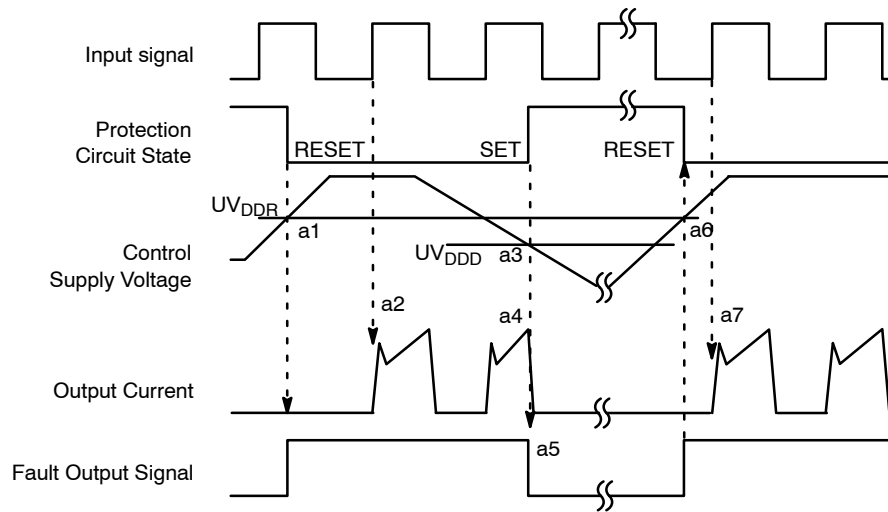
Figure 11. Recommended Heat-Sink Design

NOTES:

- 8. Do not make over torque when mounting screws. Much mounting torque may cause ceramic cracks, as well as bolts and Al heat-sink destruction.
- 9. Avoid one side tightening stress. Figure 10 shows the recommended torque order for mounting screws. Uneven mounting can cause the ceramic substrate of the SPM 45 package to be damaged. The pre-screwing torque is set to 20 ~ 30% of maximum torque rating.

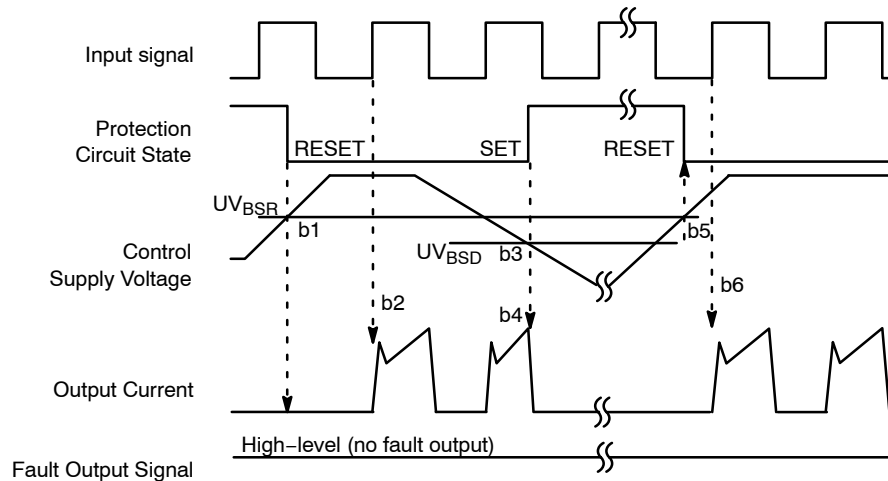
FND43060T2

TIME CHARTS OF PROTECTIVE FUNCTION



- a1: Control supply voltage rises: after the voltage rises UV_{DDR} , the circuits start to operate when next input is applied.
- a2: Normal operation: IGBT ON and carrying current.
- a3: Under voltage detection (UV_{DDDD}).
- a4: IGBT OFF in spite of control input condition.
- a5: Fault output operation starts.
- a6: Under voltage reset (UV_{DDR}).
- a7: Normal operation: IGBT ON and carrying current.

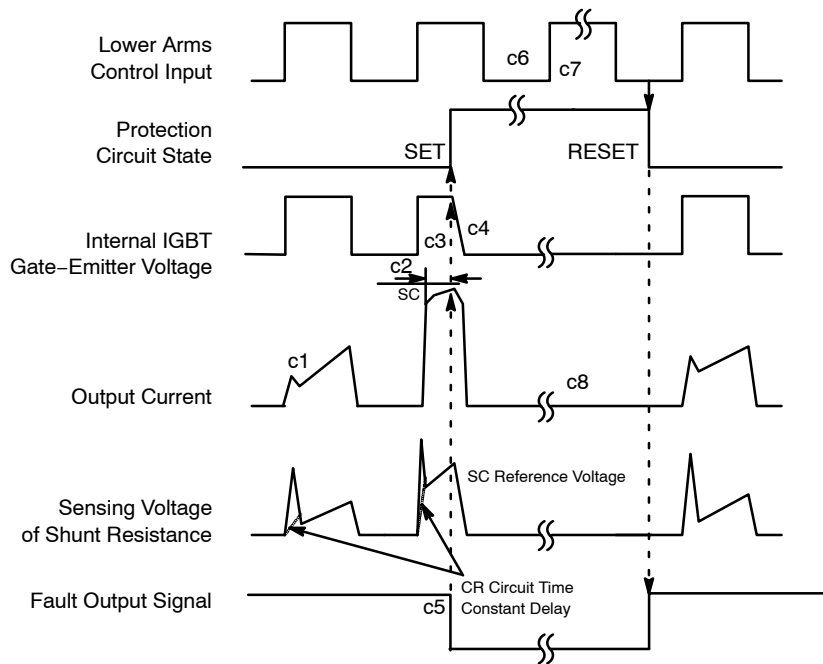
Figure 12. Under-Voltage Protection (Low-Side)



- b1: Control supply voltage rises: after the voltage reaches UV_{BSR} , the circuits start to operate when next input is applied.
- b2: Normal operation: IGBT ON and carrying current.
- b3: Under voltage detection (UV_{BSD}).
- b4: IGBT OFF in spite of control input condition, but there is no fault output signal.
- b5: Under voltage reset (UV_{BSR}).
- b6: Normal operation: IGBT ON and carrying current..

Figure 13. Under-Voltage Protection (High-Side)

FND43060T2

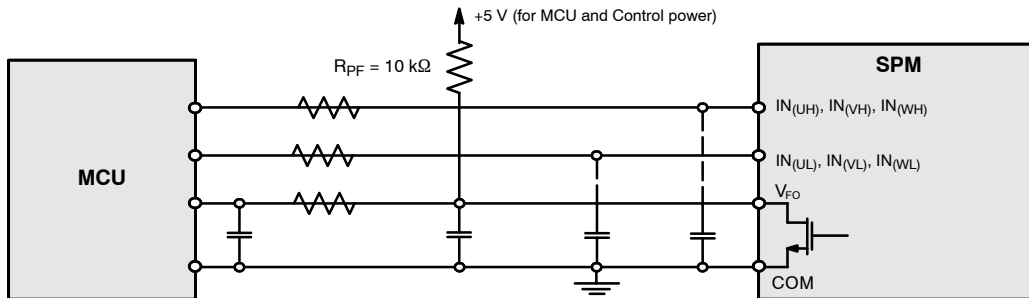


(with the external sense resistance and CR connection)

- c1: Normal operation: IGBT ON and carrying current.
- c2: Short-circuit current detection (SC trigger).
- c3: Hard IGBT gate interrupt.
- c4: IGBT turns OFF.
- c5: Input "LOW": IGBT OFF state.
- c6: Input "HIGH": IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.
- c7: IGBT OFF state.
- c8: Normal operation: IGBT ON and carrying current.

Figure 14. Short-Circuit Protection (Low-Side Operation Only)

INPUT/OUTPUT INTERFACE CIRCUIT



NOTE:

10. RC coupling at each input (parts shown dotted) might change depending on the PWM control scheme in the application and the wiring impedance of the application's printed circuit board. The input signal section of the Motion SPM 45 product integrates a 5 kΩ (typ.) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the signal voltage drop at input terminal.

Figure 15. Recommended MCU I/O Interface Circuit

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

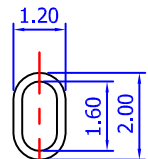
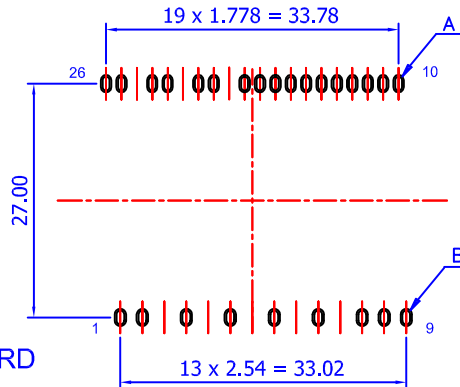
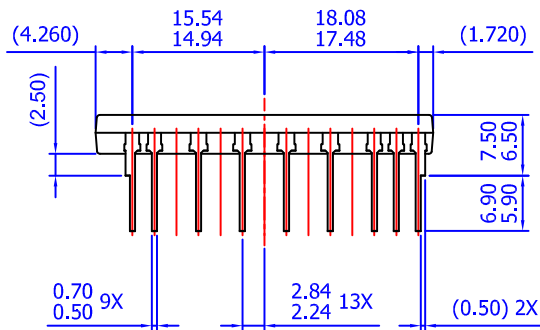
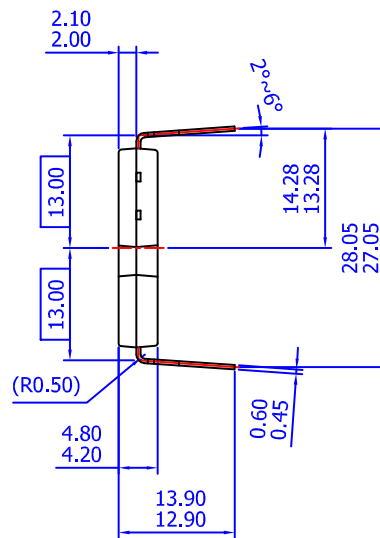
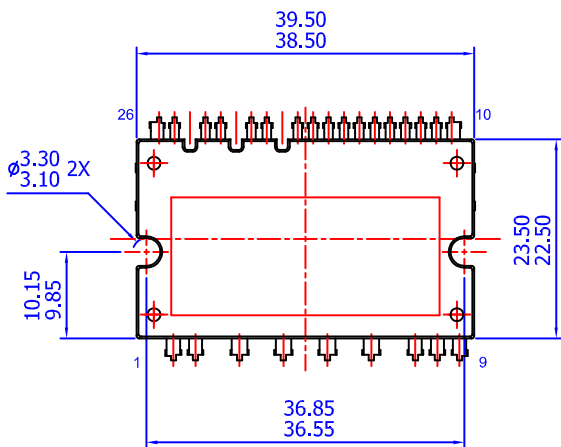
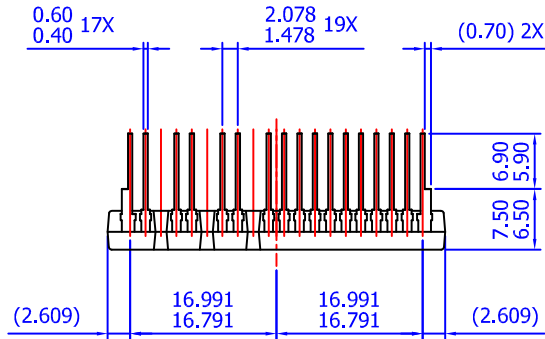
ON Semiconductor®



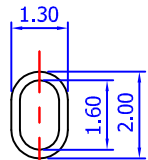
SPMAA-C26 / 26LD, PDD STD CERAMIC TYPE, LONG LEAD DUAL FORM TYPE

CASE MODFC
ISSUE O

DATE 31 JAN 2017



DETAIL A
(SCALE N/A)



DETAIL B
(SCALE N/A)

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE DOES NOT COMPLY TO ANY CURRENT PACKAGING STANDARD
 - B) ALL DIMENSIONS ARE IN MILLIMETERS
 - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
 - D) () IS REFERENCE

LAND PATTERN RECOMMENDATIONS

DOCUMENT NUMBER:	98AON13555G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SPMAA-C26 / 26LD, PDD STD CERAMIC TYPE, LONG LEAD DUAL	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:
Voice Mail: 1 800-282-9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative