

High-Speed CMOS Logic 4-Bit Magnitude Comparator

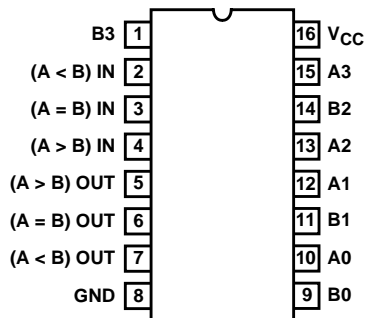
August 1997 - Revised October 2003

Features

- Buffered Inputs and Outputs
- Typical Propagation Delay: 13ns (Data to Output at $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^\circ C$)
- Serial or Parallel Expansion Without External Gating
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . $-55^\circ C$ to $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Pinout

CD54HC85, CD54HCT85 (CERDIP)
CD74HC85 (PDIP, SOIC, SOP, TSSOP)
CD74HCT85 (PDIP, SOIC)
TOP VIEW



Description

The 'HC85 and 'HCT85 are high speed magnitude comparators that use silicon-gate CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

These 4-bit devices compare two binary, BCD, or other monotonic codes and present the three possible magnitude results at the outputs ($A > B$, $A < B$, and $A = B$). The 4-bit input words are weighted (A_0 to A_3 and B_0 to B_3), where A_3 and B_3 are the most significant bits.

The devices are expandable without external gating, in both serial and parallel fashion. The upper part of the truth table indicates operation using a single device or devices in a serially expanded application. The parallel expansion scheme is described by the last three entries in the truth table.

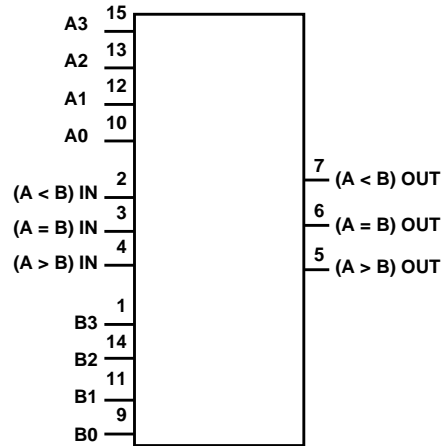
Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE |
|--------------|------------------|--------------|
| CD54HC85F3A | -55 to 125 | 16 Ld CERDIP |
| CD54HCT85F3A | -55 to 125 | 16 Ld CERDIP |
| CD74HC85E | -55 to 125 | 16 Ld PDIP |
| CD74HC85M | -55 to 125 | 16 Ld SOIC |
| CD74HC85MT | -55 to 125 | 16 Ld SOIC |
| CD74HC85M96 | -55 to 125 | 16 Ld SOIC |
| CD74HC85NSR | -55 to 125 | 16 Ld SOP |
| CD74HC85PW | -55 to 125 | 16 Ld TSSOP |
| CD74HC85PWR | -55 to 125 | 16 Ld TSSOP |
| CD74HC85PWT | -55 to 125 | 16 Ld TSSOP |
| CD74HCT85E | -55 to 125 | 16 Ld PDIP |
| CD74HCT85M | -55 to 125 | 16 Ld SOIC |
| CD74HCT85MT | -55 to 125 | 16 Ld SOIC |
| CD74HCT85M96 | -55 to 125 | 16 Ld SOIC |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small-quantity reel of 250.

CD54HC85, CD74HC85, CD54HCT85, CD74HCT85

PFunctional Diagram



TRUTH TABLE

| COMPARING INPUTS | | | | CASCADING INPUTS | | | OUTPUTS | | |
|--|----------|---------|---------|------------------|-------|-------|---------|-------|-------|
| A3, B3 | A2, B2 | A1, B1 | A0, B0 | A > B | A < B | A = B | A > B | A < B | A = B |
| SINGLE DEVICE OR SERIES CASCADING | | | | | | | | | |
| A3 > B3 | X | X | X | X | X | X | H | L | L |
| A3 < B3 | X | X | X | X | X | X | L | H | L |
| A3 = B3 | A2 > B2 | X | X | X | X | X | H | L | L |
| A3 = B3 | A2 < B2 | X | X | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 > B1 | X | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 < B1 | X | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 > B0 | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 < B0 | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | L | L | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | H | L | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | L | H | L | L | H |
| PARALLEL CASCADING | | | | | | | | | |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | X | X | H | L | L | H |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | H | L | L | L | L |
| A3 = B3 | A2 = B2S | A1 = B1 | A0 = B0 | L | L | L | H | H | L |

H = High Voltage Level, L = Low Voltage, Level, X = Don't Care

CD54HC85, CD74HC85, CD54HCT85, CD74HCT85

Absolute Maximum Ratings

| | |
|--|-------------|
| DC Supply Voltage, V_{CC} | -0.5V to 7V |
| DC Input Diode Current, I_{IK} | |
| For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Diode Current, I_{OK} | |
| For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ | $\pm 20mA$ |
| DC Output Source or Sink Current per Output Pin, I_O | |
| For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ | $\pm 25mA$ |
| DC V_{CC} or Ground Current, I_{CC} or I_{GND} | $\pm 50mA$ |

Thermal Information

| | |
|--|----------------|
| Package Thermal Impedance, θ_{JA} (see Note 1): | |
| E (PDIP) Package | 67°C/W |
| M (SOIC) Package | 73°C/W |
| NS (SOP) Package | 64°C/W |
| PW (TSSOP) Package | 108°C/W |
| Maximum Junction Temperature | 150°C |
| Maximum Storage Temperature Range | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) | 300°C |
| (SOIC - Lead Tips Only) | |

Operating Conditions

| | |
|--|----------------|
| Temperature Range (T_A) | -55°C to 125°C |
| Supply Voltage Range, V_{CC} | |
| HC Types | .2V to 6V |
| HCT Types | 4.5V to 5.5V |
| DC Input or Output Voltage, V_I, V_O | 0V to V_{CC} |
| Input Rise and Fall Time | |
| 2V | 1000ns (Max) |
| 4.5V | 500ns (Max) |
| 6V | 400ns (Max) |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | | V_{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS | |
|---|----------|----------------------|------------|--------------|------|------|-----------|---------------|---------|----------------|---------|---------|---|
| | | V_I (V) | I_O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | | |
| HC TYPES | | | | | | | | | | | | | |
| High Level Input Voltage | V_{IH} | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V | |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V | |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V | |
| Low Level Input Voltage | V_{IL} | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V | |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V | |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V | |
| High Level Output Voltage CMOS Loads | V_{OH} | V_{IH} or V_{IL} | -0.02 | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | V_{OH} | V_{IH} or V_{IL} | - | - | - | - | - | - | - | - | - | V | |
| | | | -4 | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | V_{OL} | V_{IH} or V_{IL} | 0.02 | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | V_{OL} | V_{IH} or V_{IL} | 4 | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I_I | V_{CC} or GND | - | 6 | - | - | ± 0.1 | - | ± 1 | - | ± 1 | μA | |
| Quiescent Device Current | I_{CC} | V_{CC} or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | μA | |

CD54HC85, CD74HC85, CD54HCT85, CD74HCT85

DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|---------------------------|------------------------------------|---------------------|---------------------|------|-----|------|---------------|------|----------------|-----|-------|
| | | V _I (V) | I _O (mA) | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HCT TYPES | | | | | | | | | | | | |
| High Level Input Voltage | V _{IH} | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | V _{IL} | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | V _{OH} | V _{IH} or V _{IL} | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | V _{OL} | V _{IH} or V _{IL} | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | I _I | V _{CC} and GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | I _{CC} | V _{CC} or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | µA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | ΔI _{CC} (Note 2) | V _{CC} -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | µA |

NOTE:

2. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

| INPUT | UNIT LOADS |
|-----------------------------|------------|
| A0-A3, B0-B3 and (A = B) IN | 1.5 |
| (A > B) IN, (A < B) IN | 1 |

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Table, e.g. 360µA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | V _{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
|--|-------------------------------------|-----------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| HC TYPES | | | | | | | | | | | |
| Propagation Delay, A _n , B _n to (A > B) OUT, (A < B) OUT | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 195 | - | 245 | - | 295 | ns |
| | | | 4.5 | - | - | 39 | - | 47 | - | 59 | ns |
| | | C _L = 15pF | 5 | - | 16 | - | - | - | - | - | ns |
| | | C _L = 50pF | 6 | - | - | 33 | - | 42 | - | 50 | ns |
| A _n , B _n to (A = B) OUT | t _{PLH} , t _{PHL} | C _L = 50pF | 2 | - | - | 175 | - | 240 | - | 265 | ns |
| | | | 4.5 | - | - | 35 | - | 44 | - | 53 | ns |
| | | C _L = 15pF | 5 | - | 14 | - | - | - | - | - | ns |
| | | C _L = 50pF | 6 | - | - | 30 | - | 37 | - | 45 | ns |

CD54HC85, CD74HC85, CD54HCT85, CD74HCT85

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | V_{CC} (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS | |
|--|--------------------|---------------------|---------------------|------|-----|-----|---------------|-----|----------------|-----|-------|----|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | | |
| (A > B) IN, (A < B) IN, (A = B) IN to (A > B) OUT, (A < B) OUT | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 2 | - | - | 140 | - | 175 | - | 210 | ns | |
| | | | 4.5 | - | - | 28 | - | 35 | - | 42 | ns | |
| | | | $C_L = 15\text{pF}$ | 5 | - | 11 | - | - | - | - | - | ns |
| | | | $C_L = 50\text{pF}$ | 6 | - | - | 24 | - | 30 | - | 36 | ns |
| (A > B) IN to (A = B) OUT | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 2 | - | - | 120 | - | 150 | - | 180 | ns | |
| | | | 4.5 | - | - | 24 | - | 30 | - | 36 | ns | |
| | | | $C_L = 15\text{pF}$ | 5 | - | 9 | - | - | - | - | - | ns |
| | | | $C_L = 50\text{pF}$ | 6 | - | - | 20 | - | 26 | - | 31 | ns |
| Power Dissipation Capacitance (Notes 3, 4) | C_{PD} | - | 5 | - | 24 | - | - | - | - | - | pF | |
| Output Transition Times (Figure 1) | t_{TLH}, t_{THL} | $C_L = 50\text{pF}$ | 2 | - | - | 75 | - | 95 | - | 110 | ns | |
| | | | 4.5 | - | - | 15 | - | 19 | - | 22 | ns | |
| | | | 6 | - | - | 13 | - | 16 | - | 19 | ns | |
| Input Capacitance | C_{IN} | - | - | - | 10 | - | 10 | - | 10 | pF | | |
| HCT TYPES | | | | | | | | | | | | |
| Propagation Delay, An, Bn to (A > B) OUT, (A < B) OUT | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 37 | - | 46 | - | 56 | ns | |
| | | | $C_L = 15\text{pF}$ | 5 | - | 15 | - | - | - | - | - | ns |
| An, Bn to (A = B) OUT | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 40 | - | 50 | - | 60 | ns | |
| | | | $C_L = 15\text{pF}$ | 5 | - | 17 | - | - | - | - | - | ns |
| (A > B) IN, (A < B) IN, (A = B) IN to (A > B) OUT, (A < B) OUT | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 30 | - | 38 | - | 45 | ns | |
| | | | $C_L = 15\text{pF}$ | 5 | - | 12 | - | - | - | - | - | ns |
| (A > B) IN to (A = B) OUT | t_{PLH}, t_{PHL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 31 | - | 39 | - | 47 | ns | |
| | | | $C_L = 15\text{pF}$ | 5 | - | 13 | - | - | - | - | - | ns |
| Output Transition Times (Figure 1) | t_{TLH}, t_{THL} | $C_L = 50\text{pF}$ | 4.5 | - | - | 15 | - | 19 | - | 22 | ns | |
| Power Dissipation Capacitance (Notes 3, 4) | C_{PD} | - | 5 | - | 26 | - | - | - | - | - | pF | |
| Input Capacitance | C_{IN} | - | - | - | 10 | - | 10 | - | 10 | pF | | |

NOTES:

- C_{PD} is used to determine the dynamic power consumption, per gate/package.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

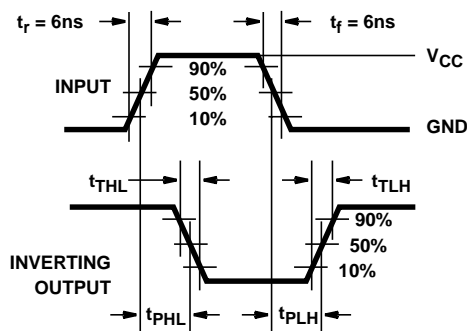


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

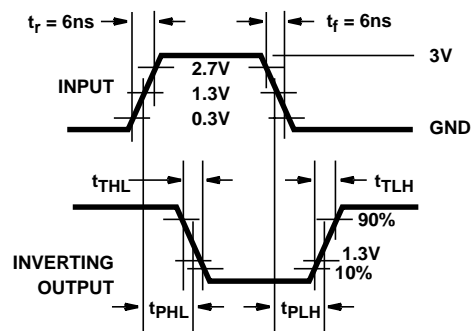


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

Test Circuits and Waveforms

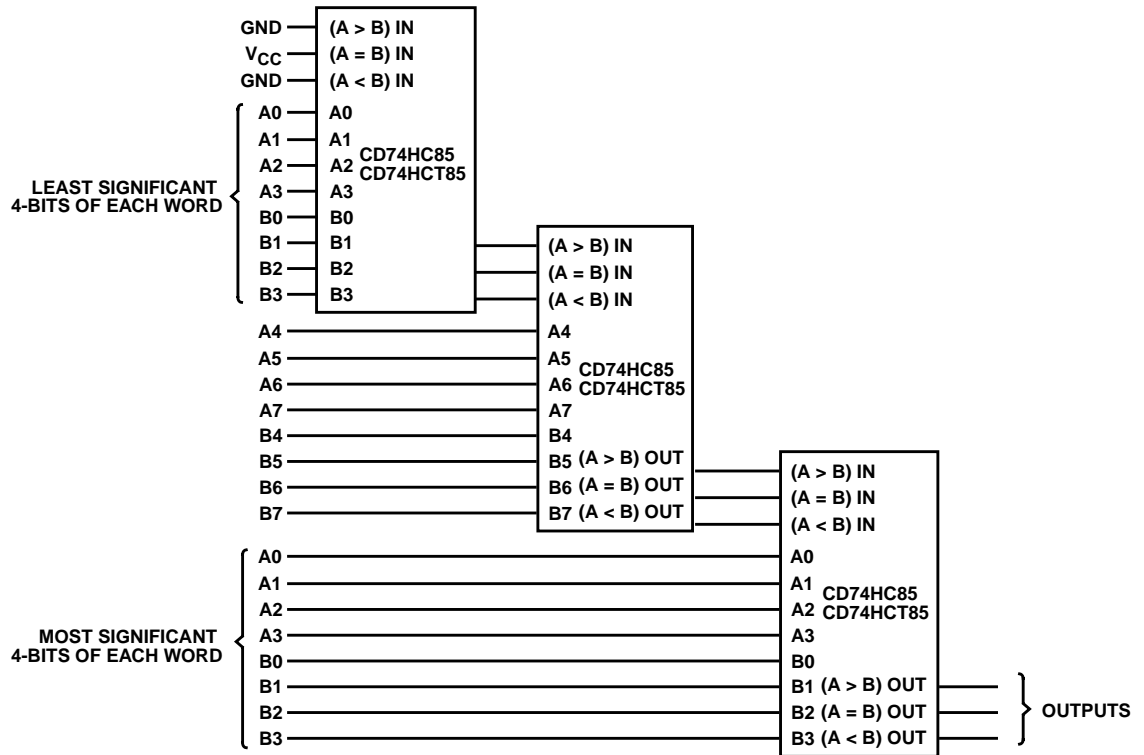


FIGURE 3. SERIES CASCADING - COMPARING 12-BIT WORDS

Test Circuits and Waveforms

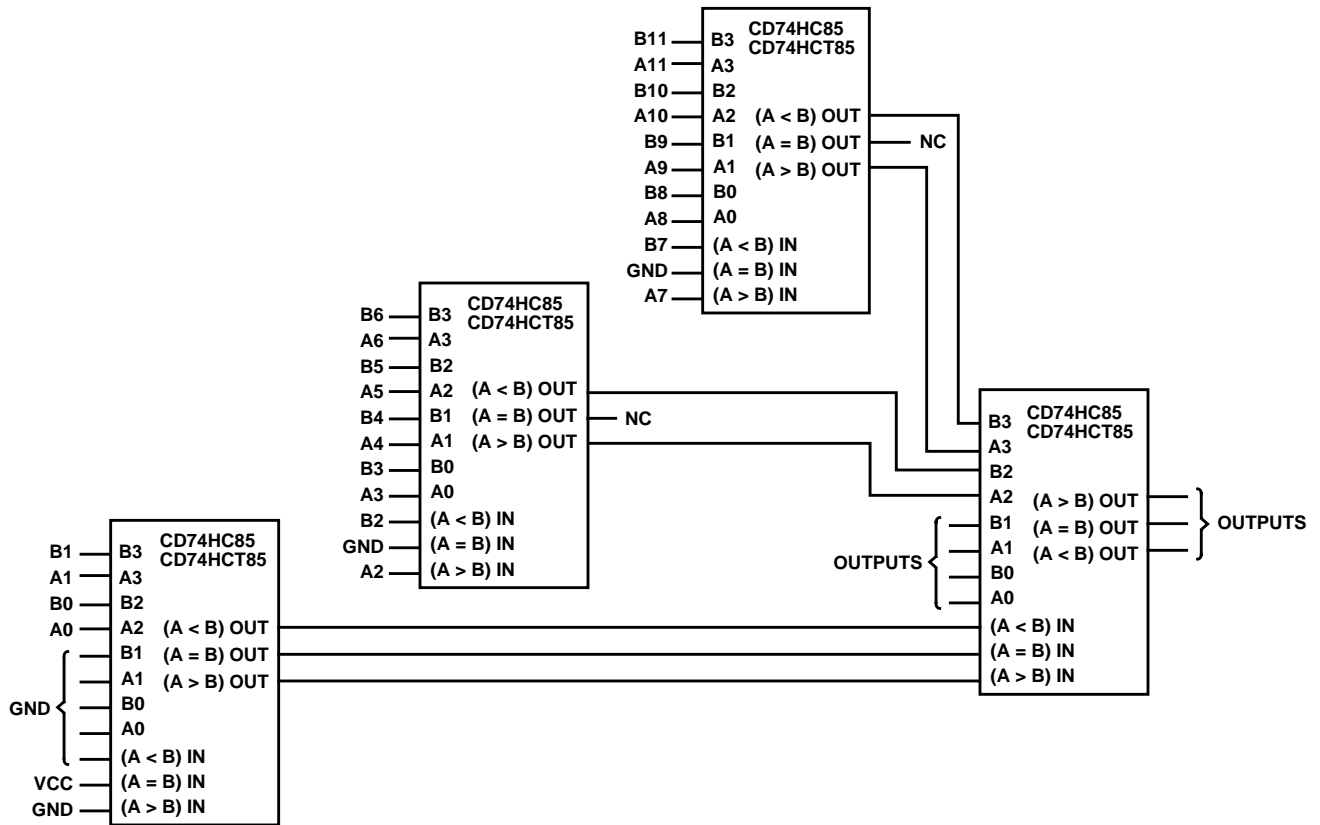


FIGURE 4. PARALLEL CASCADING - COMPARING 12-BIT WORDS

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|----------------------------|-------------------------|----------------------|--------------|--------------------------------|-------------------------|
| 5962-8867201EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8867201EA CD54HCT85F3A | Samples |
| 8601301EA | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 8601301EA CD54HC85F3A | Samples |
| CD54HC85F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 8601301EA CD54HC85F3A | Samples |
| CD54HCT85F3A | ACTIVE | CDIP | J | 16 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-8867201EA CD54HCT85F3A | Samples |
| CD74HC85E | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC85E | Samples |
| CD74HC85EE4 | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC85E | Samples |
| CD74HC85M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC85M | Samples |
| CD74HC85M96 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC85M | Samples |
| CD74HC85M96E4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC85M | Samples |
| CD74HC85M96G4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC85M | Samples |
| CD74HC85MT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC85M | Samples |
| CD74HC85MTE4 | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC85M | Samples |
| CD74HC85NSR | ACTIVE | SO | NS | 16 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC85M | Samples |
| CD74HC85PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ85 | Samples |
| CD74HC85PWE4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ85 | Samples |
| CD74HC85PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ85 | Samples |
| CD74HC85PWT | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ85 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD74HC85PWTE4 | ACTIVE | TSSOP | PW | 16 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ85 | Samples |
| CD74HCT85E | ACTIVE | PDIP | N | 16 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT85E | Samples |
| CD74HCT85M | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT85M | Samples |
| CD74HCT85MT | ACTIVE | SOIC | D | 16 | 250 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT85M | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD54HC85, CD54HCT85, CD74HC85, CD74HCT85 :

- Catalog: [CD74HC85](#), [CD74HCT85](#)
- Military: [CD54HC85](#), [CD54HCT85](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD74HC85M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC85NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD74HC85PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC85PWT | TSSOP | PW | 16 | 250 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD74HC85M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74HC85NSR | SO | NS | 16 | 2000 | 367.0 | 367.0 | 38.0 |
| CD74HC85PWR | TSSOP | PW | 16 | 2000 | 367.0 | 367.0 | 35.0 |
| CD74HC85PWT | TSSOP | PW | 16 | 250 | 367.0 | 367.0 | 35.0 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

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