

- Functionally Equivalent to AMD's AM29823 and AM29824
- Provides Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Buffered Control Inputs to Reduce DC Loading Effects
- Package Options Include both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs
- Dependable Texas Instruments Quality and Reliability

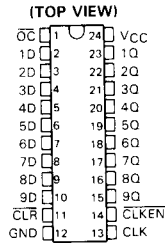
description

These 9-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers, parity bus interfacing and working registers.

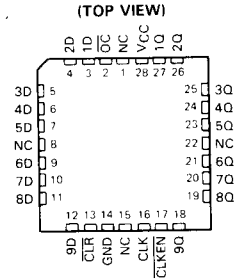
With the clock enable ($\overline{\text{CLKEN}}$) low, the nine D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{\text{CLKEN}}$ high will disable the clock buffer, thus latching the outputs. The 'ALS29823 has noninverting D inputs and the 'ALS29824 has inverting D inputs. Taking the CLR input low causes the nine Q outputs to go low independently of the clock.

A buffered output-control input ($\overline{\text{OC}}$) can be used to place the nine outputs in either normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output control does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

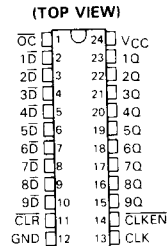
SN54ALS29823 . . . JT PACKAGE
SN74ALS29823 . . . DW OR NT PACKAGE



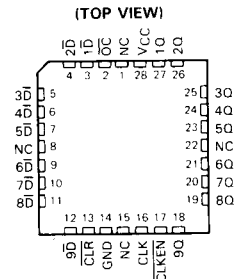
SN54ALS29823 . . . FK PACKAGE
SN74ALS29823 . . . FN PACKAGE



SN54ALS29824 . . . JT PACKAGE
SN74ALS29824 . . . DW OR NT PACKAGE



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SN74ALS29824 . . . FN PACKAGE



PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

SN54ALS29823, SN54ALS29824, SN74ALS29823, SN74ALS29824

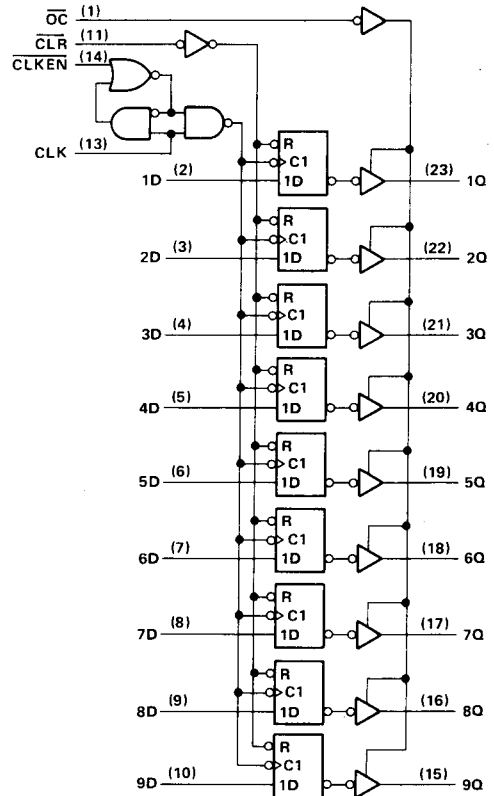
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

The SN54AS' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AS' family is characterized for operation from 0°C to 70°C .

'ALS29823 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{\text{OC}}$	$\overline{\text{CLR}}$	$\overline{\text{CLKEN}}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	\uparrow	H	H
L	H	L	\uparrow	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

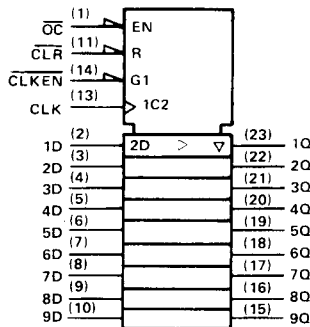
'ALS29823 logic diagram (positive logic)



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ALS and AS Circuits

'ALS29823 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

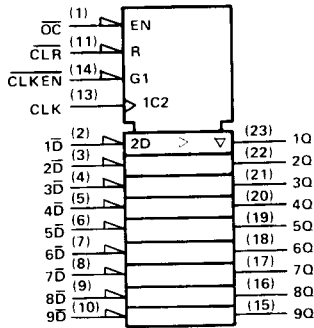
Pin numbers shown are for DW, JT, and NT packages.

SN54ALS29824, SN74ALS29824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

'ALS29824 FUNCTION TABLE

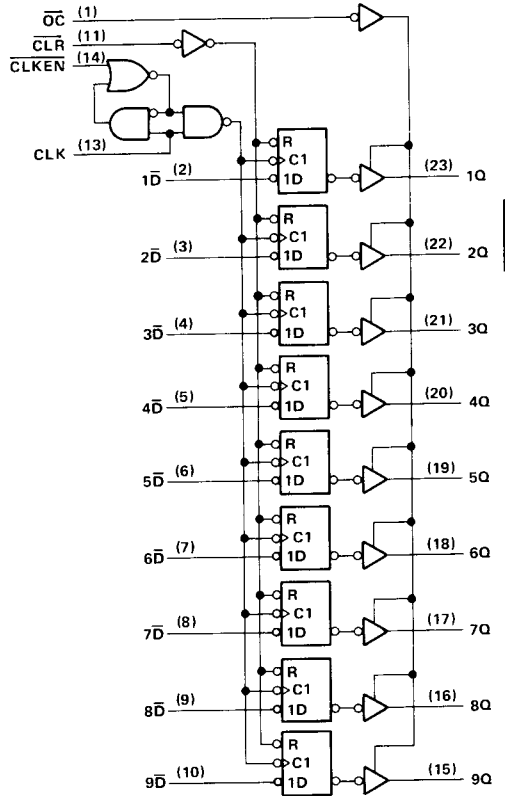
INPUTS					OUTPUT
\overline{OC}	\overline{CLR}	CLKEN	CLK	\overline{D}	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

'ALS29824 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'ALS29824 logic diagram (positive logic)



Pin numbers shown are for DW, JT, and NT packages.

SN54ALS29823, SN54ALS29824, SN74ALS29823, SN74ALS29824
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	5.5 V
Voltage applied to a disabled 3-state output	5.5 V
Input current	100 mA
Output current	-30 mA to 5 mA
Operating free-air temperature range: SN54ALS29823, SN54ALS29824	-55°C to 125°C
SN74ALS29823, SN74ALS29824	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

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ALS and AS Circuits

		SN54ALS29823			SN74ALS29823			UNIT
		SN54ALS29824			SN74ALS29824			
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage	0.7			0.8			V
I_{OH}	High-level output current	-15			-24			mA
I_{OL}	Low-level output current	32			48			mA
t_w	Pulse duration	CLR low						ns
		CLK high or low						
t_{su}	Setup time before CLK ¹	CLR inactive						ns
		Data						
		CLKEN high or low						
t_h	Hold time, \overline{CLKEN} or data after CLK ¹							ns
T_A	Operating free-air temperature	-55	125		0	70		°C

SN54ALS29823, SN54ALS29824, SN74ALS29823, SN74ALS29824

9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]		SN54ALS29823		SN74ALS29823		UNIT
			SN54ALS29824		SN74ALS29824		
			MIN	TYP [‡] MAX	MIN	TYP [‡] MAX	
V _{IK}	V _{CC} = MIN	I _I = -18 mA		-1.2		-1.2	V
V _{OH}	V _{CC} = MIN to MAX,	I _{OH} = -0.4 mA	V _{CC} - 2		V _{CC} - 2		V
	V _{CC} = MIN,	I _{OH} = -15 mA	2.4	3.3			
	V _{CC} = MIN,	I _{OH} = -24 mA			2.4	3.2	
V _{OL}	V _{CC} = MIN,	I _{OL} = 32 mA	0.25	0.4	0.25	0.4	V
	V _{CC} = MIN,	I _{OL} = 48 mA			0.35	0.5	
I _{OZH}	V _{CC} = MAX,	V _O = 2.4 V		20		20	μA
I _{OZL}	V _{CC} = MAX,	V _O = 0.4 V		-20		-20	μA
I _I	V _{CC} = MAX,	V _I = 5.5 V		0.1		0.1	mA
I _{IH}	V _{CC} = MAX,	V _I = 2.7 V		20		20	μA
I _{IL}	V _{CC} = MAX,	V _I = 0.4 V		-0.1		-0.1	mA
I _{OS} [§]	V _{CC} = MAX,	V _O = 0 V	-75	-250	-75	-250	mA
I _{CC}	'ALS29823	V _{CC} = MAX	Outputs high				mA
			Outputs low				
	Outputs disabled		48	48			
	Outputs high						
	Outputs low						
'ALS29824	Outputs disabled		48	48			

[†] For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Additional information on these products can be obtained from the factory as it becomes available.

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ALS and AS Circuits

SN54ALS29823, SN54ALS29824, SN74ALS29823, SN74ALS29824
9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

switching characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS See Figure 1	$V_{CC} = 5\text{ V,}$ $T_A = 25^\circ\text{C}$			$V_{CC} = \text{MIN TO MAX,}^\dagger$ $T_A = \text{MIN TO MAX}^\dagger$				UNIT
				'ALS29823 'ALS29824			SN54ALS29823 SN54ALS29824		SN74ALS29823 SN74ALS29824		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	$C_L = 300\text{ pF}$							ns	
t_{PHL}											
t_{PLH}					5.5						
t_{PHL}				$C_L = 50\text{ pF}$	6.5						
t_{PHL}	$\overline{\text{CLR}}$	Any Q	$C_L = 50\text{ pF}$		13					ns	
t_{PZH}	$\overline{\text{OC}}$	Any Q	$C_L = 300\text{ pF}$							ns	
t_{PZL}											
t_{PZH}				$C_L = 50\text{ pF}$	12						
t_{PZL}					11						
t_{PHZ}	$\overline{\text{OC}}$	Any Q	$C_L = 50\text{ pF}$							ns	
t_{PLZ}											
t_{PHZ}				$C_L = 5\text{ pF}$	5						
t_{PLZ}					5.5						

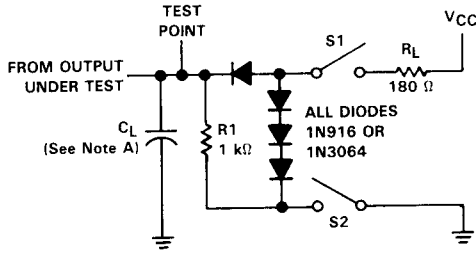
[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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2 ALS and AS Circuits

SN54ALS29823, SN54ALS29824, SN74ALS29823, SN74ALS29824 9-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

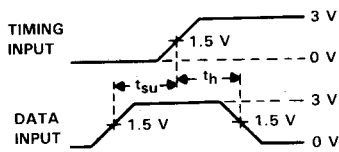
PARAMETER MEASUREMENT INFORMATION



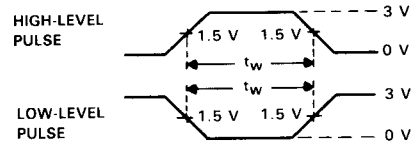
LOAD CIRCUIT

SWITCH POSITION TABLE

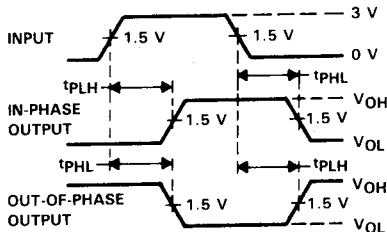
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



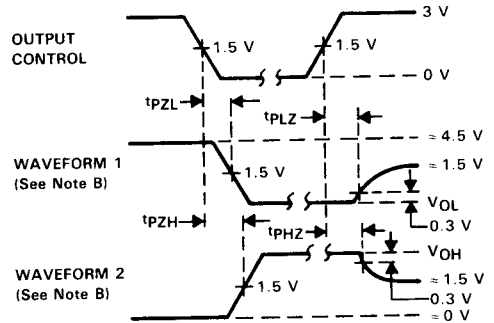
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

FIGURE 1