

NLAS4685

Ultra-Low Resistance Dual SPDT Analog Switch

The NLAS4685 is an advanced CMOS analog switch fabricated in Sub-micron silicon gate CMOS technology. The device is a dual Independent Single Pole Double Throw (SPDT) switch featuring Ultra-Low R_{ON} of 0.8 Ω , for the Normally Closed (NC) switch and for the Normally Opened switch (NO) at 2.7 V.

The part also features guaranteed Break Before Make switching, assuring the switches never short the driver.

The NLAS4685 is available in a 2.0 x 1.5 mm bumped die array, with a 3 x 4 arrangement of solder bumps. The pitch of the solder bumps is 0.5 mm for easy handling.

Features

- Ultra-Low R_{ON} , < 0.8 Ω at 2.7 V
- Threshold Adjusted to Function with 1.8 V Control at $V_{CC} = 2.7-3.3$ V
- Single Supply Operation from 1.8–5.5 V
- Tiny 2 x 1.5 mm Bumped Die
- Low Crosstalk, < 81 dB at 100 kHz
- Full 0– V_{CC} Signal Handling Capability
- High Isolation, –65 dB at 100 kHz
- Low Standby Current, < 50 nA
- Low Distortion, < 0.14% THD
- R_{ON} Flatness of 0.15 Ω
- Pin for Pin Replacement for MAX4685
- Pb-Free Package is Available

Applications

- Cell Phone
- Speaker Switching
- Power Switching (Up to 100 mA)
- Modems
- Automotive



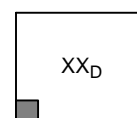
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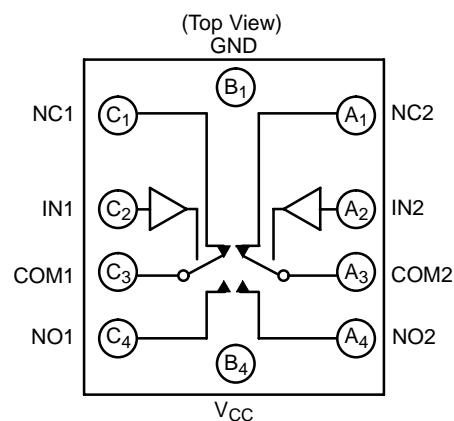
A1
Microbump-10
CASE 489AA

MARKING DIAGRAM



A1
XX = Device Code
D = Date Code

PIN CONNECTIONS AND LOGIC DIAGRAM



FUNCTION TABLE

| IN 1, 2 | NO 1, 2 | NC 1, 2 |
|---------|---------|---------|
| 0 | OFF | ON |
| 1 | ON | OFF |

ORDERING INFORMATION

| Device | Package | Shipping† |
|---------------|---------------------|----------------|
| NLAS4685FCT1 | Microbump | 3000 Tape/Reel |
| NLAS4685FCT1G | Microbump (Pb-Free) | 3000 Tape/Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------------|--|--|------|
| V _{CC} | Positive DC Supply Voltage | -0.5 to +7.0 | V |
| V _{IS} | Analog Input Voltage (V _{NO} , V _{NC} , or V _{COM}) (Note 1) | -0.5 ≤ V _{IS} ≤ V _{CC} + 0.5 | V |
| V _{IN} | Digital Select Input Voltage | -0.5 ≤ V _I ≤ +7.0 | V |
| I _{IK} | DC Current, Into or Out of Any Pin | ±50 | mA |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Signal voltage on NC, NO, and COM exceeding V_{CC} or GND are clamped by the internal diodes. Limit forward diode current to maximum current rating.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---------------------------------|------------------------------------|--|-----------------|------|
| V _{CC} | DC Supply Voltage | 1.8 | 5.5 | V |
| V _{IN} | Digital Select Input Voltage | GND | 5.5 | V |
| V _{IS} | Analog Input Voltage (NC, NO, COM) | GND | V _{CC} | V |
| T _A | Operating Temperature Range | -55 | +125 | °C |
| t _r , t _f | Input Rise or Fall Time, SELECT | V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V | 0 100 | ns/V |

DC CHARACTERISTICS – Digital Section (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V _{CC} ± 10% | Guaranteed Limit | | | Unit |
|------------------|---|---|-----------------------|------------------|--------|---------|------|
| | | | | -55°C to 25°C | < 85°C | < 125°C | |
| V _{IH} | Minimum High-Level Input Voltage, Select Inputs | | 2.0 | 1.4 | 1.4 | 1.4 | V |
| | | | 2.5 | 1.4 | 1.4 | 1.4 | |
| | | | 3.0 | 1.4 | 1.4 | 1.4 | |
| | | | 5.0 | 2.0 | 2.0 | 2.0 | |
| V _{IL} | Maximum Low-Level Input Voltage, Select Inputs | | 2.0 | 0.5 | 0.5 | 0.5 | V |
| | | | 2.5 | 0.5 | 0.5 | 0.5 | |
| | | | 3.0 | 0.5 | 0.5 | 0.5 | |
| | | | 5.0 | 0.8 | 0.8 | 0.8 | |
| I _{IN} | Maximum Input Leakage Current, Select Inputs | V _{IN} = 5.5 V or GND | 5.5 | ± 1.0 | ± 1.0 | ± 1.0 | μA |
| I _{OFF} | Power Off Leakage Current | V _{IN} = 5.5 V or GND | 0 | ± 10 | ± 10 | ± 10 | μA |
| I _{CC} | Maximum Quiescent Supply Current | Select and V _{IS} = V _{CC} or GND | 5.5 | ± 180 | ± 200 | ± 200 | nA |

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DC ELECTRICAL CHARACTERISTICS – Analog Section

| Symbol | Parameter | Condition | $V_{CC} \pm 10\%$ | Guaranteed Maximum Limit | | | | | | Unit |
|--------------------------------|--|--|-------------------|--------------------------|------|--------|------|---------|------|----------|
| | | | | -55°C to 25°C | | < 85°C | | < 125°C | | |
| | | | | Min | Max | Min | Max | Min | Max | |
| R_{ON} (NC, NO) | "ON" Resistance (Note 2) | $V_{IN} \geq V_{IH}$ $V_{IS} = \text{GND to } V_{CC}$ $ I_{IN} \leq 100 \text{ mA}$ | 2.5 | | 2.0 | | 2.0 | | 2.0 | Ω |
| | | | 3.0 | | 0.8 | | 0.8 | | 1.0 | |
| | | | 5.0 | | 0.8 | | 0.8 | | 0.9 | |
| R_{FLAT} (NC, NO) | On-Resistance Flatness (Notes 2, 4) | $I_{COM} = 100 \text{ mA}$ $V_{IS} = 0 \text{ to } V_{CC}$ | 2.5 | | 0.35 | | 0.35 | | 0.35 | Ω |
| | | | 3.0 | | 0.35 | | 0.35 | | 0.35 | |
| | | | 5.0 | | 0.35 | | 0.35 | | 0.35 | |
| ΔR_{ON} | On-Resistance Match Between Channels (Notes 2 and 3) | $V_{IS} = 1.3 \text{ V};$ $I_{COM} = 100 \text{ mA}$ $V_{IS} = 1.5 \text{ V};$ $I_{COM} = 100 \text{ mA}$ $V_{IS} = 2.8 \text{ V};$ $I_{COM} = 100 \text{ mA}$ | 2.5 | | 0.18 | | 0.18 | | 0.18 | Ω |
| | | | 3.0 | | 0.06 | | 0.06 | | 0.06 | |
| | | | 5.0 | | 0.06 | | 0.06 | | 0.06 | |
| $I_{NC(OFF)}$ $I_{NO(OFF)}$ | NC or NO Off Leakage Current (Figure 10) | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{NO} \text{ or } V_{NC} = 1.0$ $V_{COM} = 4.5 \text{ V}$ | 5.5 | -1 | 1 | -10 | 10 | -150 | 150 | nA |
| $I_{COM(ON)}$ | COM ON Leakage Current (Figure 10) | $V_{IN} = V_{IL} \text{ or } V_{IH}$ $V_{NO} 1.0 \text{ V or } 4.5 \text{ V with}$ $V_{NC} \text{ floating or}$ $V_{NC} 1.0 \text{ V or } 4.5 \text{ V with}$ $V_{NO} \text{ floating}$ $V_{COM} = 1.0 \text{ V or } 4.5 \text{ V}$ | 5.5 | -1 | 1 | -10 | 10 | -150 | 150 | nA |

2. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.
3. $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$ between all switches.
4. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

| Symbol | Parameter | Test Conditions | V_{CC} (V) | V_{IS} (V) | Guaranteed Maximum Limit | | | | | | Unit | |
|-----------|--------------------------------|--|-----------------|-----------------|--------------------------|------|-----|--------|-----|---------|------|-----|
| | | | | | -55°C to 25°C | | | < 85°C | | < 125°C | | |
| | | | | | Min | Typ* | Max | Min | Max | Min | | Max |
| t_{ON} | Turn-On Time | $R_L = 50 \Omega$, $C_L = 35$ pF (Figures 2 and 3) | 2.5 | 1.3 | | | 55 | | 65 | | 70 | ns |
| | | | 3.0 | 1.5 | | | 50 | | 60 | | 60 | |
| | | | 5.0 | 2.8 | | | 30 | | 35 | | 35 | |
| t_{OFF} | Turn-Off Time | $R_L = 50 \Omega$, $C_L = 35$ pF (Figures 2 and 3) | 2.5 | 1.3 | | | 55 | | 65 | | 70 | ns |
| | | | 3.0 | 1.5 | | | 50 | | 60 | | 60 | |
| | | | 5.0 | 2.8 | | | 25 | | 30 | | 30 | |
| t_{BBM} | Minimum Break-Before-Make Time | $V_{IS} = 3.0$ $R_L = 300 \Omega$, $C_L = 35$ pF (Figure 1) | 3.0 | 1.5 | 2 | 15 | | | | | | ns |

| | Parameter | Typical @ 25, $V_{CC} = 5.0$ V | $V_{CC} = 3.0$ V | Unit |
|--------------|---------------------------------|--------------------------------|---------------------------------|------|
| | | C_{NC} Off | NC Off Capacitance, $f = 1$ MHz | |
| C_{NO} Off | NO Off Capacitance, $f = 1$ MHz | | 102 | |
| C_{NC} On | NC On Capacitance, $f = 1$ MHz | | 547 | |
| C_{NO} On | NO On Capacitance, $f = 1$ MHz | | 431 | |

*Typical Characteristics are at 25°C.

ADDITIONAL APPLICATION CHARACTERISTICS (Voltages Referenced to GND Unless Noted) (Note 6)

| Symbol | Parameter | Condition | V_{CC} V | Typical | Unit |
|-----------|---|---|---------------|----------|------|
| | | | | 25°C | |
| BW | Maximum On-Channel -3dB Bandwidth or Minimum Frequency Response | $V_{IN} = 0$ dBm V_{IN} centered between V_{CC} and GND (Figure 4) | NC/NO 3.0 | 11.5 | MHz |
| V_{ONL} | Maximum Feed-through On Loss | $V_{IN} = 0$ dBm @ 100 kHz to 50 MHz V_{IN} centered between V_{CC} and GND (Figure 4) | 3.0 | -0.05 | dB |
| V_{ISO} | Off-Channel Isolation | $f = 100$ kHz; $V_{IS} = 1$ V RMS; $C_L = 5$ nF V_{IN} centered between V_{CC} and GND (Figure 4) | 3.0 | -65 | dB |
| Q | Charge Injection Select Input to Common I/O | $V_{IN} = V_{CC}$ to GND, $R_{IS} = 0 \Omega$, $C_L = 1$ nF $Q = C_L - \Delta V_{OUT}$ (Figure 5) | 3.0 5.0 | 15 20 | pC |
| THD | Total Harmonic Distortion THD + Noise | $F_{IS} = 20$ Hz to 20 kHz, $R_L = R_{gen} = 600 \Omega$, $C_L = 50$ pF $V_{IS} = 1$ V RMS | 3.0 | 0.14 | % |
| VCT | Channel-to-Channel Crosstalk | $f = 100$ kHz; $V_{IS} = 1$ V RMS, $C_L = 5$ pF, $R_L = 50 \Omega$ V_{IN} centered between V_{CC} and GND (Figure 4) | 3.0 | -81 | dB |

5. Off-Channel Isolation = $20 \log_{10} (V_{com}/V_{no})$, V_{com} = output, V_{no} = input to off switch.

6. -40°C specifications are guaranteed by design.

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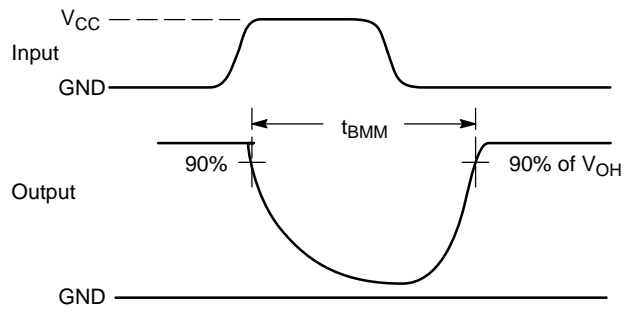
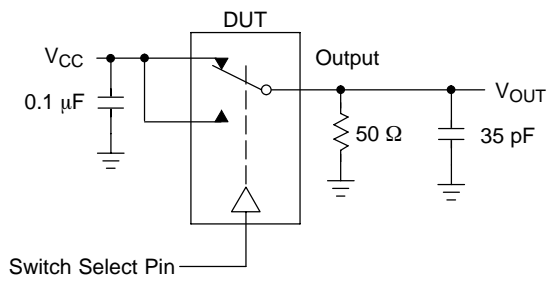


Figure 1. t_{BMM} (Time Break-Before-Make)

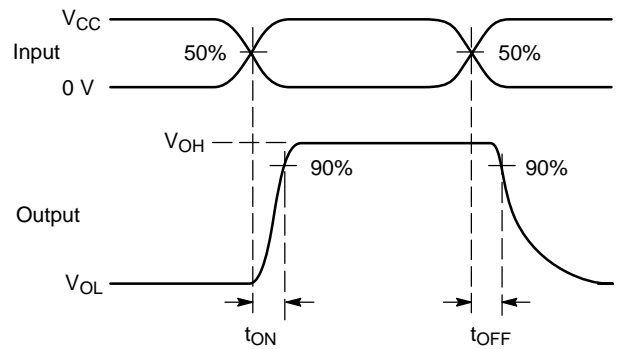
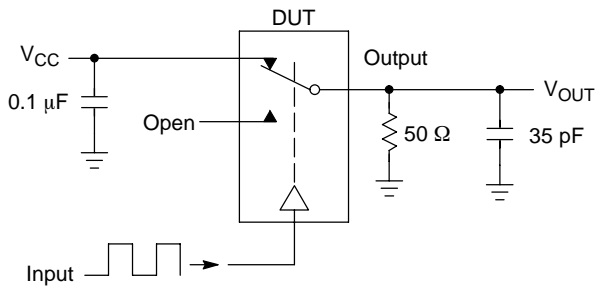


Figure 2. t_{ON}/t_{OFF}

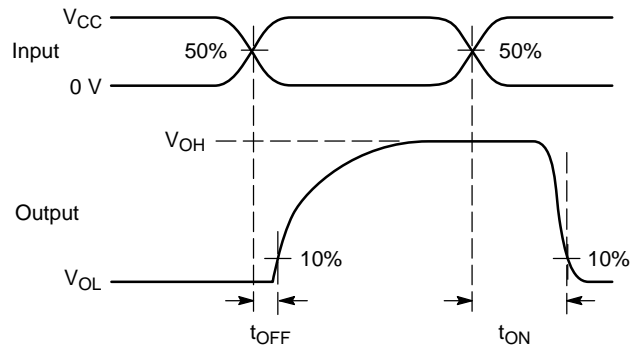
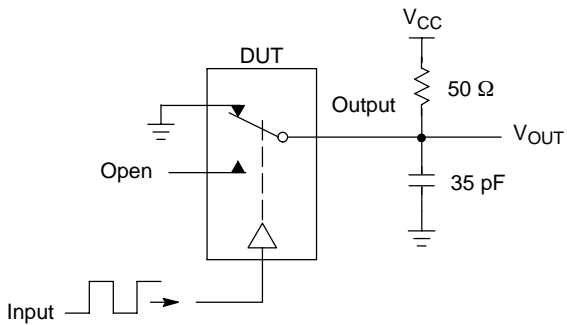
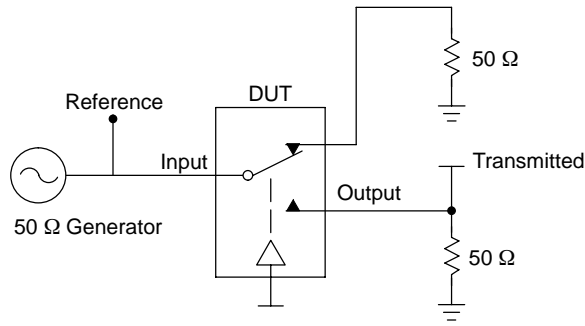


Figure 3. t_{ON}/t_{OFF}

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Channel switch control/s test socket is normalized. Off isolation is measured across an off channel. On loss is the bandwidth of an On switch. V_{ISO} , Bandwidth and V_{ONL} are independent of the input signal direction.

$$V_{ISO} = \text{Off Channel Isolation} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz}$$

$$V_{ONL} = \text{On Channel Loss} = 20 \text{ Log} \left(\frac{V_{OUT}}{V_{IN}} \right) \text{ for } V_{IN} \text{ at } 100 \text{ kHz to } 50 \text{ MHz}$$

Bandwidth (BW) = the frequency 3 dB below V_{ONL}

V_{CT} = Use V_{ISO} setup and test to all other switch analog input/outputs terminated with 50 Ω

Figure 4. Off Channel Isolation/On Channel Loss (BW)/Crosstalk (On Channel to Off Channel)/ V_{ONL}

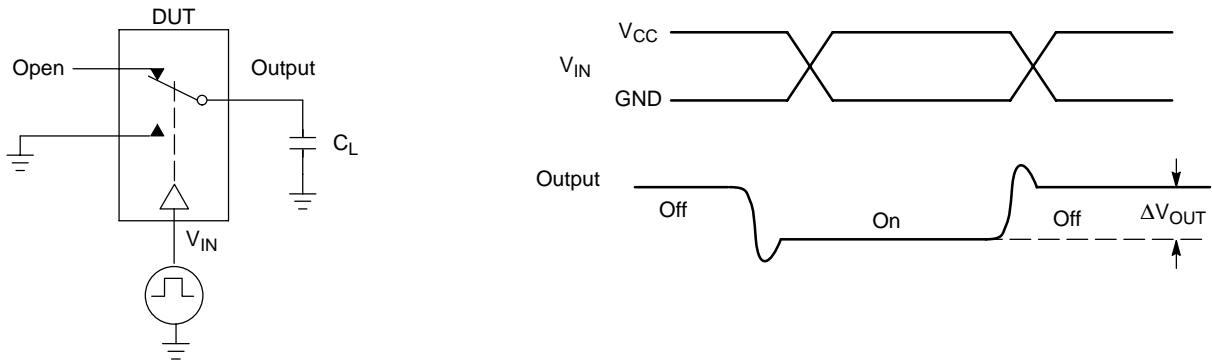


Figure 5. Charge Injection: (Q)

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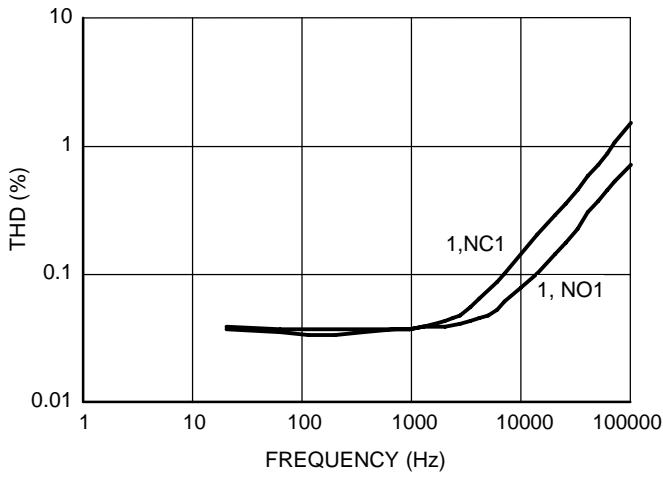


Figure 6. Total Harmonic Distortion Plus Noise versus Frequency

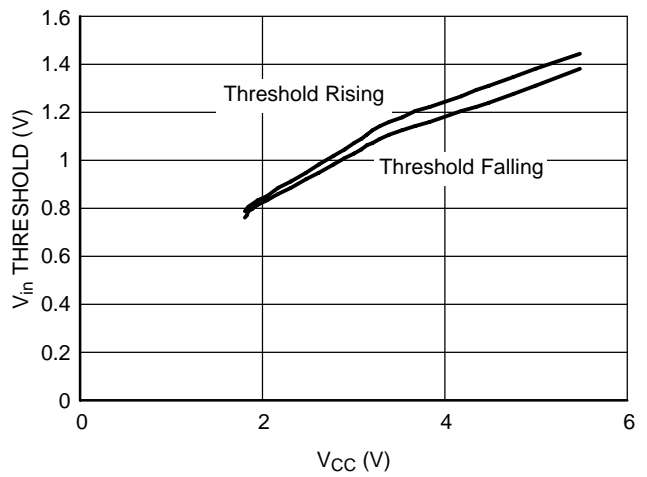


Figure 7. Voltage in Threshold on Logic Pins

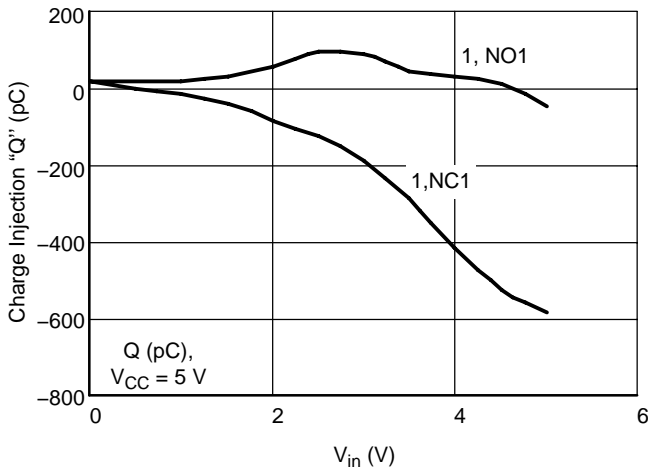


Figure 8. Charge Injection versus V_{is}

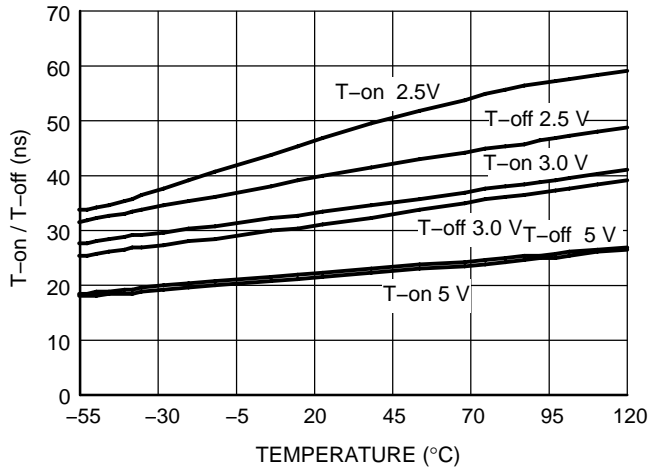


Figure 9. T-on/T-off Time versus Temperature

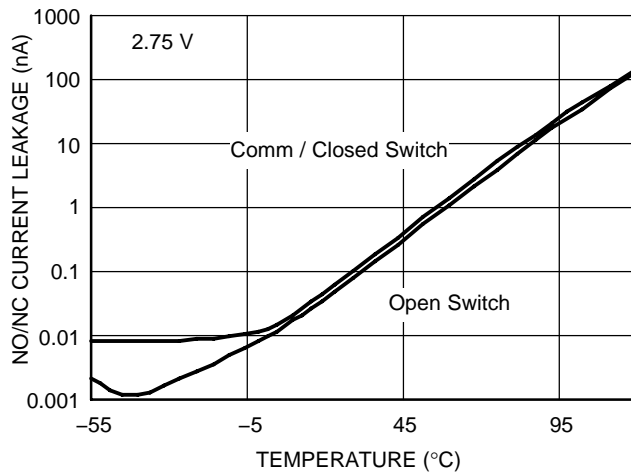


Figure 10. NO/NC Current Leakage Off and On, $V_{CC} = 5 V$

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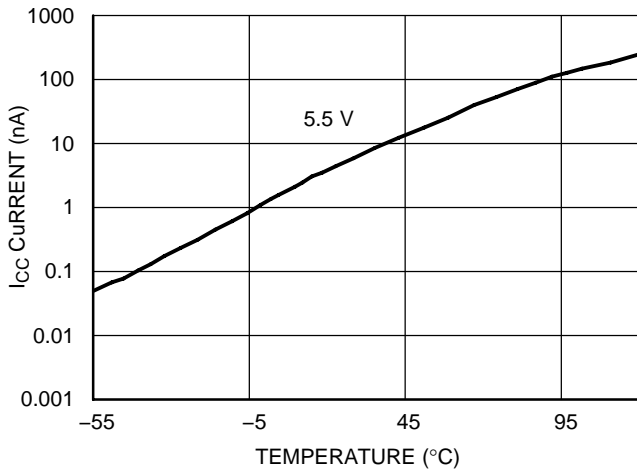


Figure 11. I_{CC} Current Leakage versus Temperature $V_{CC} = 5.5 V$

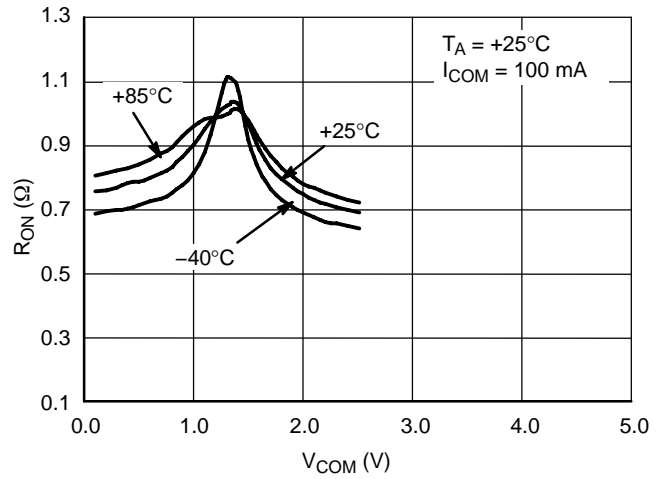


Figure 12. NC/NO On-Resistance versus COM Voltage

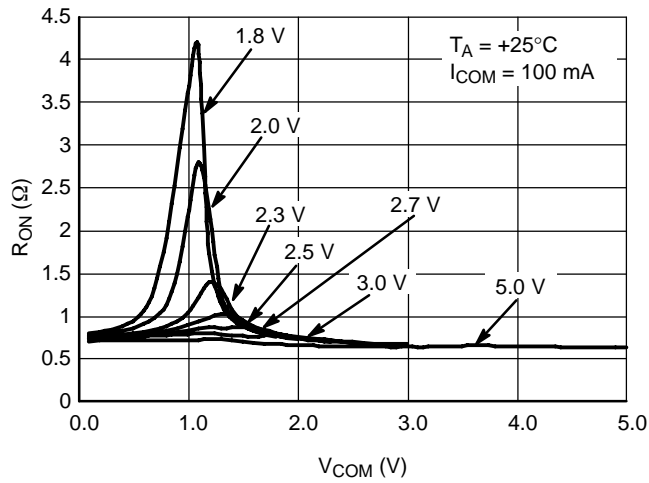


Figure 13. NC/NO On-Resistance versus COM Voltage

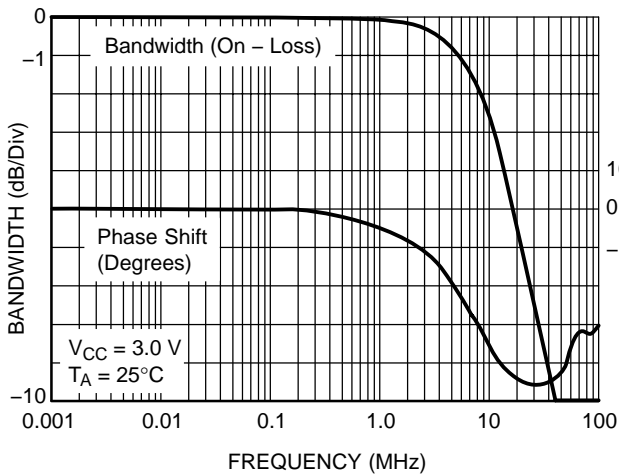


Figure 14. NC/NO Bandwidth and Phase Shift versus Frequency

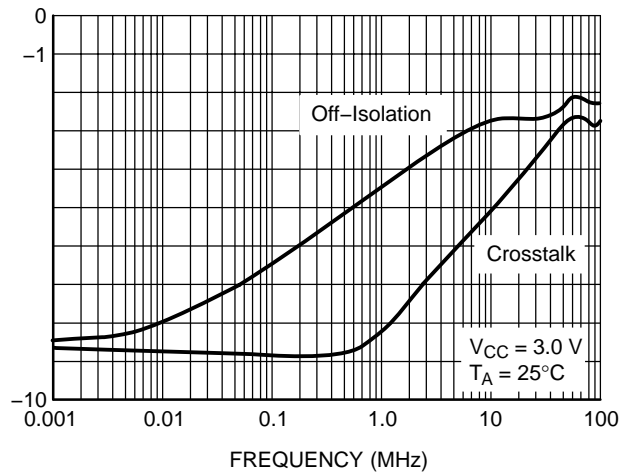


Figure 15. NC/NO Off Isolation and Crosstalk

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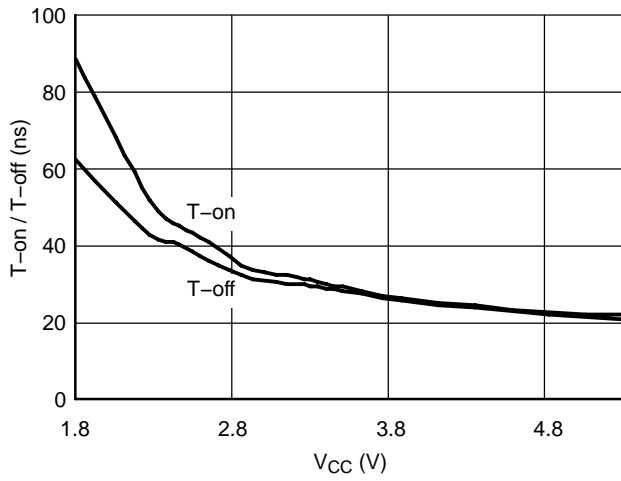


Figure 16. T-on/T-off versus V_{CC}

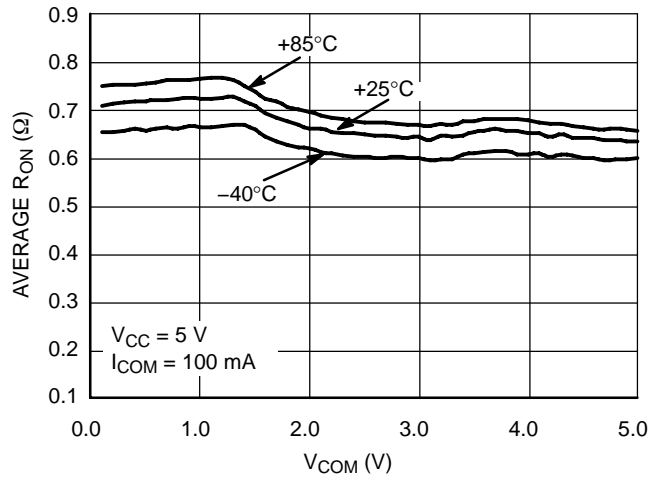


Figure 17. NC/NO On-Resistance versus COM Voltage

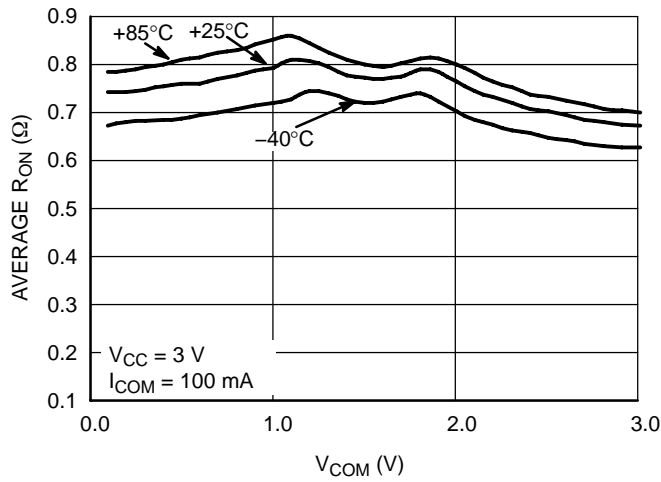


Figure 18. NC/NO On-Resistance versus COM Voltage

MECHANICAL CASE OUTLINE

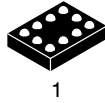
PACKAGE DIMENSIONS

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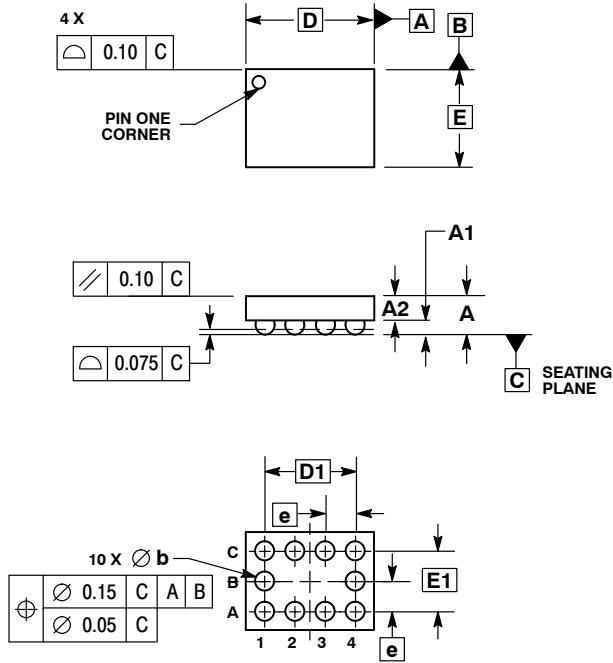
10 PIN FLIP-CHIP CASE 489AA-01 ISSUE A

DATE 04 MAY 2004



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SCALE 4:1

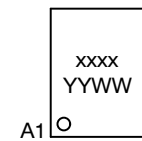


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | --- | 0.650 |
| A1 | 0.210 | 0.270 |
| A2 | 0.280 | 0.380 |
| D | 1.965 BSC | |
| E | 1.465 BSC | |
| b | 0.250 | 0.350 |
| e | 0.500 BSC | |
| D1 | 1.500 BSC | |
| E1 | 1.000 BSC | |

GENERIC MARKING DIAGRAM*



- xxxx = Specific Device Code
- YY = Year
- WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
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