4007UB

DUAL COMPLEMENTARY PAIR PLUS INVERTER

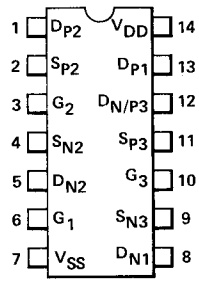
DESCRIPTION – The 4007UB is a Dual Complementary Pair and an Inverter with access to each device. It has three n-channel and three p-channel enhancement mode MOS transistors. For proper operation $V_{SS} \leq V_1 \leq V_{DD}$.

- **INPUT DIODE PROTECTION ON ALL INPUTS**
- **DRAINS AND SOURCES TO N- AND P-CHANNEL TRANSISTORS AVAILABLE**

PIN NAMES

S_{P2}, S_{P3}	Source Connection to Second and Third p-channel Transistors
D_{P1}, D_{P2}	Drain Connection from the First and Second p-channel Transistors
D_{N1}, D_{N2}	Drain Connection from the First and Second n-channel Transistors
S_{N2}, S_{N3}	Source Connection to the Second and Third n-channel Transistors
$D_{N/P3}$	Common Connection to the Third p-channel and n-channel Transistor Drains
G_1-G_3	Gate Connection to n- and p-channel Transistors 1, 2 and 3

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

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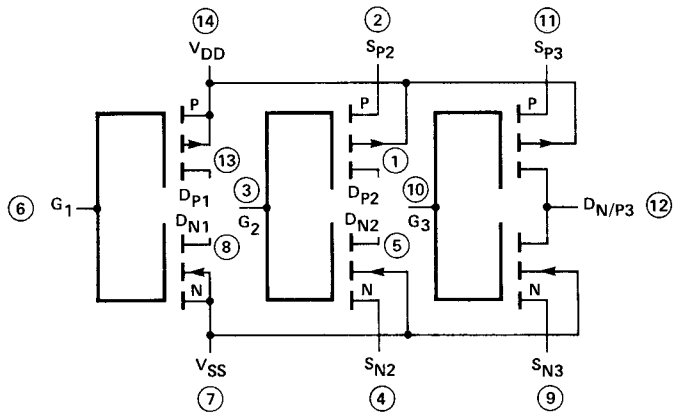
LOGIC SYMBOL



DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

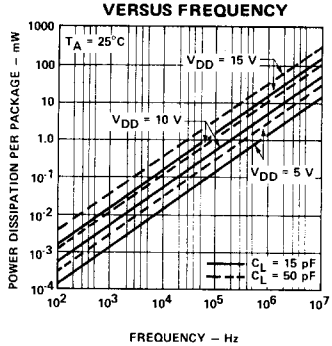
SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			1 7.5			2 15			4 30	μA	MIN, 25°C MAX	All inputs at 0 V or V_{DD}
		XM			0.25 7.5			0.5 15			1 30	μA	MIN, 25°C MAX	

AC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

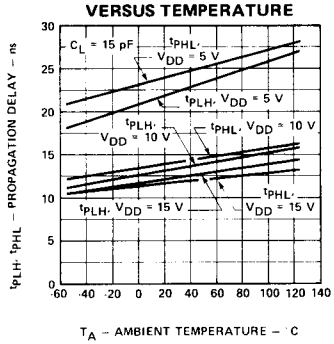
SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay		42	85		23	40		18	32	ns	C_L = 50 pF,
t_{PHL}			42	85		23	40		18	32	ns	R_L = 200 kΩ
t_{TLH}	Output Transition Time		65	135		30	70		25	45	ns	Input Transition
t_{THL}			65	135		30	70		25	45	ns	Times ≤ 20 ns

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.

POWER DISSIPATION VERSUS FREQUENCY



PROPAGATION DELAY VERSUS TEMPERATURE



PROPAGATION DELAY VERSUS LOAD CAPACITANCE