

## Description

The AP2151A is an integrated high-side power switches optimized for Universal Serial Bus (USB) and other hot-swap applications. The family of devices complies with USB 2.0 and is available with active high Enable input. They offer current and thermal limiting and short circuit protection as well as controlled rise time and under-voltage lockout functionality. A 7ms deglitch capability on the open-drain Flag output prevents false over-current reporting and does not require any external components.

AP2151A is available in SO-8, MSOP-8EP, SOT25 and U-DFN2018-6 packages.

## Features

- Single USB Port Power Switches
- Over-Current and Thermal Protection
- 0.8A Accurate Current Limiting
- Reverse Current Blocking
- 95mΩ On-Resistance
- Input Voltage Range: 2.7V to 5.5V
- 0.6ms Typical Rise Time
- Very Low Shutdown Current: 1μA (Max)
- Fault Report (FLG) with Blanking Time (7ms Typ)
- ESD Protection: 4kV HBM, 400V MM
- Active High Enable
- Ambient Temperature Range -40°C to +85°C
- SOT25, SO-8, MSOP-8EP (Exposed Pad) and U-DFN2018-6: Available in "Green" Molding Compound (No Br, Sb)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- 15kV ESD Protection per IEC 61000-4-2 (With External Capacitance)
- UL Recognized, File Number E322375
- IEC60950-1 CB Scheme Certified

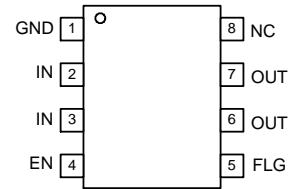
## Applications

- Consumer Electronics – LCD TVs & Monitors, Game Machines
- Communications – Set-Top-Boxes, GPS Systems, Smartphones
- Computing – Laptops, Desktops, Servers, Printers, Docking Stations, HUBs

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

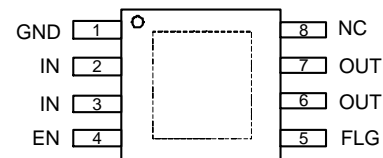
## Pin Assignments

(Top View)



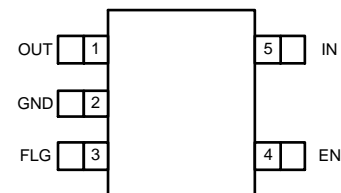
SO-8

(Top View)



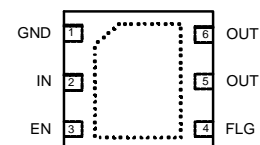
MSOP-8EP

(Top View)



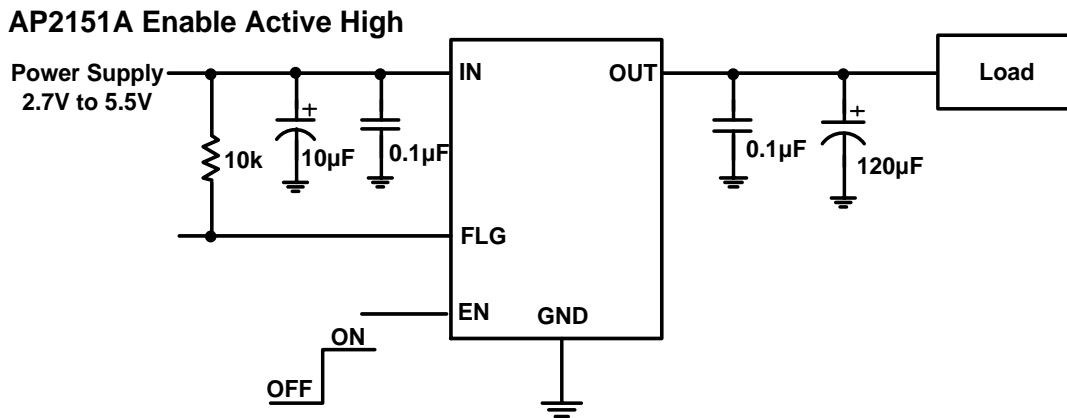
SOT25

(Top View)



U-DFN2018-6

**Typical Applications Circuit**

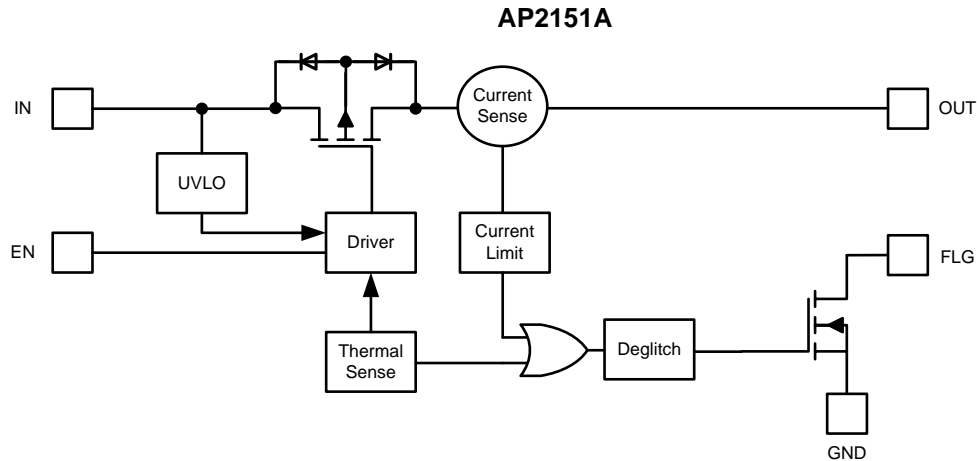


**Available Options**

| Part Number | Channel | Enable Pin (EN) | Current Limit (Typical) | Recommended Maximum Continuous Load Current |
|-------------|---------|-----------------|-------------------------|---|
| AP2151A     | 1       | Active High     | 0.8A                    | 0.5A  |

**Pin Descriptions**

| Pin Name    | Pin Number |             |       |             | Function   |
|-------------|------------|-------------|-------|-------------|--|
|             | SO-8       | MSOP-8EP    | SOT25 | U-DFN2018-6 |  |
| GND         | 1          | 1           | 2     | 1           | Ground   |
| IN          | 2, 3       | 2, 3        | 5     | 2           | Voltage Input Pin (all IN pins must be tied together externally).  |
| EN          | 4          | 4           | 4     | 3           | Enable Input. Active High (AP2151A).   |
| FLG         | 5          | 5           | 3     | 4           | Over-Current and Over-Temperature Fault Report. Open-Drain Flag is Active Low When Triggered   |
| OUT         | 6, 7       | 6, 7        | 1     | 5, 6        | Voltage Output Pin (all OUT pins must be tied together externally).  |
| NC          | 8          | 8           | N/A   | N/A         | No internal connection; recommend tie to OUT pins  |
| Exposed Pad | —          | Exposed Pad | —     | Exposed Pad | Exposed Pad. It should be externally connected to GND plane and thermal mass for enhanced thermal impedance. It should not be used as electrical ground conduction path. |

**Functional Block Diagram**

**Absolute Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

| Symbol   | Parameter                          |  | Ratings              | Unit |
|--|------------------------------------|--|----------------------|------|
| ESD  | HBM                                | Human Body Model ESD Protection  | 4                    | kV   |
|  | MM                                 | Machine Model ESD Protection for SO-8, MSOP-8EP, SOT25 packages          | 400                  | V    |
|  | MM                                 | Machine Model ESD Protection for U-DFN2018-6, SO-8 packages              | 300                  | V    |
|  | IEC system level                   | Surges per EN61000-4-2. 1999 applied to output terminals of EVM (Note 5) | Air                  | 15   |
| Surges per EN61000-4-2. 1999 applied to output terminals of EVM (Note 5) |                                    | Contact  | 8                    | kV   |
| V <sub>IN</sub>  | Input Voltage                      |  | 6.5                  | V    |
| V <sub>OUT</sub>   | Output Voltage                     |  | V <sub>IN</sub> +0.3 | V    |
| V <sub>EN</sub> , V <sub>FLG</sub>                                       | Enable Voltage                     |  | 6.5                  | V    |
| I <sub>LOAD</sub>  | Maximum Continuous Load Current    |  | Internal Limited     | A    |
| T <sub>J(MAX)</sub>  | Maximum Junction Temperature       |  | +150                 | °C   |
| T <sub>ST</sub>  | Storage Temperature Range (Note 4) |  | -65 to +150          | °C   |

Caution: Stresses greater than the 'Absolute Maximum Ratings' specified above, may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Notes:  
 4. UL Recognized Rating from -30°C to +70°C (Diodes Incorporated qualified T<sub>ST</sub> from -65°C to +150°C).  
 5. External capacitors need to be connected to the output, EVM board was tested with capacitor 2.2µF 50V 0805. This level is a pass test only and not a limit.

**Recommended Operating Conditions** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

| Symbol           | Parameter                     | Min | Max             | Unit |
|------------------|-------------------------------|-----|-----------------|------|
| V <sub>IN</sub>  | Input Voltage                 | 2.7 | 5.5             | V    |
| I <sub>OUT</sub> | Output Current                | 0   | 500             | mA   |
| T <sub>A</sub>   | Operating Ambient Temperature | -40 | +85             | °C   |
| V <sub>IL</sub>  | EN Input Logic Low Voltage    | 0   | 0.8             | V    |
| V <sub>IH</sub>  | EN Input Logic High Voltage   | 2   | V <sub>IN</sub> | V    |

**Electrical Characteristics** (@ $T_A = +25^\circ\text{C}$ ,  $V_{IN} = +5.0\text{V}$ , unless otherwise specified.)

| Symbol        | Parameter                              | Conditions   | Min   | Typ                   | Max | Unit                      |     |            |
|---------------|--|--|---|-----------------------|-----|---------------------------|-----|------------|
| $V_{UVLO}$    | Input UVLO                             | $R_{LOAD} = 1\text{k}\Omega$   | 1.6   | 1.9                   | 2.5 | V                         |     |            |
| $I_{SHDN}$    | Input Shutdown Current                 | Disabled, $I_{OUT} = 0$  | —   | 0.5                   | 1   | $\mu\text{A}$             |     |            |
| $I_Q$         | Input Quiescent Current                | Enabled, $I_{OUT} = 0$   | —   | 45                    | 70  | $\mu\text{A}$             |     |            |
| $I_{LEAK}$    | Input Leakage Current                  | Disabled, OUT grounded   | —   | —                     | 1   | $\mu\text{A}$             |     |            |
| $I_{REV}$     | Reverse Leakage Current                | Disabled, $V_{IN} = 0\text{V}$ , $V_{OUT} = 5\text{V}$ , $I_{REV}$ at $V_{IN}$   | —   | 1                     | —   | $\mu\text{A}$             |     |            |
| $R_{DS(ON)}$  | Switch On-Resistance                   | $V_{IN} = 5\text{V}$ ,<br>$I_{OUT} = 0.5\text{A}$  | $T_A = +25^\circ\text{C}$                           | SOT25, SO-8, MSOP-8EP | —   | 95                        | 115 | m $\Omega$ |
|               |  |  | $T_A = +25^\circ\text{C}$                           | U-DFN2018-6           | —   | 90                        | 110 |            |
|               |  | $V_{IN} = 3.3\text{V}$ ,<br>$I_{OUT} = 0.5\text{A}$  | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ | —                     | —   | 140                       | —   |            |
|               |  |  | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ | —                     | —   | 170                       |     |            |
| $I_{SHORT}$   | Short-Circuit Current Limit            | Enabled into short circuit, $C_L = 22\mu\text{F}$  | —   | 0.6                   | —   | A                         |     |            |
| $I_{LIMIT}$   | Over-Load Current Limit                | $V_{IN} = 5\text{V}$ , $V_{OUT} = 4.8\text{V}$ , $C_L = 22\mu\text{F}$ , $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ | 0.6   | 0.8                   | 1.0 | A                         |     |            |
| $I_{TRIG}$    | Current Limiting Trigger Threshold     | Output Current Slew Rate (<100A/s), $C_L = 22\mu\text{F}$  | —   | 1.0                   | —   | A                         |     |            |
| $I_{SINK}$    | EN Input Leakage                       | $V_{EN} = 5\text{V}$   | —   | —                     | 1   | $\mu\text{A}$             |     |            |
| $t_{D(ON)}$   | Output Turn-On Delay Time              | $C_L = 1\mu\text{F}$ , $R_{LOAD} = 10\Omega$   | —   | 0.05                  | —   | ms                        |     |            |
| $t_R$         | Output Turn-On Rise Time               | $C_L = 1\mu\text{F}$ , $R_{LOAD} = 10\Omega$   | —   | 0.6                   | 1.5 | ms                        |     |            |
| $t_{D(OFF)}$  | Output Turn-Off delay Time             | $C_L = 1\mu\text{F}$ , $R_{LOAD} = 10\Omega$   | —   | 0.01                  | —   | ms                        |     |            |
| $t_F$         | Output Turn-Off Fall Time              | $C_L = 1\mu\text{F}$ , $R_{LOAD} = 10\Omega$   | —   | 0.05                  | 0.1 | ms                        |     |            |
| $R_{FLG}$     | FLG Output FET On-Resistance           | $I_{FLG} = 10\text{mA}$  | —   | 20                    | 40  | $\Omega$                  |     |            |
| $t_{BLANK}$   | FLG Blanking Time                      | $C_{IN} = 10\mu\text{F}$ , $C_L = 22\mu\text{F}$   | 4   | 7                     | 15  | ms                        |     |            |
| $T_{SHDN}$    | Thermal Shutdown Threshold             | Enabled, $R_{LOAD} = 1\text{k}\Omega$  | —   | +140                  | —   | $^\circ\text{C}$          |     |            |
| $T_{HYS}$     | Thermal Shutdown Hysteresis            | —  | —   | +25                   | —   | $^\circ\text{C}$          |     |            |
| $\theta_{JA}$ | Thermal Resistance Junction-to-Ambient | SO-8 (Note 6)  | —   | 110                   | —   | $^\circ\text{C}/\text{W}$ |     |            |
|               |  | MSOP-8EP (Note 7)  | —   | 60                    | —   | $^\circ\text{C}/\text{W}$ |     |            |
|               |  | SOT25 (Note 8)   | —   | 157                   | —   | $^\circ\text{C}/\text{W}$ |     |            |
|               |  | U-DFN2018-6 (Note 9)   | —   | 70                    | —   | $^\circ\text{C}/\text{W}$ |     |            |

- Notes:
6. Test condition for SO-8: Device mounted on FR-4, 2oz copper, with minimum recommended pad layout.
  7. Test condition for SO-8, MSOP-8EP: Device mounted on 2" x 2" FR-4 substrate PC board, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.
  8. Test condition for SOT25: Device mounted on FR-4, 2oz copper, with minimum recommended pad layout.
  9. Test condition for U-DFN2018-6: Device mounted on FR-4 2-layer board, 2oz copper, with minimum recommended pad on top layer and 3 vias to bottom layer 1.0" x 1.4" ground plane.

**Typical Performance Characteristics**

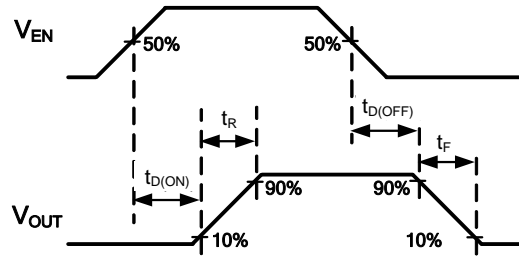
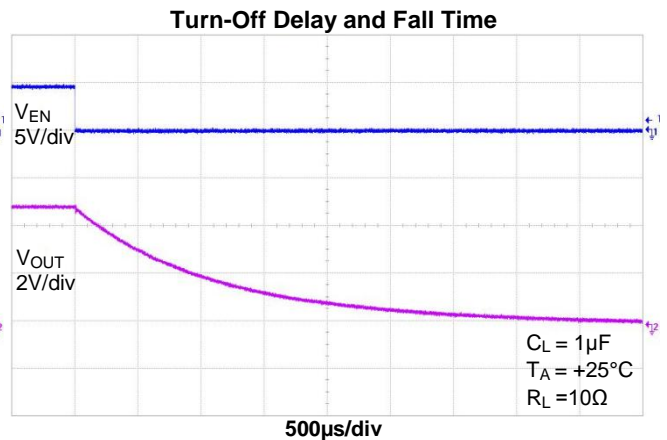
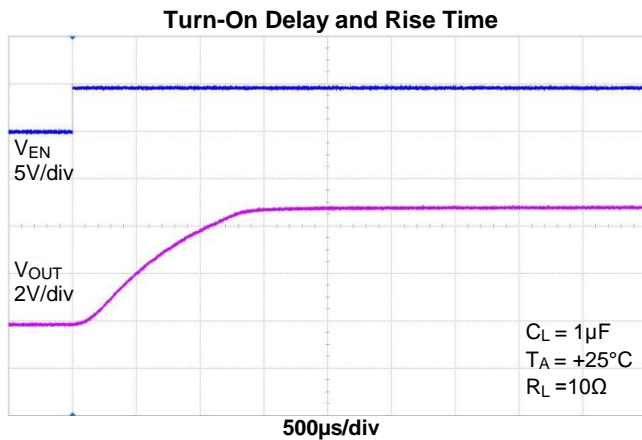
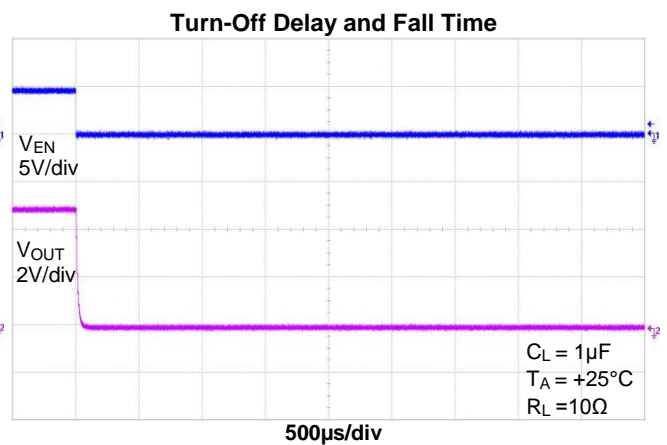
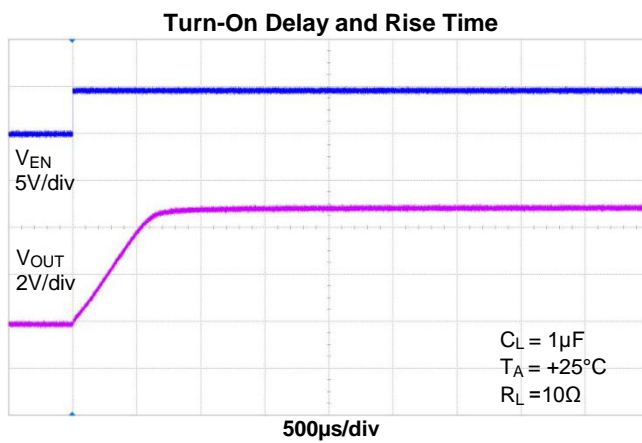
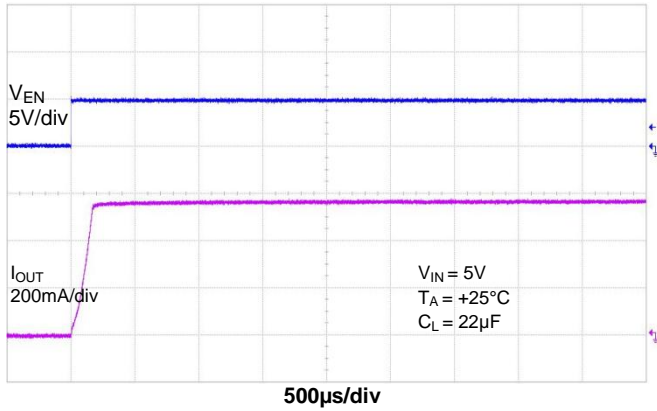


Figure 1. Voltage Waveforms: AP2151A  
All Enable Plots are for AP2151A Active High

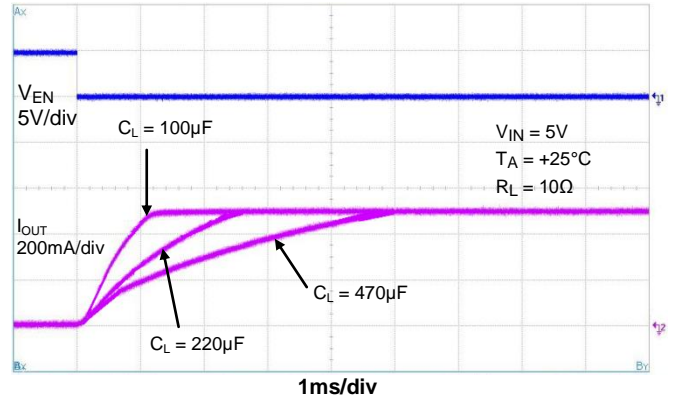


**Typical Performance Characteristics (Cont.)**

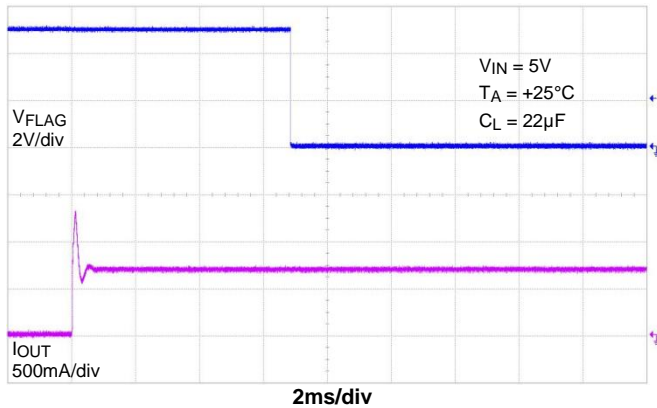
**Short Circuit Current, Device Enabled Into Short**



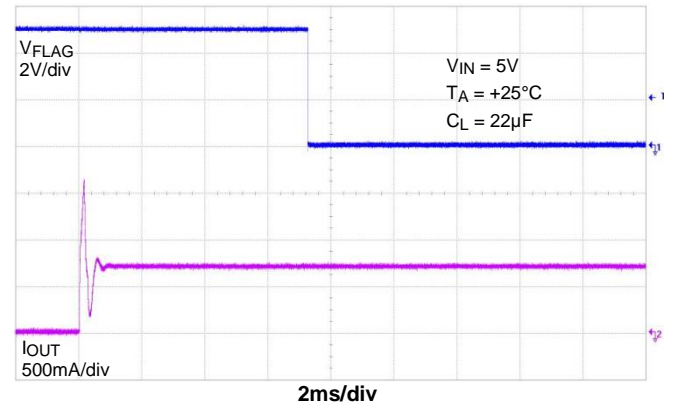
**Inrush Current**



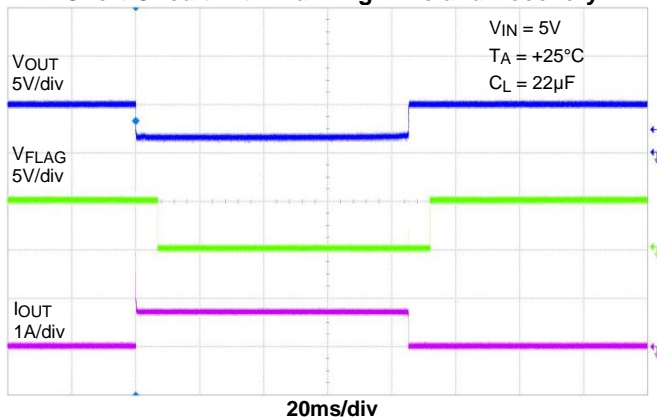
**3Ω Load Connected to Enabled Device**



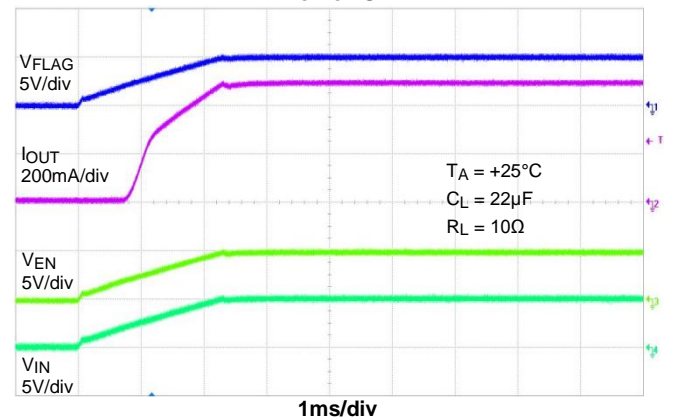
**2Ω Load Connected to Enabled Device**



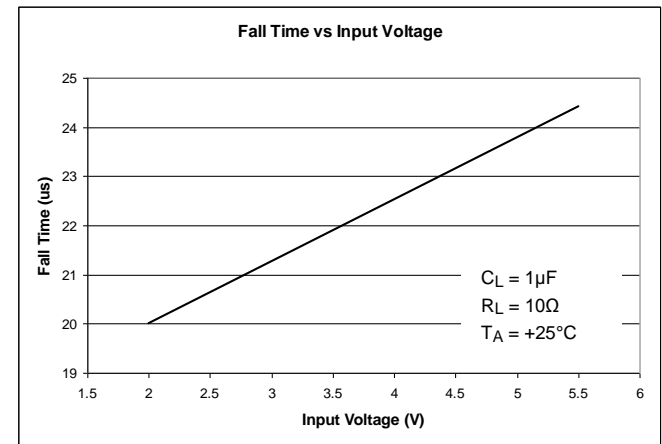
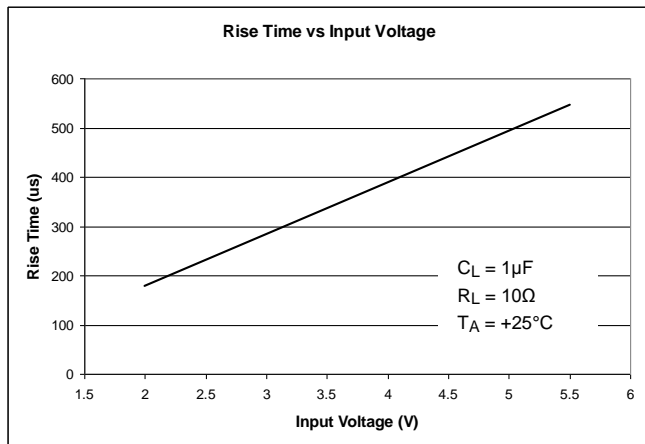
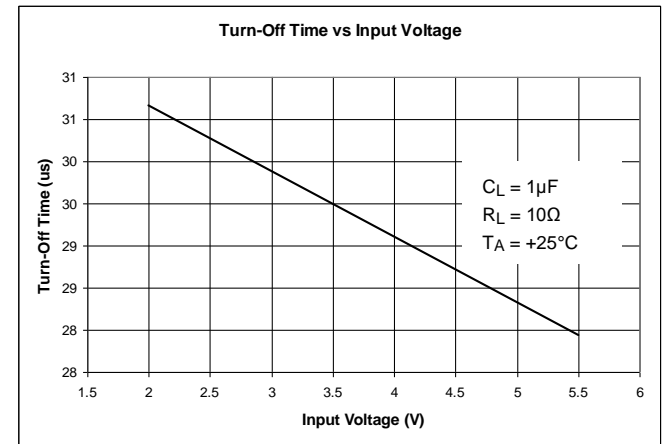
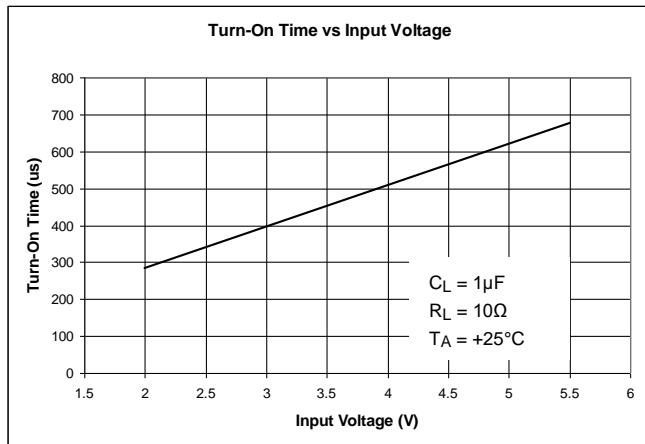
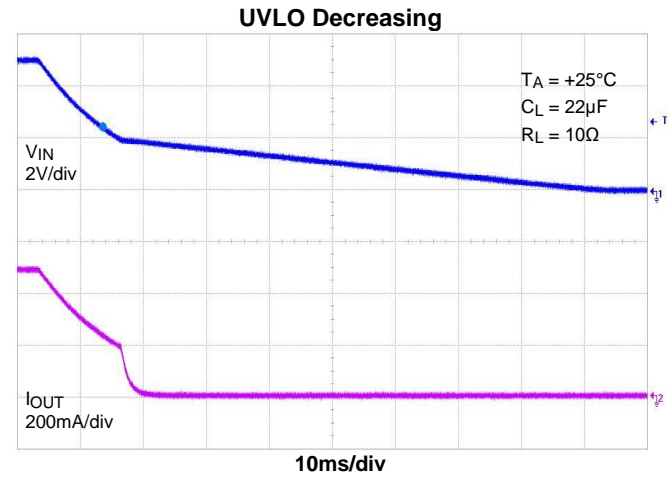
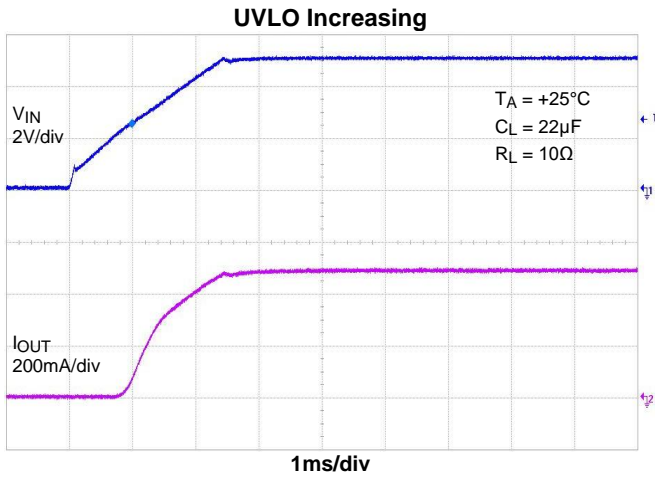
**Short Circuit with Blanking Time and Recovery**



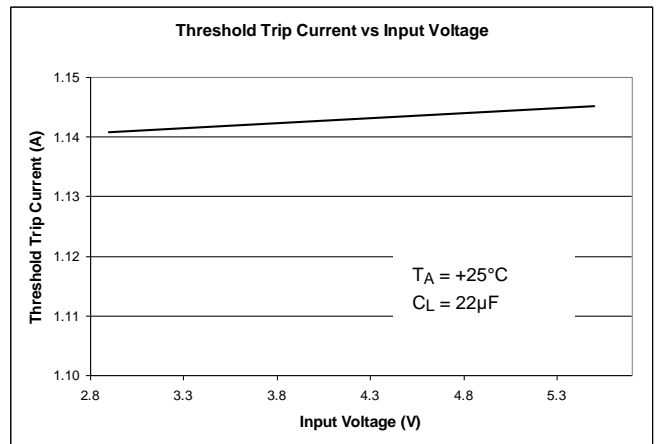
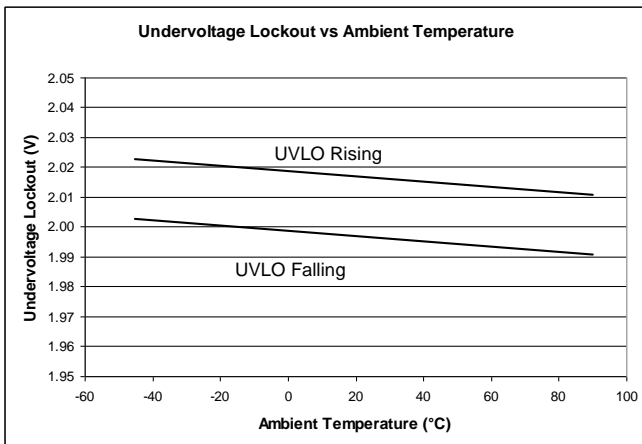
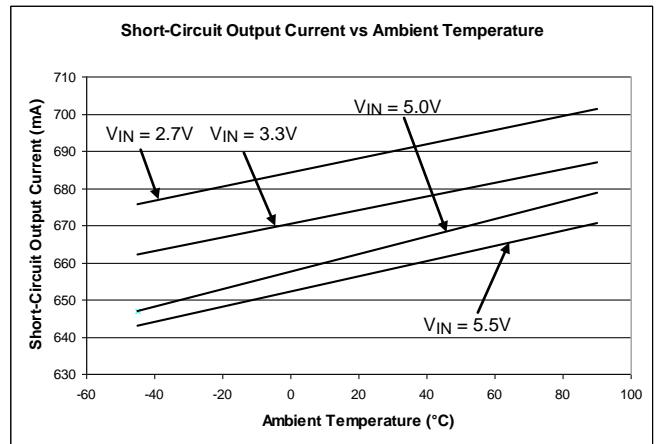
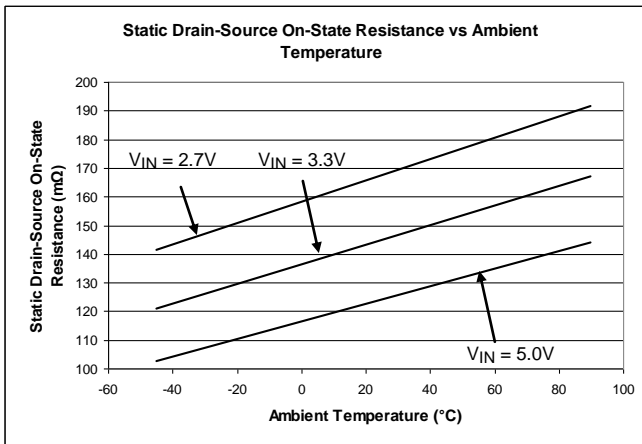
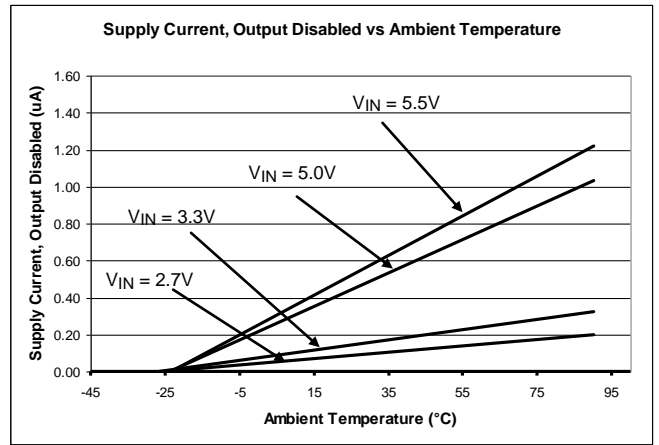
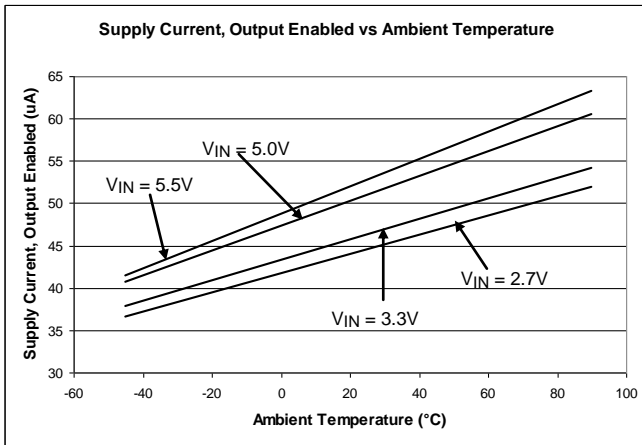
**Power On**



**Typical Performance Characteristics (Cont.)**

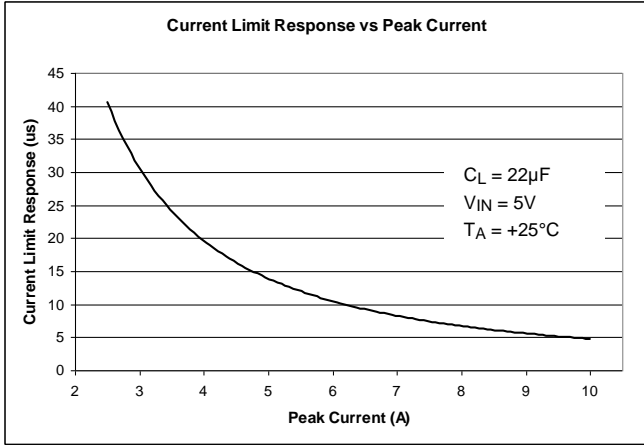


**Typical Performance Characteristics (Cont.)**





**Typical Performance Characteristics** (Cont.)



## Application Information

### Power Supply Considerations

A 0.01 $\mu$ F to 0.1 $\mu$ F X7R or X5R ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the input (10 $\mu$ F minimum) and output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01 $\mu$ F to 0.1 $\mu$ F ceramic capacitor improves the immunity of the device to short-circuit transients.

### Over-current and Short Circuit Protection

An internal sensing FET is employed to check for over-current conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault stays long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted to GND before the device is enabled or before  $V_{IN}$  has been applied. The AP2151A senses the short circuit and immediately clamps output current to a certain safe level namely  $I_{LIMIT}$ .

In the second condition, an output short or an overload occurs while the device is enabled. At the instance the overload occurs, higher current may flow for a very short period of time before the current limit function can react. After the current limit function has tripped (reached the over-current trip threshold), the device switches into current limiting mode and the current is clamped at  $I_{LIMIT}$ .

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold ( $I_{TRIG}$ ) is reached or until the thermal limit of the device is exceeded. The AP2151A is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its current limiting mode and is set at  $I_{LIMIT}$ .

Note that when the output has been shorted to GND at an extremely low temperature (< -30°C), a minimum 120- $\mu$ F electrolytic capacitor on the output pin is recommended. A correct capacitor type with capacitor voltage rating and temperature characteristics must be properly chosen so that capacitance value does not drop too low at the extremely low temperature operation. A recommended capacitor should have temperature characteristics of less than a 10% variation of capacitance change when operated at extremely low temperatures. Our recommended aluminum electrolytic capacitor type is Panasonic FC series.

### FLG Response

When an over-current or over-temperature shutdown condition is encountered, the FLG open-drain output goes active low after a nominal 7ms deglitch timeout. The FLG output remains low until both over-current and over-temperature conditions are removed. Connecting a heavy capacitive load to the output of the device can cause a momentary over-current condition, which does not trigger the FLG due to the 7ms deglitch timeout. The AP2151A is designed to eliminate false over-current reporting without the need of external components to remove unwanted pulses.

### Power Dissipation and Junction Temperature

The low on-resistance of the internal MOSFET allows the small surface-mount packages to pass large current. Using the maximum operating ambient temperature ( $T_A$ ) and  $R_{DS(ON)}$ , the power dissipation can be calculated by:

$$P_D = R_{DS(ON)} \times I^2$$

Finally, calculate the junction temperature:

$$T_J = P_D \times R_{\theta JA} + T_A$$

Where:

$T_A$  = Ambient Temperature °C

$R_{\theta JA}$  = Thermal Resistance

$P_D$  = Total Power Dissipation

**Application Information (Cont.)**

**Thermal Protection**

Thermal protection prevents the IC from damage when heavy-overload or short-circuit faults are present for extended periods of time. The AP2151A implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. Once the die temperature rises to approximately +140°C due to excessive power dissipation in an over-current or short-circuit condition the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit allowing the device to cool down approximately +25°C before the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The FLG open-drain output is asserted when an over-temperature shutdown or over-current occurs with 7ms deglitch.

**Under-Voltage Lockout (UVLO)**

Under-voltage lockout function (UVLO) keeps the internal power switch from being turned on until the power supply has reached at least 1.9V, even if the switch is enabled. Whenever the input voltage falls below approximately 1.9V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed.

**Host/Self-Powered HUBs**

Hosts and self-powered hubs (SPH) have a local power supply that powers the embedded functions and the downstream ports (see Figure 2). This power supply must provide from 5.25V to 4.75V to the board side of the downstream connection under both full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report over-current conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

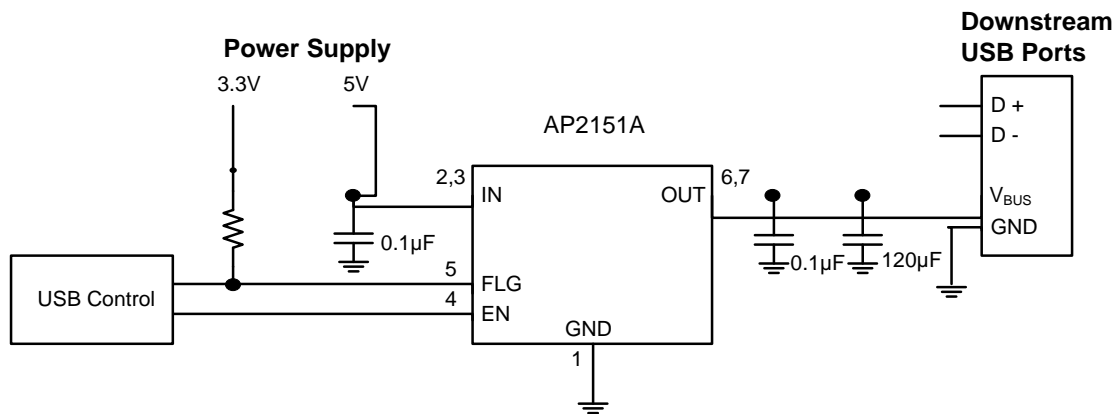


Figure 2. Typical One-Port USB Host / Self-Powered Hub

**Generic Hot-Plug Applications**

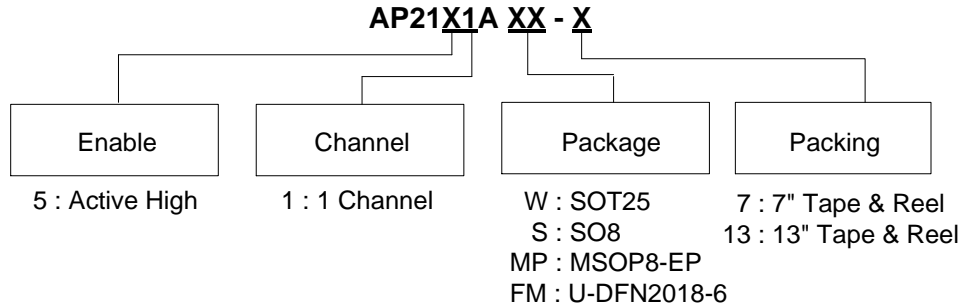
In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the AP2151A, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the AP2151A also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion.

By placing the AP2151A between the V<sub>CC</sub> input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge current and provides a hot-plugging mechanism for any device.

**Dual-Purpose Port Applications**

AP2151A is suitable for use in dual-purpose port applications in which a single port is used for data communication between the host and peripheral devices while simultaneously maintaining a charge to the battery of the peripheral device. An example of this is a shared HDMI/MHL (Mobile High-definition Link) port that allows streaming video between an HDTV or set-top box and a smartphone or tablet while maintaining a charge to the smartphone or tablet battery. In such dual-purpose port applications, it is important to insure Vin of the AP2151A is ramped to its operating voltage prior to enabling the output.

## Ordering Information

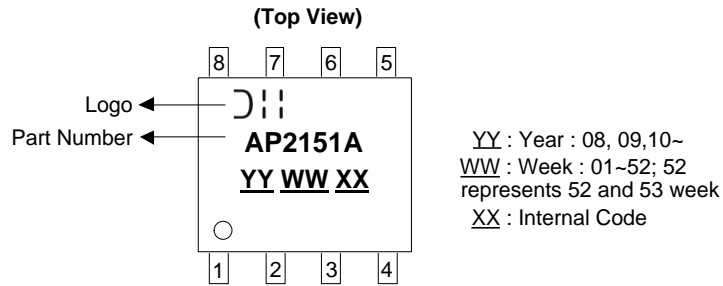


| Part Number  | Package (Note 11) | Package Code | 7"/13" Tape and Reel Quantity | Status (Note 10) |
|--------------|-------------------|--------------|-------------------------------|------------------|
| AP2151AW-7   | SOT25             | W            | 3000                          | In Production    |
| AP2151AS-13  | SO-8              | S            | 2500                          | In Production    |
| AP2151AMP-13 | MSOP-8EP          | MP           | 2500                          | In Production    |
| AP2151AFM-7  | U-DFN2018-6       | FM           | 3000                          | In Production    |

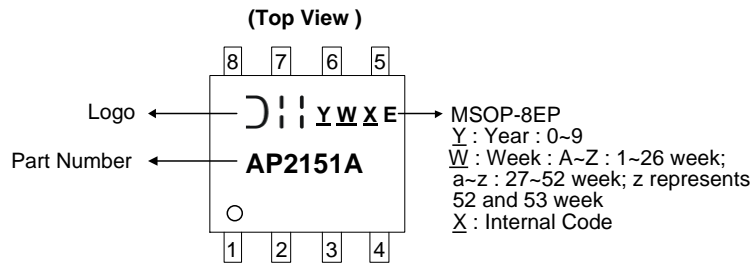
Notes: 10. All variants of AP2141A are End of Life and recommended alternatives are AP2141.  
 11. For packaging details, go to our website at: <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information

### (1) SO-8

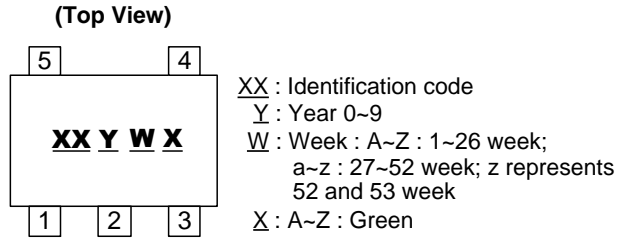


### (2) MSOP-8EP



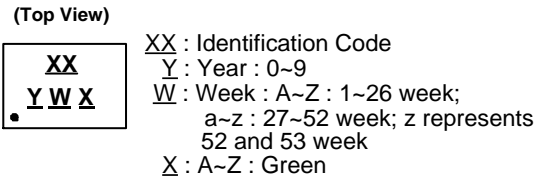
**Marking Information** (Cont.)

(3) SOT25



| Device   | Package Type | Identification Code |
|----------|--------------|---------------------|
| AP2151AW | SOT25        | VU                  |

(4) U-DFN2018-6

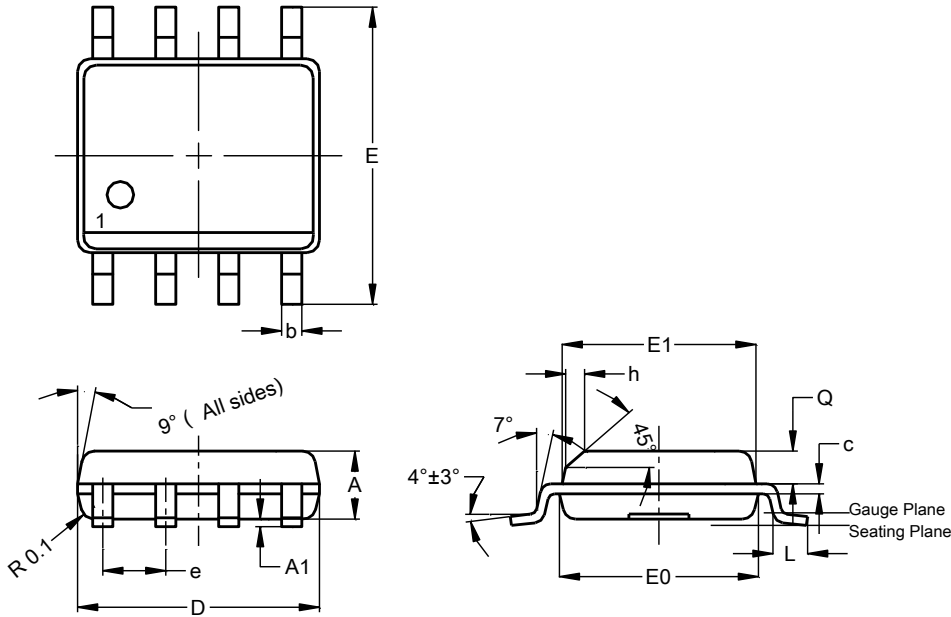


| Device    | Package Type | Identification Code |
|-----------|--------------|---------------------|
| AP2151AFM | U-DFN2018-6  | ZU                  |

**Package Outline Dimensions**

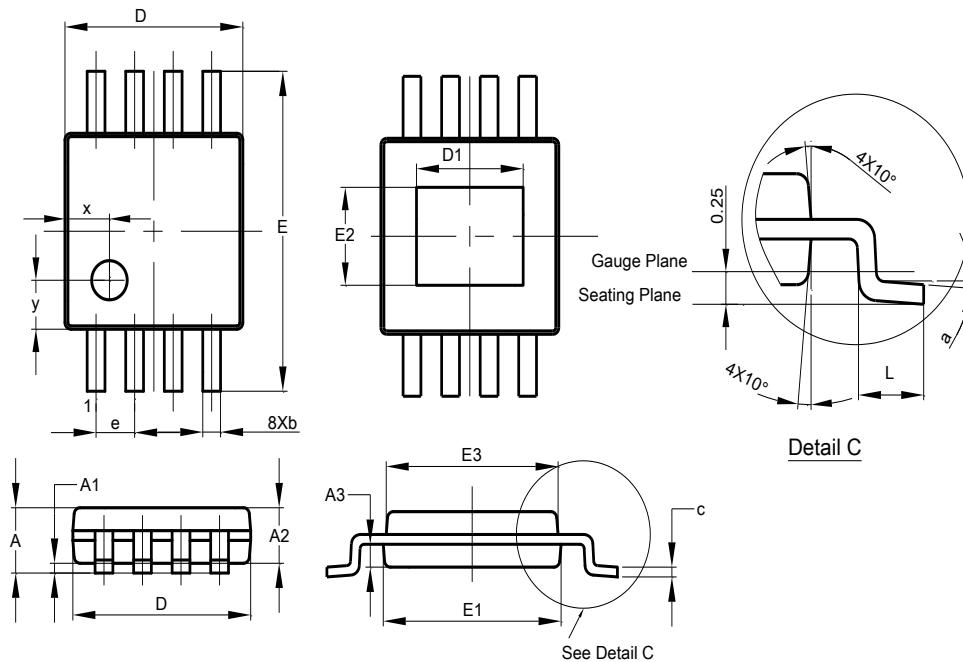
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**(1) Package Type: SO-8**



| SO-8                 |      |      |      |
|----------------------|------|------|------|
| Dim                  | Min  | Max  | Typ  |
| A                    | 1.40 | 1.50 | 1.45 |
| A1                   | 0.10 | 0.20 | 0.15 |
| b                    | 0.30 | 0.50 | 0.40 |
| c                    | 0.15 | 0.25 | 0.20 |
| D                    | 4.85 | 4.95 | 4.90 |
| E                    | 5.90 | 6.10 | 6.00 |
| E1                   | 3.80 | 3.90 | 3.85 |
| E0                   | 3.85 | 3.95 | 3.90 |
| e                    | --   | --   | 1.27 |
| h                    | -    | --   | 0.35 |
| L                    | 0.62 | 0.82 | 0.72 |
| Q                    | 0.60 | 0.70 | 0.65 |
| All Dimensions in mm |      |      |      |

**(2) Package Type: MSOP-8EP**

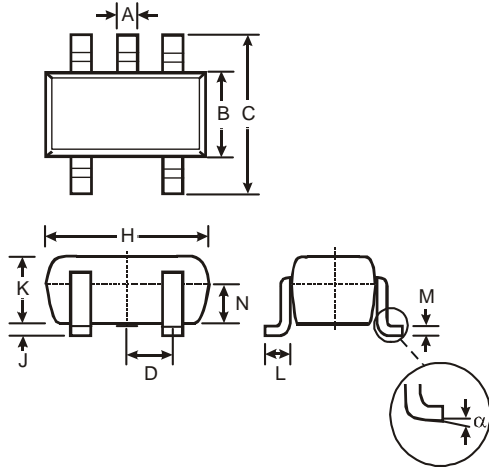


| MSOP-8EP             |      |      |       |
|----------------------|------|------|-------|
| Dim                  | Min  | Max  | Typ   |
| A                    | -    | 1.10 | -     |
| A1                   | 0.05 | 0.15 | 0.10  |
| A2                   | 0.75 | 0.95 | 0.86  |
| A3                   | 0.29 | 0.49 | 0.39  |
| b                    | 0.22 | 0.38 | 0.30  |
| c                    | 0.08 | 0.23 | 0.15  |
| D                    | 2.90 | 3.10 | 3.00  |
| D1                   | 1.60 | 2.00 | 1.80  |
| E                    | 4.70 | 5.10 | 4.90  |
| E1                   | 2.90 | 3.10 | 3.00  |
| E2                   | 1.30 | 1.70 | 1.50  |
| E3                   | 2.85 | 3.05 | 2.95  |
| e                    | -    | -    | 0.65  |
| L                    | 0.40 | 0.80 | 0.60  |
| a                    | 0°   | 8°   | 4°    |
| x                    | -    | -    | 0.750 |
| y                    | -    | -    | 0.750 |
| All Dimensions in mm |      |      |       |

**Package Outline Dimensions (Cont.)**

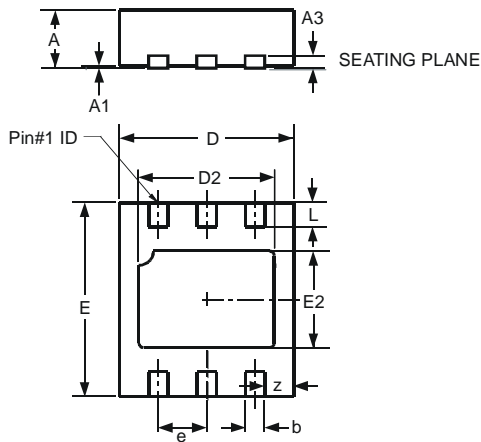
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**(3) Package Type: SOT25**



| SOT25                |       |      |      |
|----------------------|-------|------|------|
| Dim                  | Min   | Max  | Typ  |
| A                    | 0.35  | 0.50 | 0.38 |
| B                    | 1.50  | 1.70 | 1.60 |
| C                    | 2.70  | 3.00 | 2.80 |
| D                    | —     | —    | 0.95 |
| H                    | 2.90  | 3.10 | 3.00 |
| J                    | 0.013 | 0.10 | 0.05 |
| K                    | 1.00  | 1.30 | 1.10 |
| L                    | 0.35  | 0.55 | 0.40 |
| M                    | 0.10  | 0.20 | 0.15 |
| N                    | 0.70  | 0.80 | 0.75 |
| α                    | 0°    | 8°   | —    |
| All Dimensions in mm |       |      |      |

**(4) U-DFN2018-6**

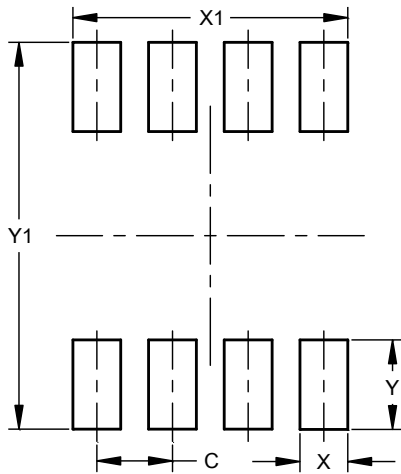


| U-DFN2018-6          |       |       |       |
|----------------------|-------|-------|-------|
| Dim                  | Min   | Max   | Typ   |
| A                    | 0.545 | 0.605 | 0.575 |
| A1                   | 0     | 0.05  | 0.02  |
| A3                   | —     | —     | 0.13  |
| b                    | 0.15  | 0.25  | 0.20  |
| D                    | 1.750 | 1.875 | 1.80  |
| D2                   | 1.30  | 1.50  | 1.40  |
| e                    | —     | —     | 0.50  |
| E                    | 1.95  | 2.075 | 2.00  |
| E2                   | 0.90  | 1.10  | 1.00  |
| L                    | 0.20  | 0.30  | 0.25  |
| z                    | —     | —     | 0.30  |
| All Dimensions in mm |       |       |       |

**Suggested Pad Layout**

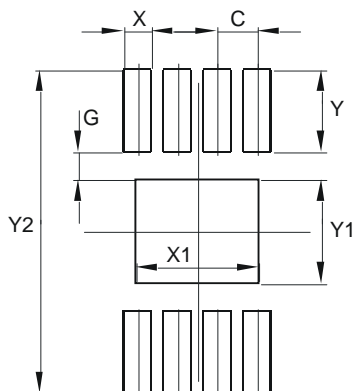
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**(1) Package Type: SO-8**



| Dimensions | Value (in mm) |
|------------|---------------|
| C          | 1.27          |
| X          | 0.802         |
| X1         | 4.612         |
| Y          | 1.505         |
| Y1         | 6.50          |

**(2) Package Type: MSOP-8EP**



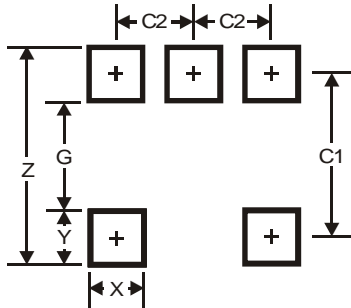
| Dimensions | Value (in mm) |
|------------|---------------|
| C          | 0.650         |
| G          | 0.450         |
| X          | 0.450         |
| X1         | 2.000         |
| Y          | 1.350         |
| Y1         | 1.700         |
| Y2         | 5.300         |



**Suggested Pad Layout (Cont.)**

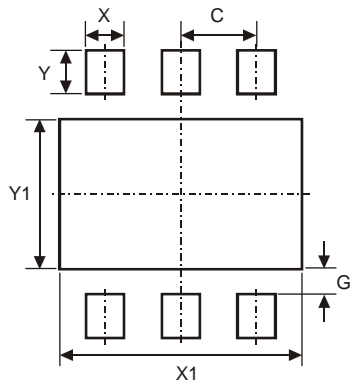
Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**(3) Package Type: SOT25**



| Dimensions | Value (in mm) |
|------------|---------------|
| Z          | 3.20          |
| G          | 1.60          |
| X          | 0.55          |
| Y          | 0.80          |
| C1         | 2.40          |
| C2         | 0.95          |

**(4) Package Type: U-DFN2018-6**



| Dimensions | Value (in mm) |
|------------|---------------|
| C          | 0.50          |
| G          | 0.20          |
| X          | 0.25          |
| X1         | 1.60          |
| Y          | 0.35          |
| Y1         | 1.20          |

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