HARRIS SEMICONDUCTOR

HI-506A, HI-507A HI-508A, HI-509A

16 Channel, 8 Channel, Differential 8 and Differential 4 Channel, CMOS Analog MUXs with Active Overvoltage Protection

December 1993

Features

- Analog Overvoltage $70V_{P-P}$
- No Channel Interaction During Overvoltage
- 44V Maximum Power Supply
- Fail Safe with Power Loss (No Latch-Up)
- Break-Before-Make Switching
- Analog Signal Range ±15V
- Access Time 500ns
- Power Dissipation 7.5mW

Applications

- Data Acquisition Systems
- Industrial Controls
- Telemetry

Description

The HI-506A, HI-507A, HI-508A and HI-509A are analog multiplexers with active overvoltage protection. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70V peak-to-peak levels with ±15V supplies. Digital inputs will also sustain continuous faults up to 4V greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur. Each input presents 1kΩ of resistance under this condition. These features make the HI-506A, HI-507A, HI-508A and HI-509A ideal for use in systems where the analog inputs originate from external equipment, or separately powered circuitry. All devices are fabricated with 44V dielectrically isolated CMOS technology. The HI-506A is a single 16 channel multiplexer, the HI-507A is an 8 channel differential multiplexer, the HI-508A is a single 8 channel multiplexer and the HI-509A is a differential 4 channel multiplexer. If input overvoltage protection is not needed the HI-506/507/508/509 multiplexers are recommended. For further information see Application Notes AN520 and AN521.

The HI-506A/507A devices are available in a 28 lead Plastic or Ceramic DIP and the HI-508A/509A devices are available in a 16 lead Plastic or Ceramic DIP package.

The HI-50XA are offered in industrial/commercial and military grades, additional Hi-Rel screening including 160 hour burn-in is specified by the "8" suffix. For Mil-Std-883 compliant parts, request the HI-546/883, HI-547/883, HI-548/883 or HI-549/883 data sheets.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0506A-2	-55°C to +125°C	28 Lead Ceramic DIP
HI1-0506A-5	0°C to +75°C	28 Lead Ceramic DIP
HI1-0506A-7	0°C to +75°C + 96 Hour Burn-In	28 Lead Ceramic DIP
HI1-0506A-8	-55°C to +125°C + 160 Hour Burn-In	28 Lead Ceramic DIP
HI3-0506A-5	+0°C to +75°C	28 Lead Plastic DIP
HI1-0507A-2	-55°C to +125°C	28 Lead Ceramic DIP
HI1-0507A-5	0°C to +75°C	28 Lead Ceramic DIP
HI1-0507A-7	0°C to +75°C + 96 Hour Burn-In	28 Lead Ceramic DIP
HI1-0507A-8	-55°C to +125°C + 160 Hour Burn-In	28 Lead Ceramic DIP
HI3-0507A-5	0°C to +75°C	28 Lead Plastic DIP

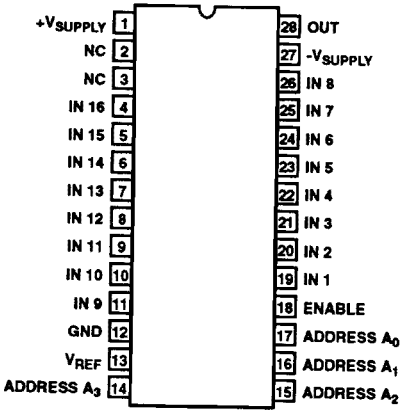
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0508A-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0508A-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-0508A-7	0°C to +75°C + 96 Hour Burn-In	16 Lead Ceramic DIP
HI1-0508A-8	-55°C to +125°C + 160 Hour Burn-In	16 Lead Ceramic DIP
HI3-0508A-5	+0°C to +75°C	16 Lead Plastic DIP
HI1-0509A-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0509A-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-0509A-7	0°C to +75°C + 96 Hour Burn-In	16 Lead Ceramic DIP
HI1-0509A-8	-55°C to +125°C + 160 Hour Burn-In	16 Lead Ceramic DIP
HI3-0509A-5	0°C to +75°C	16 Lead Plastic DIP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

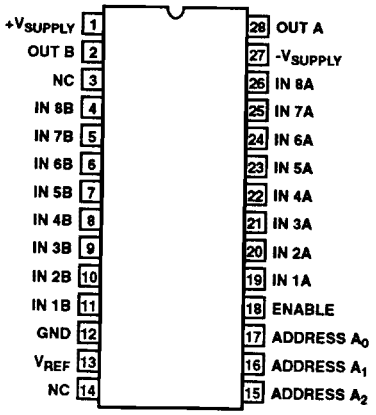
File Number **3143**

Pinouts

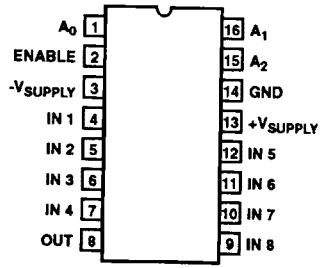
HI1-506A (CDIP)
HI3-506A (PDIP)
TOP VIEW



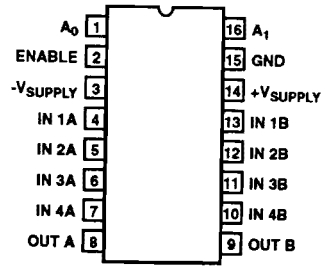
HI1-507A (CDIP)
HI3-507A (PDIP)
TOP VIEW



HI1-508A (CDIP)
HI3-508A (PDIP)
TOP VIEW

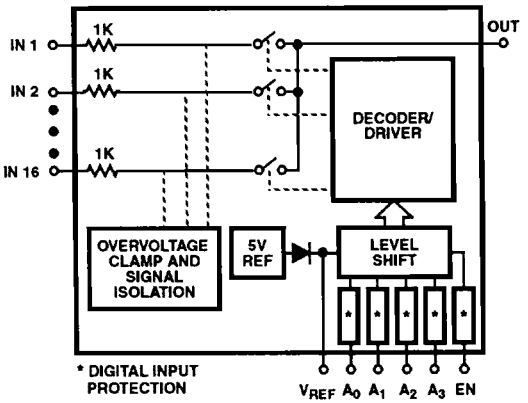


HI1-509A (CDIP)
HI3-509A (PDIP)
TOP VIEW

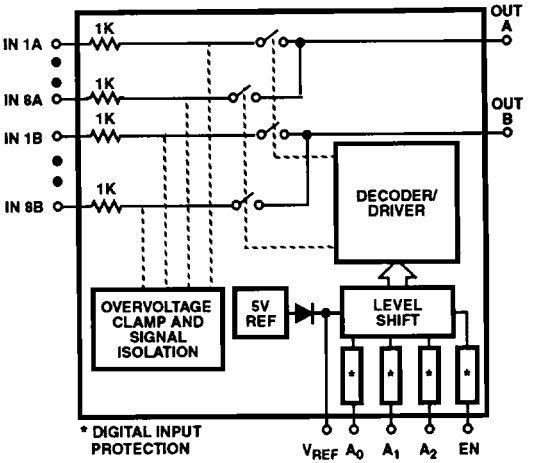


Functional Diagrams

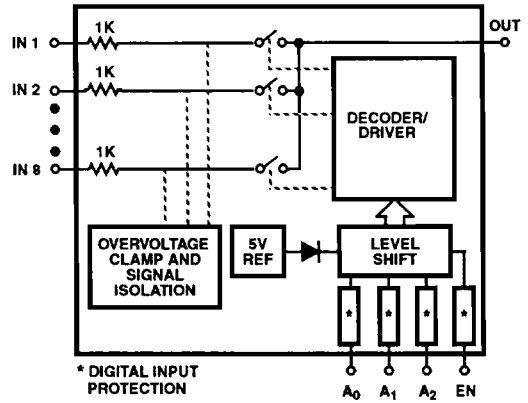
HI-506A



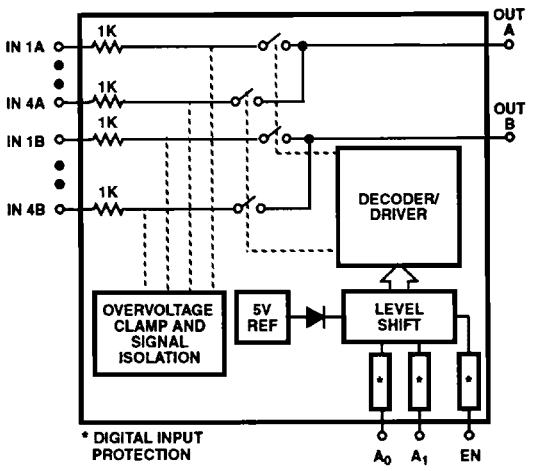
HI-507A



HI-508A

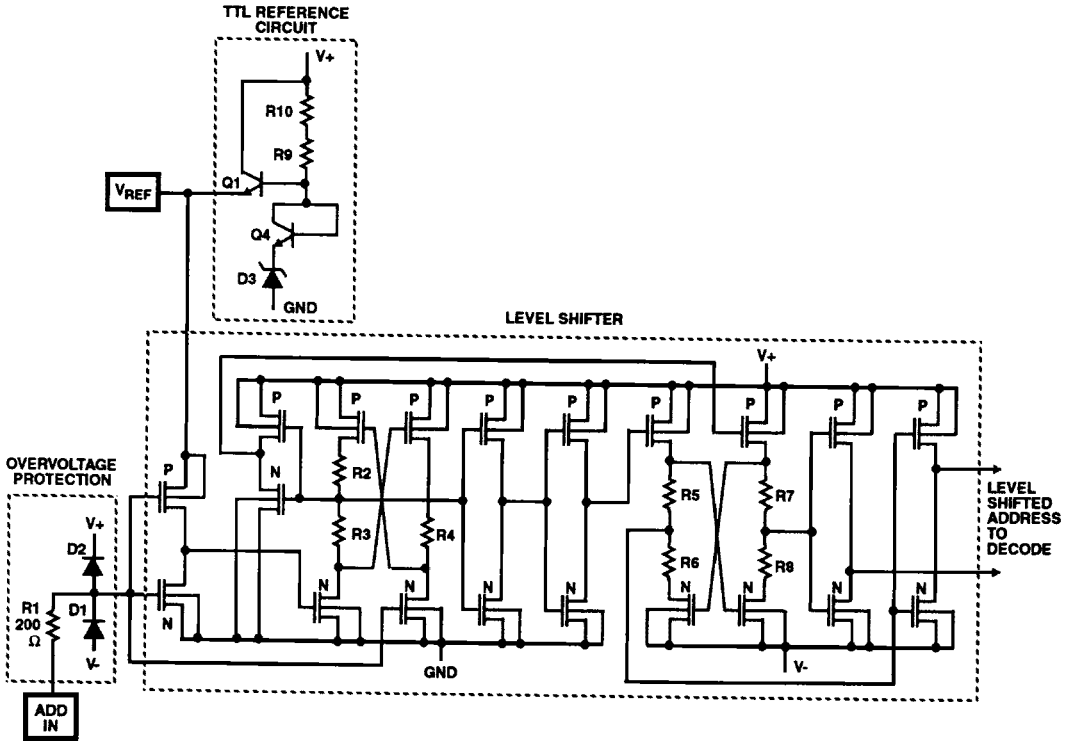


HI-509A

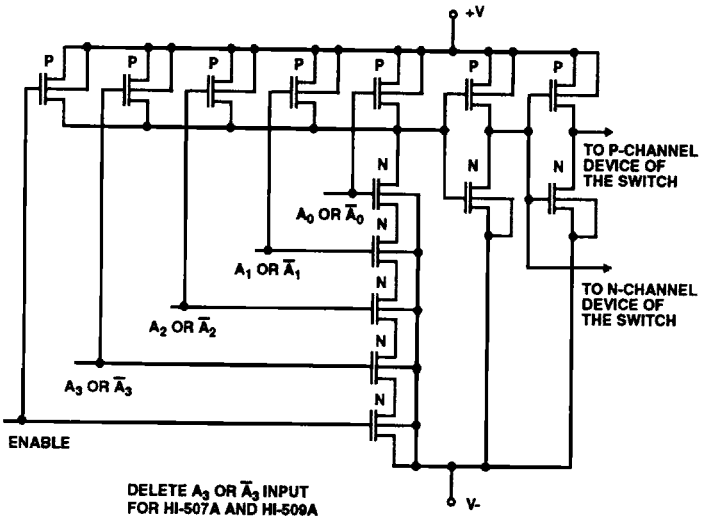


Schematic Diagrams

ADDRESS INPUT BUFFER AND LEVEL SHIFTER

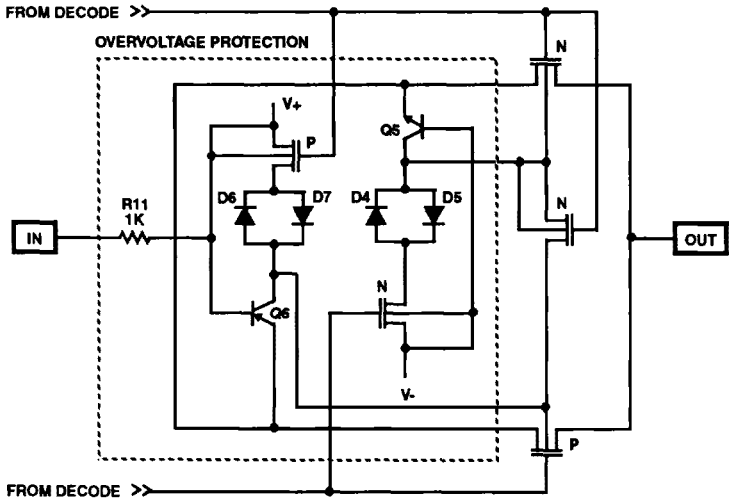


ADDRESS DECODER



Schematic Diagrams (Continued)

MULTIPLEX SWITCH



Absolute Maximum Ratings

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ ..... +44V
$V_{SUPPLY(+)}$ to GND ..... +22V
$V_{SUPPLY(-)}$ to GND ..... +25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first
Analog Signal Overvoltage
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V
Continuous Current, S or D 20mA
Peak Current, S or D 40mA
(Pulsed at 1ms, 10% duty cycle max)
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
28 Lead Ceramic DIP Packages (HI-506A, HI-507A)	20°C/W	55°C/W
16 Lead Ceramic DIP Packages (HI-508A, HI-509A)	24°C/W	80°C/W
28 Lead Plastic DIP Packages (HI-506A, HI-507A)		60°C/W
16 Lead Plastic DIP Packages (HI-508A, HI-509A)		100°C/W

Operating Temperature Ranges
HI-506A/507A/508A/509A-2, -8 ..... -55°C to +125°C
HI-506A/507A/508A/509A-5, -7 ..... 0°C to +75 °C
Junction Temperature
Ceramic DIP ..... +175°C
Plastic DIP ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. For Test Conditions, Consult Performance Curves.

PARAMETER	TEMP	HI-50XA-2, -8			HI-50XA-5, -7			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS								
Access Time, t_A (Note 1)	+25°C	-	0.5	-	-	0.5	-	µs
	Full	-	-	1.0	-	-	1.0	µs
Break-Before-Make Delay, t_{OPEN} (Note 1)	+25°C	25	80	-	25	80	-	ns
Enable Delay (ON), $t_{ON(EN)}$ (Note 1)	+25°C	-	300	500	-	300	-	ns
	Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$ (Note 1)	+25°C	-	300	500	-	300	-	ns
	Full	-	-	1000	-	-	1000	ns
Settling Time to 0.1%, t_S (HI-506A and HI-507A)	+25°C	-	1.2	-	-	1.2	-	µs
Settling Time to 0.01%, t_S (HI-506A and HI-507A)	+25°C	-	3.5	-	-	3.5	-	µs
Settling Time to 0.1%, t_S (HI-508A and HI-509A)	+25°C	-	1.2	-	-	1.2	-	µs
Settling Time to 0.01%, t_S (HI-508A and HI-509A)	+25°C	-	3.5	-	-	3.5	-	µs
"Off Isolation" (Note 6)	+25°C	50	68	-	50	68	-	dB
Channel Input Capacitance, $C_{S(OFF)}$	+25°C	-	12	-	-	12	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-506A)	+25°C	-	52	-	-	52	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-507A)	+25°C	-	30	-	-	30	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-508A)	+25°C	-	25	-	-	25	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-509A)	+25°C	-	12	-	-	12	-	pF
Digital Input Capacitance, C_A	+25°C	-	10	-	-	10	-	pF
Input to Output Capacitance, $C_{DS(OFF)}$	+25°C	-	0.1	-	-	0.1	-	pF
DIGITAL INPUT CHARACTERISTICS								
Input Low Threshold, TTL Drive, V_{AL} (Note 1)	Full	-	-	+0.8	-	-	+0.8	V
Input High Threshold, V_{AH} (Notes 1, 8)	Full	+4.0	-	-	+4.0	-	-	V
Input Leakage Current (High or Low), I_A (Notes 1, 5)	Full	-	-	1.0	-	-	1.0	µA
MOS Drive, V_{AL}, HI-506A/HI-507A (Note 9)	+25°C	-	-	0.8	-	-	0.8	V
MOS Drive, V_{AH}, HI-506A/HI-507A (Note 9)	+25°C	6.0	-	-	6.0	-	-	V

Electrical Specifications Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. For Test Conditions, Consult Performance Curves. **(Continued)**

PARAMETER	TEMP	HI-50XA-2, -8			HI-50XA-5, -7			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG CHANNEL CHARACTERISTICS								
Analog Signal Range, V_S (Note 1)	Full	-15	-	+15	-15	-	+15	V
On Resistance, R_{ON}, (Notes 1, 2)	+25°C	-	1.2	1.5	-	1.5	1.8	kΩ
	Full	-	1.5	1.8	-	1.8	2.0	kΩ
Off Input Leakage Current, $I_{S(OFF)}$ (Notes 1, 3)	+25°C	-	0.03	-	-	0.03	-	nA
	Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$ (Notes 1, 3)	+25°C	-	0.1	-	-	0.1	-	nA
HI-506A	Full	-	-	300	-	-	300	nA
HI-507A	Full	-	-	200	-	-	200	nA
HI-508A	Full	-	-	200	-	-	200	nA
HI-509A	Full	-	-	100	-	-	100	nA
With Input Overvoltage Applied, (I_{DOFF}) (Note 4)	+25°C	-	4.0	-	-	4.0	-	nA
	Full	-	-	2.0	-	-	-	µA
On Channel Leakage Current, $I_{D(ON)}$ (Notes 1, 3)	+25°C	-	0.1	-	-	0.1	-	nA
HI-506A	Full	-	-	300	-	-	300	nA
HI-507A	Full	-	-	200	-	-	200	nA
HI-508A	Full	-	-	200	-	-	200	nA
HI-509A	Full	-	-	100	-	-	100	nA
Differential Off Output Leakage Current, I_{DIFF} (HI-507A, HI-509A Only)	Full	-	-	50	-	-	50	nA
POWER REQUIREMENTS								
Current, I+, Pin 1 (Notes 1, 7)	Full	-	1.5	2.0	-	1.5	2.0	mA
Current, I+, HI-508A/HI-509A (Notes 1, 7)	Full	-	1.5	2.4	-	1.5	2.0	mA
Current, I-, Pin 27 (Notes 1, 7)	Full	-	0.02	1.0	-	0.02	1.0	mA
Power Dissipation, P_D	Full	-	7.5	-	-	7.5	-	mW

NOTES:

1. 100% tested for Dash 8. Leakage currents not tested at -55°C.
2. V_{OUT} = ±10V, I_{OUT} = ∓100µA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at +25°C.
6. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz.
7. V_{EN}, V_A = 0V or 4.0V.
8. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.
9. V_{REF} = +10V.

Performance Curves and Test Circuits

T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = +4V, V_{AL} = 0.8V, V_{REF} = Open, Unless Otherwise Specified

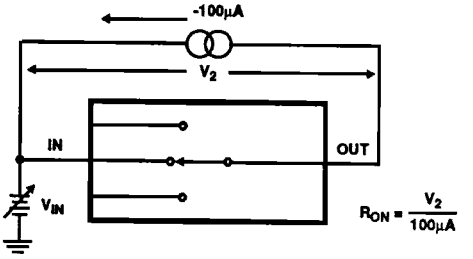


FIGURE 1A. TEST CIRCUIT

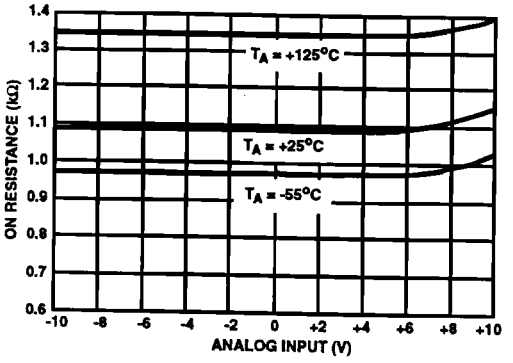


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE

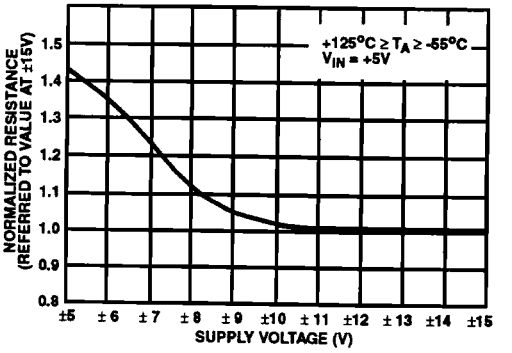


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

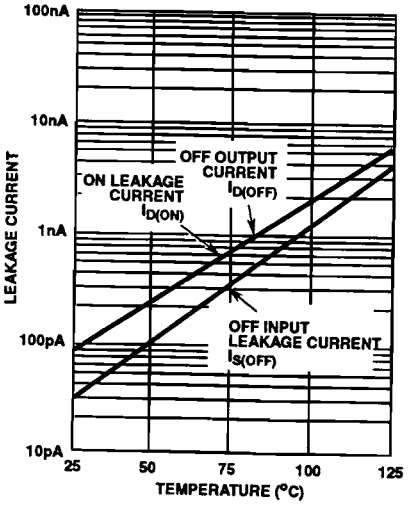


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

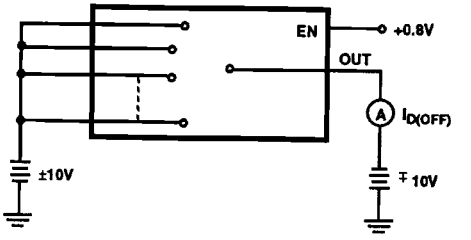


FIGURE 2B. $I_{D(OFF)}$ (NOTE 1)

NOTE:

1. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V)

FIGURE 2. LEAKAGE CURRENTS

Performance Curves and Test Circuits $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified (Continued)

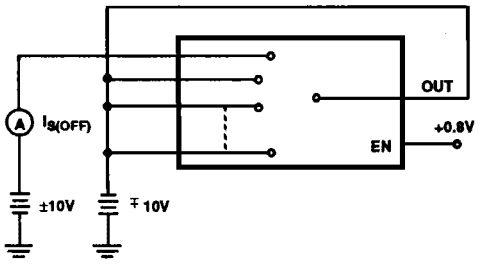


FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT (NOTE 1)

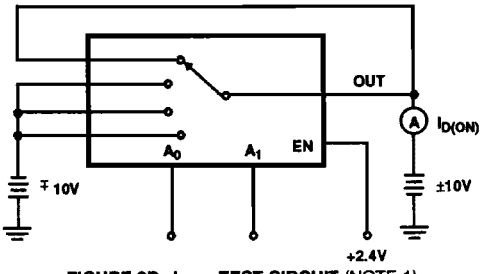


FIGURE 2D. $I_{D(On)}$ TEST CIRCUIT (NOTE 1)

NOTE:

1. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V)

FIGURE 2. LEAKAGE CURRENTS (Continued)

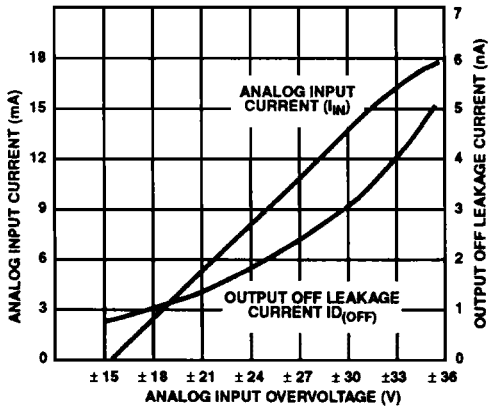


FIGURE 3A. ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

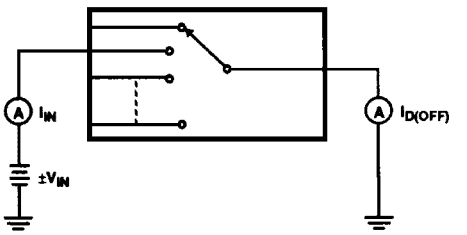


FIGURE 3B. TEST CIRCUIT

FIGURE 3. OVERVOLTAGE CHARACTERISTICS

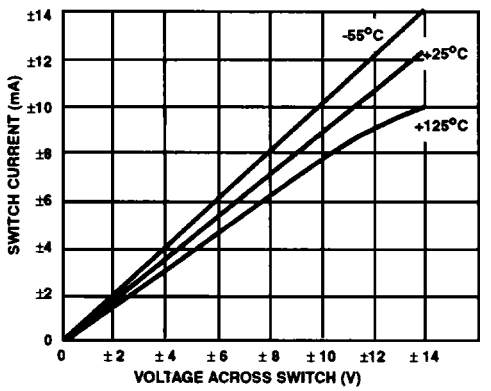


FIGURE 4A. ON CHANNEL CURRENT vs VOLTAGE

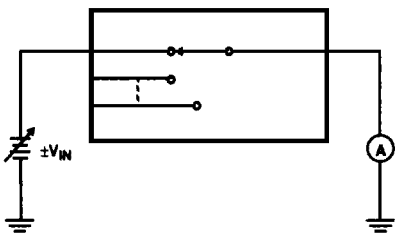


FIGURE 4B. TEST CIRCUIT

FIGURE 4. ON CHANNEL CURRENT

Performance Curves and Test Circuits T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = +4V, V_{AL} = 0.8V, V_{REF} = Open, Unless Otherwise Specified (Continued)

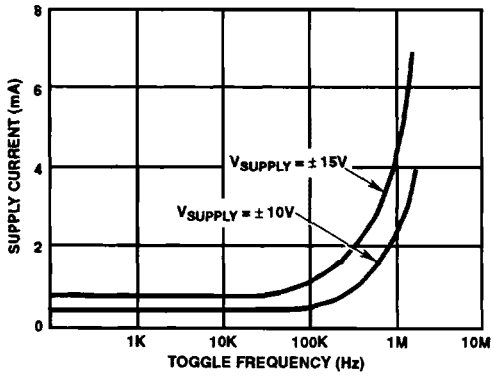
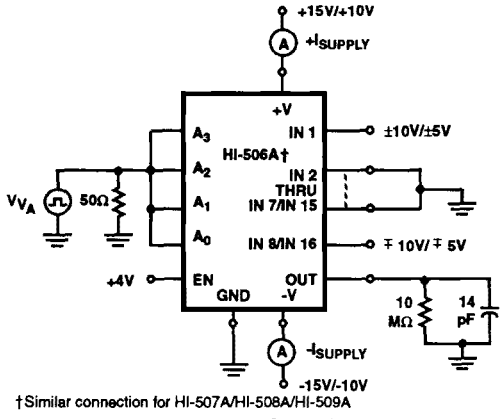


FIGURE 5A. SUPPLY CURRENT vs TOGGLE FREQUENCY



†Similar connection for HI-507A/HI-508A/HI-509A

FIGURE 5B. TEST CIRCUIT

FIGURE 5. SUPPLY CURRENTS

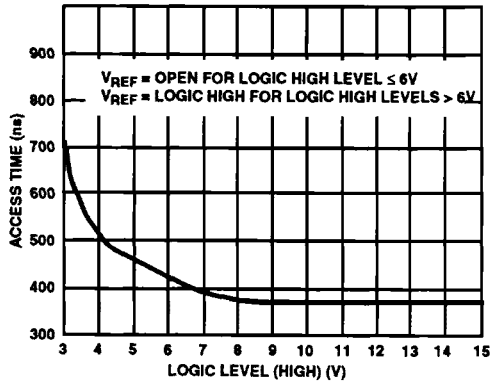
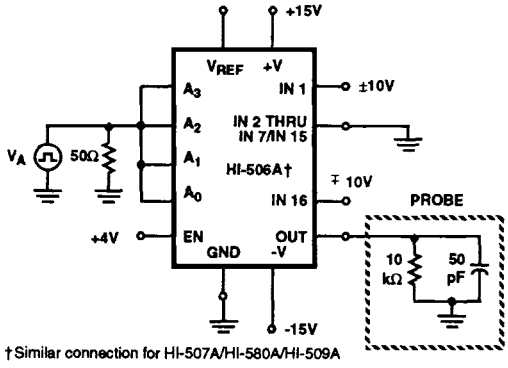


FIGURE 6A. ACCESS TIME vs LOGIC LEVEL (HIGH)



†Similar connection for HI-507A/HI-580A/HI-509A

FIGURE 6B. TEST CIRCUIT

FIGURE 6. ACCESS TIME

Switching Waveforms

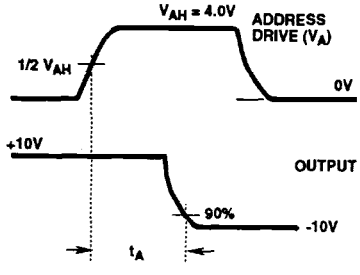


FIGURE 7A.

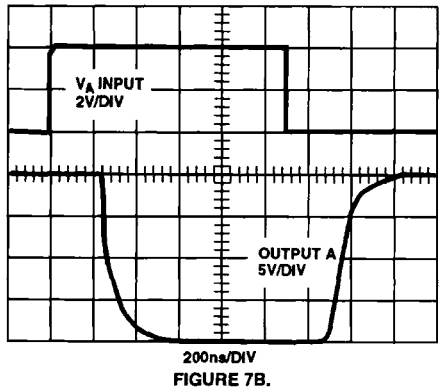
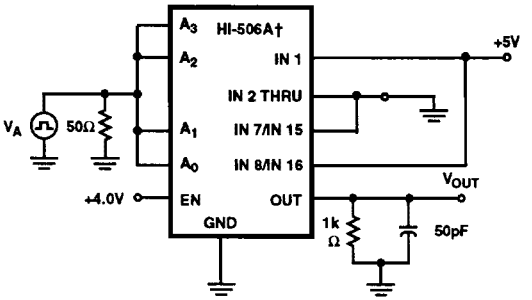


FIGURE 7B.

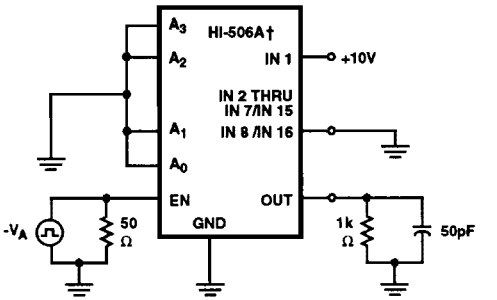
FIGURE 7. ACCESS TIME

Switching Waveforms (Continued)



†Similar connection for HI-507A/HI-508A/HI-509A

FIGURE 8A.



†Similar connection for HI-507A//HI-508A/HI-509A

FIGURE 9A.

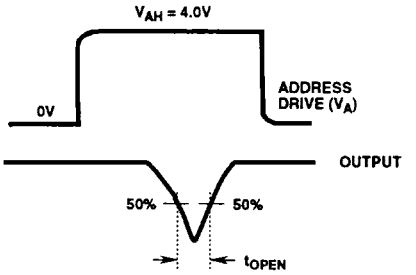


FIGURE 8B.

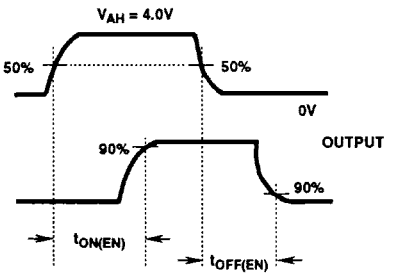


FIGURE 9B.

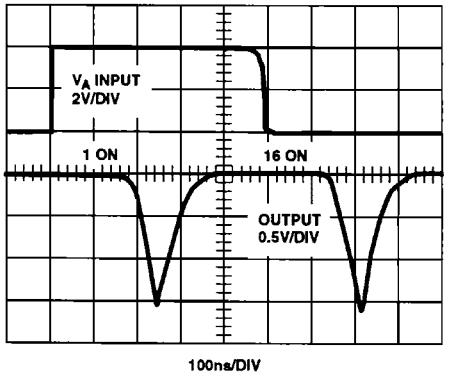


FIGURE 8C.

FIGURE 8. BREAK-BEFORE-MAKE DELAY

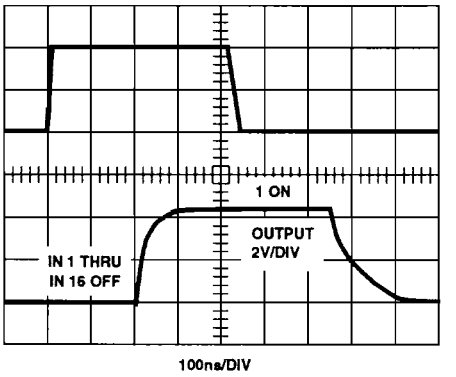


FIGURE 9C.

FIGURE 9. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

Truth Tables

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-508A

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Die Characteristics

DIE DIMENSIONS: 159 mils x 83.9 mils x 19 mils

METALLIZATION:
Type: CuAl
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Silox: 12kÅ ± 2kÅ
Nitride: 3.5kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
$1.4 \times 10^5 A/cm^2$

TRANSISTOR COUNT: 485

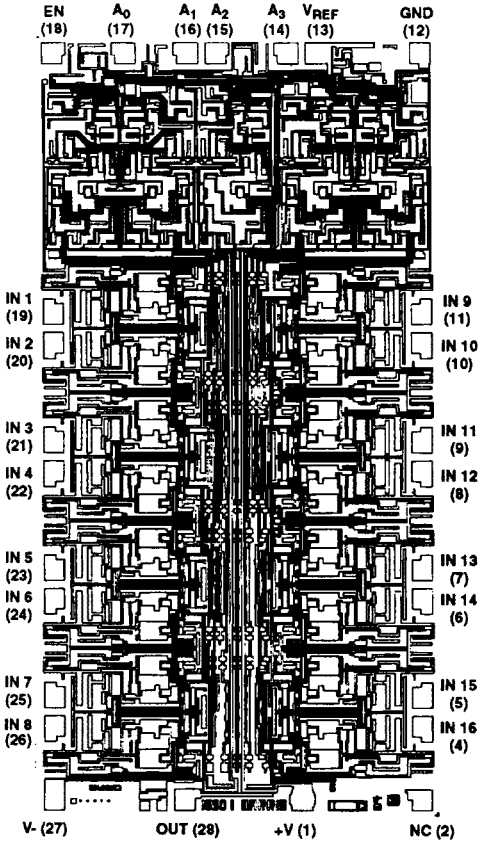
PROCESS: CMOS-DI

SUBSTRATE POTENTIAL*: $-V_{SUPPLY}$

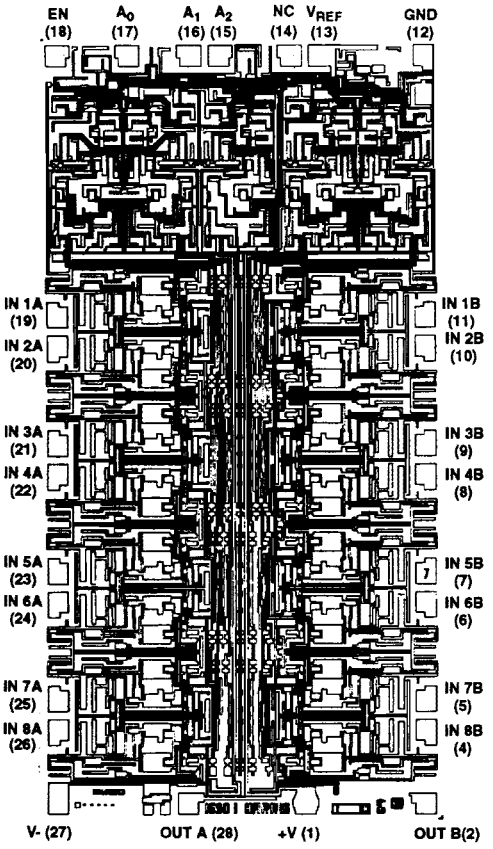
* The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential

Metallization Mask Layout

HI-506A



HI-507A



Die Characteristics

DIE DIMENSIONS: 108 mils x 83 mils

METALLIZATION:
Type: CuAl
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Silox: 12kÅ ± 2kÅ
Nitride: 3.5kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
$1.4 \times 10^5 A/cm^2$

TRANSISTOR COUNT: 253

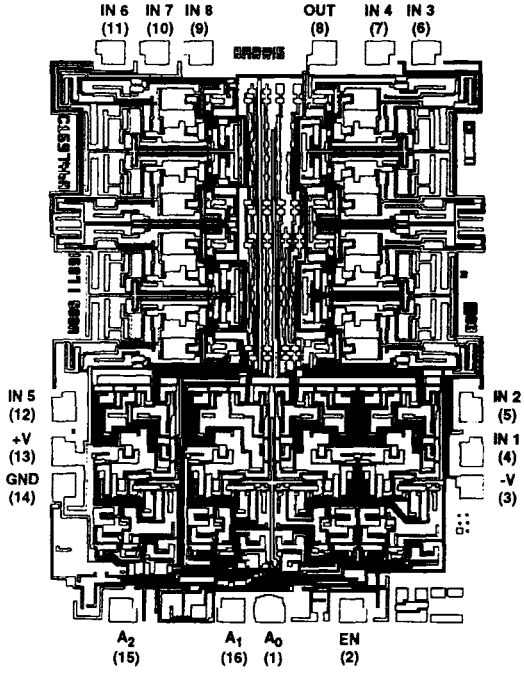
PROCESS: CMOS-DI

SUBSTRATE POTENTIAL*: $-V_{SUPPLY}$

* The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential

Metallization Mask Layout

HI-508A



HI-509A