KAI-0373

768 (H) x 484 (V) Interline CCD Image Sensor

ON Semiconductor®

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Description

The KAI−0373 is a high-performance silicon charge-coupled device (CCD) designed for video image sensing and electronic still photography. The device is built using an advanced true two-phase, double-polysilicon, NMOS CCD technology. The p+npn− photodetector elements eliminate image lag and reduce image smear while providing anti-blooming protection and electronic-exposure control. The total chip size is 9.9 (H) mm × 7.7 (V) mm. The KAI−0373 comes in monochrome versions, with an option with microlens for sensitivity improvement.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Interline Transfer CDD; Progressive Scan
Number of Active Pixels	768 (H) × 484 (V)
Number of Outputs	1
Pixel Size	11.6 μm(H) × 13.6 μm (V)
Active Image Size	8.91 mm (H) × 6.58 mm (V), 11.1 mm (Diagonal), 2/3″ Optical Format
Aspect Ratio	3:2
Output Sensitivity	9 μV/e⁻
Photometric Sensitivity KAI−0373−ABA	2.2 V/lux−sec
Charge Capacity	55 ke⁻
Maximum Pixel Clock Speed	14.32 MHz
Maximum Frame Rate	30 fps
Package Type	CerDIP
Package Size	0.800″ [20.32 mm] Width 1.200″ [30.48 mm] Length
Package Pins	24
Package Pin Spacing	0.100″ (2.54 mm)

NOTE: All Parameters are specified at T = 40°C unless otherwise noted.

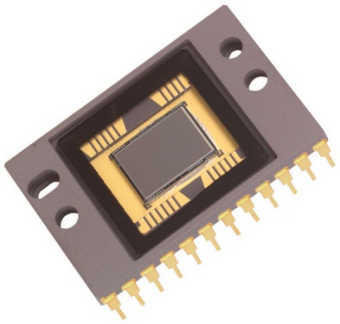


Figure 1. KAI−0373 Interline CCD Image Sensor

Features

- High Resolution
- High Sensitivity
- High Dynamic Range
- Low Noise Architecture
- High Frame Rate
- Binning Capability for Higher Frame Rate
- Electronic Shutter

Application

- Intelligent Traffic Systems
- Surveillance

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION

Part Number	Description	Marking Code
KAI−0373−AAA−CP−BA	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Standard Grade	KAI−0373−AAA Serial Number
KAI−0373−ABA−CB−AE	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Sealed Clear Cover Glass (No Coatings), Engineering Grade	KAI−0373−ABA Serial Number
KAI−0373−ABA−CB−BA	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Sealed Clear Cover Glass (No Coatings), Standard Grade	
KAI−0373−ABA−CP−BA	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass (No Coatings), Standard Grade	

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

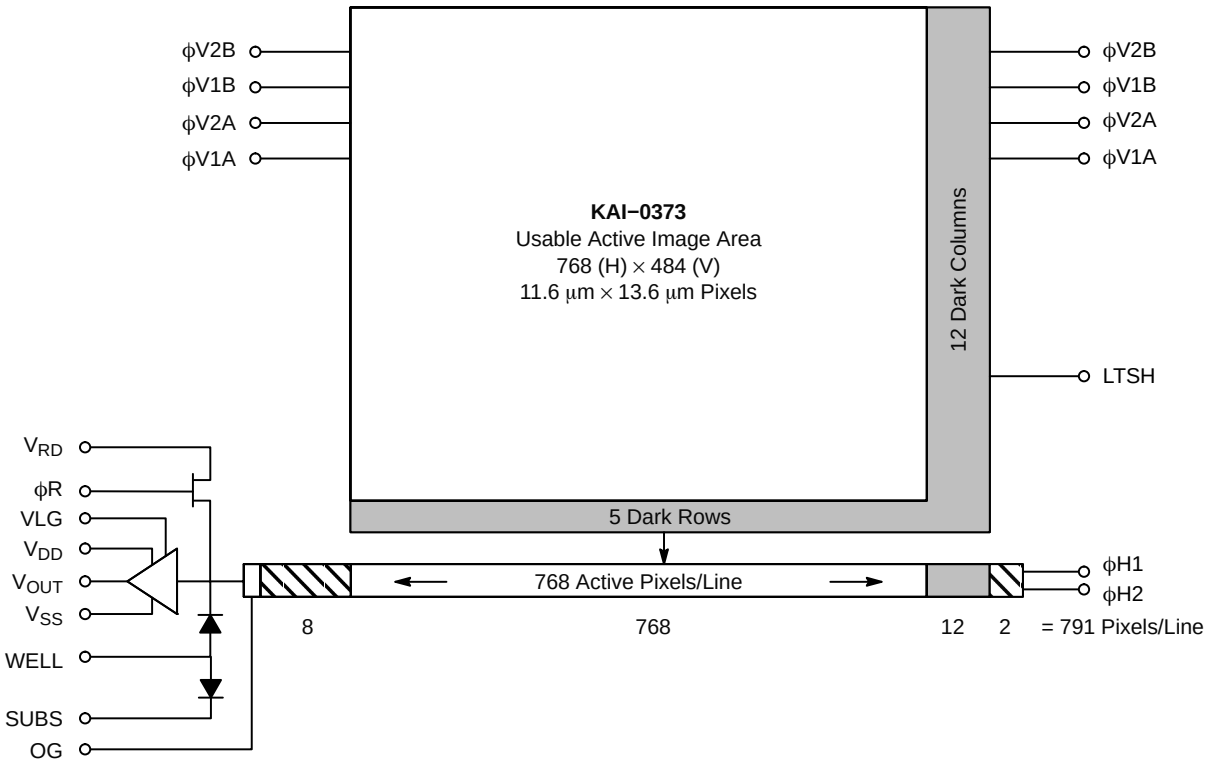


Figure 2. Block Diagram

The KAI−0373 consists of 371, 712 photodiodes, 768 vertical (parallel) CCD shift registers (VCCDs), one horizontal (serial) CCD shift register and one output amplifier. The advanced, progressive-scan architecture of the device allows the entire image area to be read out in a single scan. The pixels are arranged in a 768 (H) × 484 (V) array in which an additional 12 columns and 5 rows of light shielded pixels are added as dark reference.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the photodiode's charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

Charge Transport

The accumulated or integrated charge from each photodiode is transported to the output by a three step process. The charge is first transported from the photodiodes to the VCCDs by applying a large positive voltage to the phase-one vertical clock (ϕV2). This reads out every row, or line, of photodiodes into the VCCDs.

The charge is then transported from the VCCDs to the HCCDs line by line. Finally, the HCCDs transport these rows of charge packets to the output structures pixel by pixel. On each falling edge of the horizontal clock, ϕH2, these charge packets are dumped over the output gate (OG, Figure 3) onto the floating diffusion (FD Figure 3).

Both the horizontal and vertical shift registers use traditional two-phase complementary clocking for charge transport. Transfer to the horizontal CDD begins when ϕV2 is brought low (and ϕV1 high) causing a line of charge to transfer from ϕV2 to ϕV1 and subsequently into the horizontal register. The sequence completes when ϕV1 is brought low before the horizontal CCD reads the first line of charge.

Output Structure

Charge packets contained in the horizontal register are dumped pixel by pixel, onto the floating diffusion output node whose potential varies linearly with the quantity of charge in each packet. The amount of potential change is determined by the expression $\Delta V_{FD} = \Delta Q / C_{FD}$. A three stage source-follower amplifier is used to buffer this signal voltage off chip with slightly less than unity gain. The translation from the charge domain to the voltage domain is quantified by the output sensitivity or charge to voltage conversion in terms of $\mu V/e^-$. After the signal has been sampled off-chip, the reset clock (ϕR) removes the charge from the floating diffusion and resets its potential to the reset-drain voltage (VRD).

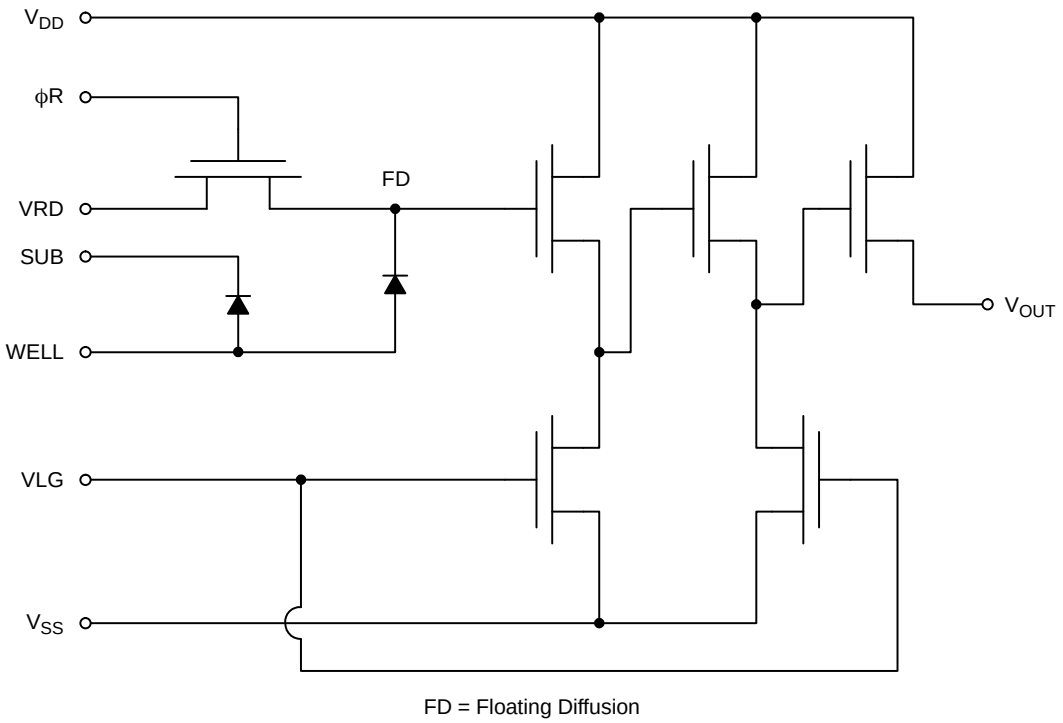


Figure 3. Output Structure

Electronic Shutter

The KAI−0373 provides a structure for the prevention of blooming which may be used to realize a variable exposure time as well as performing the anti-blooming function. The anti-blooming function limits the charge capacity of the photodiode by draining excess electrons vertically into the substrate (hence the name Vertical Overflow Drain or VOD). This function is controlled by applying a large potential to the device substrate (device terminal SUB). If a sufficiently large voltage pulse (VES ≈ 40 V) is applied to the substrate, all photodiodes will be emptied of charge through the substrate, beginning the integration period. After returning the substrate voltage to the nominal value, charge can accumulate in the diodes and the charge packet is subsequently readout onto the VCCD at the next occurrence of the high level on ϕV2. The integration time is then the time between the falling edges of the substrate shutter pulse and ϕV2. This scheme allows electronic variation of the exposure time by a variation in the clock timing while maintaining a standard video frame rate.

Application of the large shutter pulse must be avoided during the horizontal register readout or an image artifact will appear due to feedthrough. The shutter pulse VES must be “hidden” in the horizontal retrace interval. The integration time is changed by skipping the shutter pulse from one horizontal retrace interval to another.

The smear specification is not met under electronic shutter operation. Under constant light intensity and spot size, if the electronic exposure time is decreased, the smear signal will remain the same while the image signal will decrease linearly with exposure. Smear is quoted as a percentage of the image signal and so the percent smear will increase by the same factor that the integration time has decreased. This effect is basic to interline devices.

Extremely bright light can potentially harm solid state imagers such as Charge-Coupled Devices (CCDs). Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

On-Chip Gate Protection

Gates OG, ϕR, VLG, V_{SS}, ϕH1 and ϕH2 are internally connected to transistors as shown in Figure 4 to provide active ESD protection. For the protection to work, pin 11 (Horizontal ESD well) and pin 13 (Vertical ESD well) must be biased to –10 V. The ESD bias must be at least 1 V more negative that ϕH1 and ϕH2 during sensor operation and during camera power turn on.

This sensor, like most other MOS-based image sensors, is extremely sensitive to electrostatic discharge (ESD) damage. The handling and environment of the sensor must be controlled to protect this device from ESD damage.

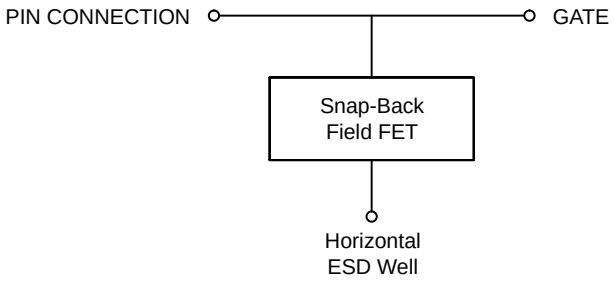


Figure 4. Internal Protection Circuit for ϕH1 and ϕH2

Physical Description

Pin Description and Device Orientation

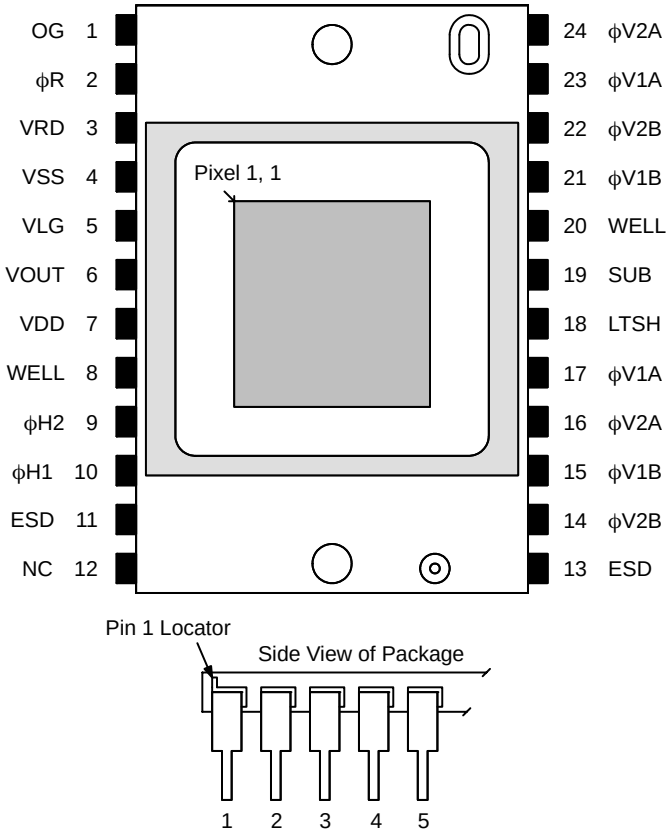


Figure 5. Pin Description

Table 3. PIN DESCRIPTION

Pin	Name	Description
1	OG	Output Gate
2	ϕR	Reset Clock
3	VRD	Reset Drain
4	VSS	Output Amplifier Return
5	VLG	Output Amplifier Load Gate
6	VOUT	Video Output
7	VDD	Output Amplifier Supply
8	WELL	Ground
9	ϕH2	Horizontal CCD Clock − Phase 2
10	ϕH1	Horizontal CCD Clock − Phase 1
11	ESD	Horizontal ESD Well
12	NC	No Connect

Pin	Name	Description
13	ESD	Horizontal ESD Well
14	ϕV2B	Vertical CCD Clock − Phase 2
15	ϕV1B	Vertical CCD Clock − Phase 1
16	ϕV2A	Vertical CCD Clock − Phase 2
17	ϕV1A	Vertical CCD Clock − Phase 1
18	LTSH	Lightshield
19	SUB	Substrate
20	WELL	Ground
21	ϕV1B	Vertical CCD Clock − Phase 1
22	ϕV2B	Vertical CCD Clock − Phase 2
23	ϕV1A	Vertical CCD Clock − Phase 1
24	ϕV2A	Vertical CCD Clock − Phase 2

1. The pins are on a 0.100″ spacing.
2. Pins 14, 16, 22, and 24 must be connected together – only one Phase 2 clock driver is required.
3. Pins 15, 17, 21, and 23 must be connected together – only one Phase 1 clock driver is required.

IMAGING PERFORMANCE

All following values were derived for the KAI−0373−ABA series devices (with microlens array) using nominal operating conditions and the recommended timing. Unless otherwise stated, readout time = 33 ms, integration time = 33 ms, no electronic shutter pulse is applied, and sensor temperature = 40°C. Correlated double sampling of the output is assumed and recommended. Defects are excluded from the following tests and the signal output is referenced to the dark pixels at the end of each line unless otherwise specified.

Specifications

Table 4. CCD

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
Saturation Signal – VCCD	Ne^-_{SAT}	55	−	−	ke^-	
Output Saturation Signal	V_{SAT}	500	−	−	mV	1, 2, 6
Photodiode Dark Current	I_D	−	−	0.5	nA	
Charge Transfer Efficiency	CTE	−	0.99999	−		2, 3
Horizontal CCD Frequency	f_H	−	14.3	−	MHz	
Image Lag	IL	−	Negligible	−		
Blooming Margin	X_{AB}	−	300	−		4, 6
Smear	Smr	−	0.01	0.04	%	5

1. V_{SAT} is the mean value at saturation as measured at the output of the device with X_{AB} = 300. This value is guaranteed only when $V_{SUB} = V_{AB}$ as indicated on the sensor package. V_{SAT} can be varied by adjusting V_{SUB}.
2. Measured at the sensor output.
3. With stray load capacitance of CL = 10pF between the output and AC ground.
4. X_{AB} represents the increase above the saturation-irradiance level (H_{SAT}) that the device can be exposed to before blooming of the vertical shift register will occur. It should be noted that V_{OUT} rises above V_{SAT} for irradiance levels above H_{SAT}.
5. Measured under 10% (~48 lines) image height illumination with white light source and without electronic shutter operation and below V_{SAT}.
6. It should be noted that there is a tradeoff between X_{AB} and V_{SAT}.

Table 5. OUTPUT AMPLIFIER @ V_{DD} = 15 V, V_{SS} = 0.5 V

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
Output DC Offset	V_{ODC}	5	6.3	7.5	V	
Power Dissipation	P_D	−	75	−	mW	
Output Amplifier Bandwidth	f_{-3db}	100	−	−	MHz	1
Sensitivity (Output Referred)	$\Delta V_O/\Delta N$	−	9	−	$\mu V/e^-$	
Off-Chip Load	C_L	−	−	10	pF	

1. With stray output load capacitance of C_L = 10 pF between output and AC ground.

Table 6. GENERAL

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
Total Sensor Noise	Ne^-_{TOTAL}	−	55	−	e^- rms	1
Dynamic Range	DR	−	60	−	dB	2

1. Includes amplifier noise, dark pattern noise and dark current shot noise at data rates of 14 MHz.
2. Uses 20 Log (Ne^-_{SAT} / Ne^-_{TOTAL}) where Ne^-_{SAT} refers to the vertical CCD saturation signal.

Table 7. ELECTRO-OPTICAL FOR KAI−0373−ABA MONOCHROME WITH MICROLENS

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
Saturation Exposure	E_{SAT}	−	0.044	−	$\mu J/cm^2$	1
Peak Quantum Efficiency	QE	−	35	−	%	2
Photoresponse Non-Uniformity	PRNU	−	−	2	% rms	3
Photoresponse Non-Linearity	PRNL	−	−	2	%	
Photoresponse Shading	R_S	−	−	10	%	4

1. For λ = 530 nm wavelength, and N_{SAT} = 55 ke$^-$.
2. Refer to typical values from Figure 8.
3. For a 100 $\times$ 100 pixel region under uniform illumination with output signal equal to 80% of saturation signal. Saturation signal, V_{SAT}, is the output voltage at the knee of the output vs illumination curve as shown in Figure 6.
4. This is the global variation in chip output across the entire chip measured at 80% saturation and is expressed as a percentage of the mean pixel value. Saturation signal, V_{SAT}, is the output voltage at the knee of the output vs illumination curve as shown in Figure 6.

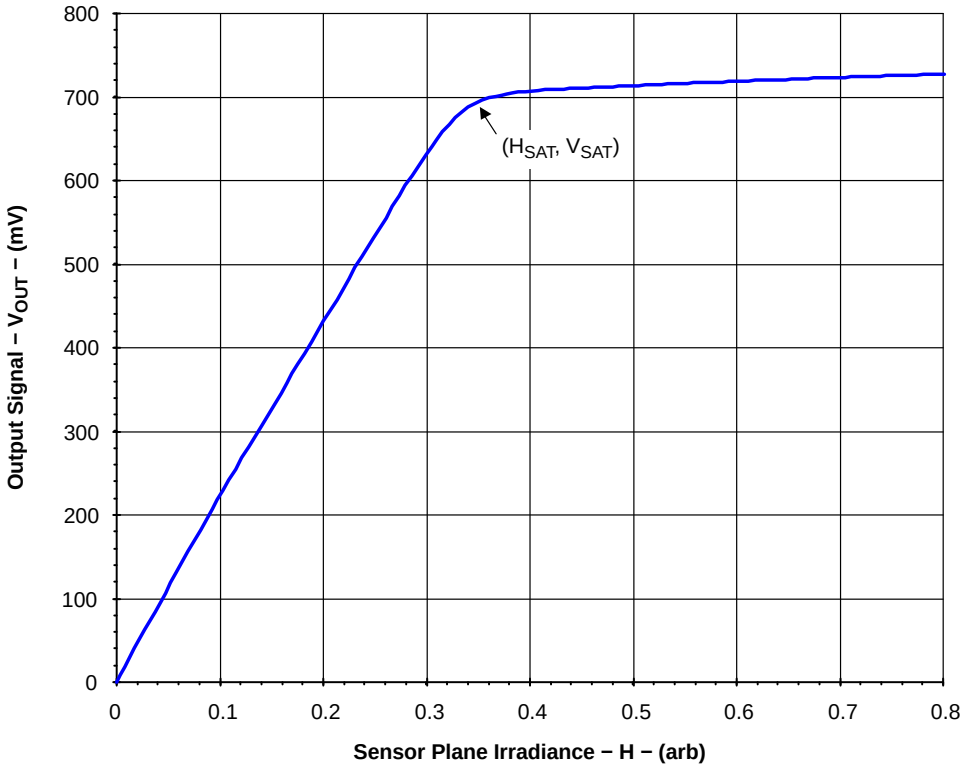


Figure 6. Typical KAI−0373 Photoresponse

Defect Definitions

All values are derived under normal operating conditions at 40°C operating temperature.

Table 8. DEFECT DEFINITIONS

Defect Type	Defect Definition	Number Allowed	Notes
Defective Pixel	Under uniform illumination with mean pixel output of 400 mV, a defective pixel deviates by more than 15% from the mean value of all active pixels in its section.	5	1, 2
Bright Defect	Under dark field conditions, a bright defect deviates more than 15 mV from the mean value of all pixels in its section.	0	1, 2
Cluster Defect	Two or more vertically or horizontally adjacent defective pixels.	0	2

1. Sections are 256 (H) × 242 (V) pixel groups, which divide the imager into six equal areas as shown below.
2. Test conditions: Junction Temperature = 40°C, Integration Time = 33 ms and Readout Time = 33 ms.

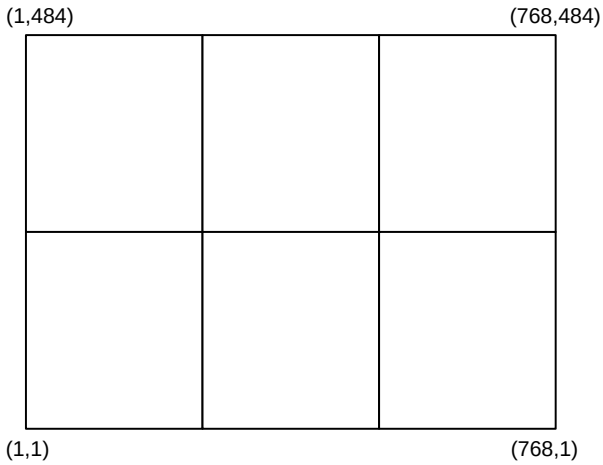


Figure 7.

TYPICAL PERFORMANCE CURVES

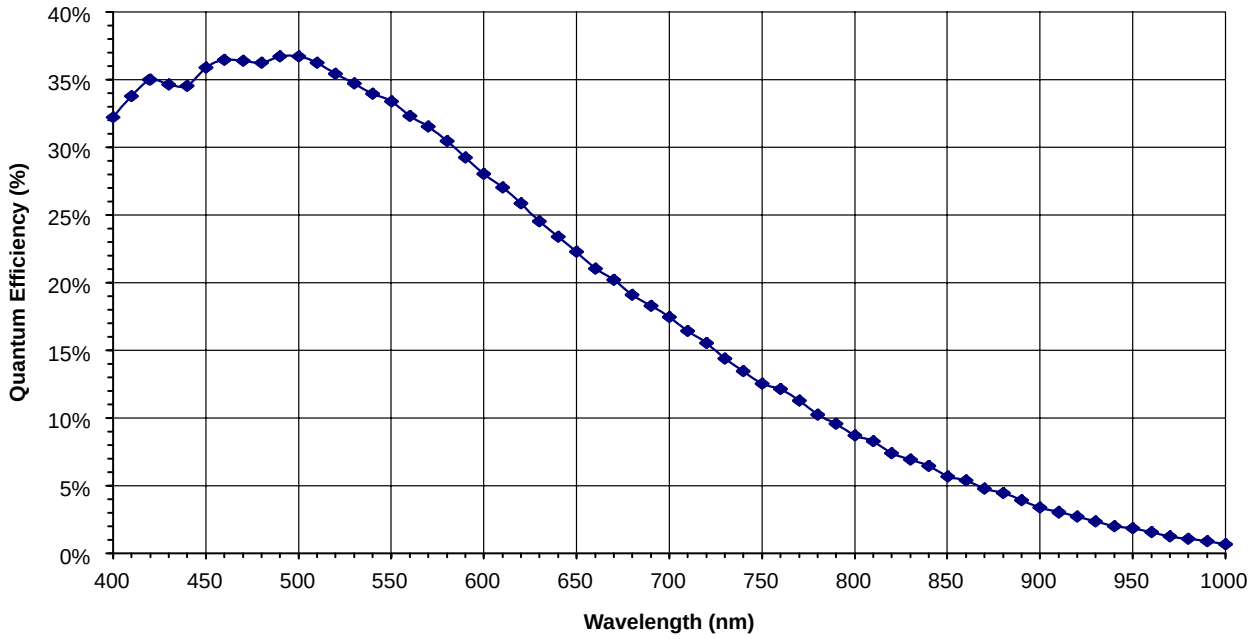


Figure 8. Monochrome with Microlens Quantum Efficiency

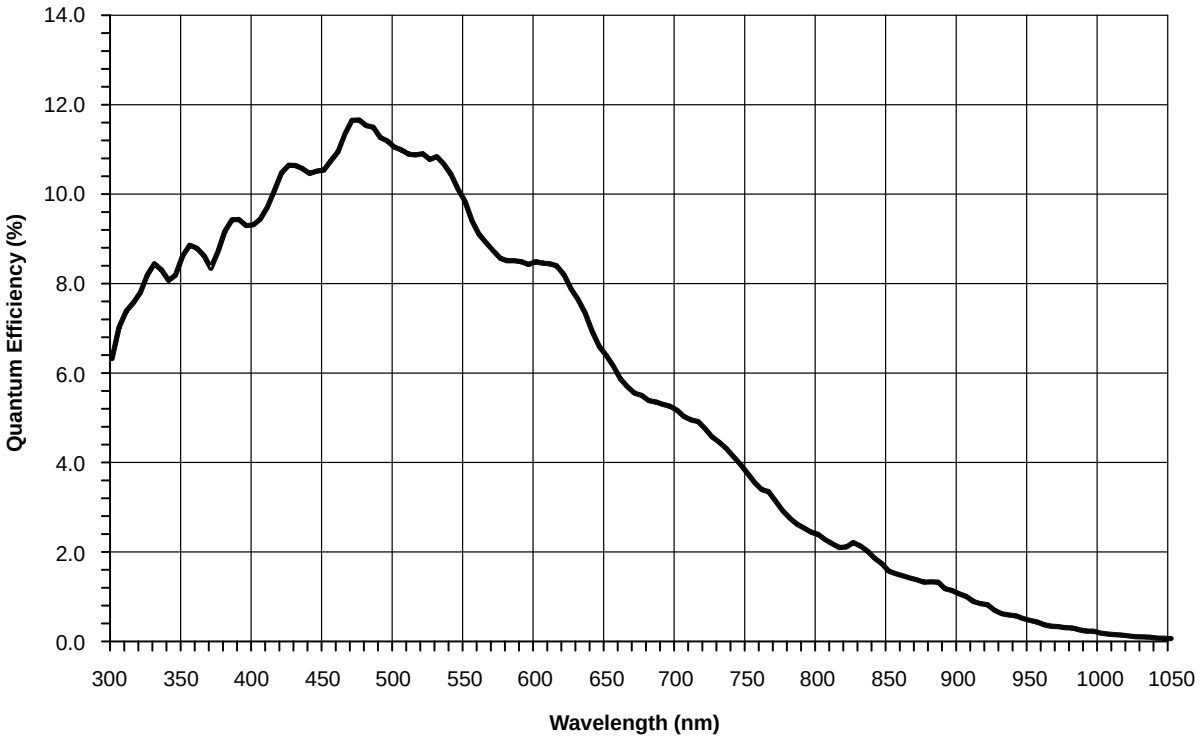


Figure 9. Monochrome, No Microlens, No Cover Glass Quantum Efficiency

OPERATION

Absolute Maximum Ratings

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged.

Table 9. ABSOLUTE MAXIMUM RATINGS

Rating	Description	Min.	Max.	Unit	Notes
Temperature (@ 10% ±5% RH)	Operation to Specification	25	40	°C	
	Operation Without Damage	−25	55	°C	
	Storage	−25	70	°C	
Voltage (Between Pins)	SUB−WELL	0	50	V	1, 3
	VRD, VDD, and VSS−WELL	0	25	V	2
	All Clocks − WELL	−	17	V	2
	ϕV1 − ϕV2	−	17	V	2
	ϕH1 − ϕH2	−	17	V	2
	ϕH1, ϕH2 − ϕV2	−	17	V	2
	ϕH2 − OG	−	17	V	2
	All Clocks − LTSH	−	17	V	2
	VLG, OG − WELL	−	17	V	2
	All Gates – LTSH	−	17	V	2
Current	Output Bias Current (I_{DD})	−	10	mA	
Capacitance	Output Load Capacitance (C_{LOAD})	−	10	pF	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Under normal operating conditions the substrate voltage should be above +7 V, but may be pulsed to 40 V for electronic shuttering.
2. Care must be taken in handling so as not to create static discharge which may permanently damage the device.
3. Refer to Application Note *Using Interline CCD Image Sensors s in High Intensity Visible Lighting Conditions*.

DC Bias Operating Conditions

Table 10. DC BIAS OPERATING CONDITIONS

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
Output Gate	OG	1.5	2	2.5	V	
Reset Drain	V_{RD}	10	10.5	11	V	
Output Amplifier Return	V_{SS}	0.4	0.5	0.6	V	
Output Amplifier Load Gate	V_{LG}	1.7	2	2.5	V	
Output Amplifier Supply	V_{DD}	14.5	15	15.5	V	
Well	WELL	−	0	−	V	
Lightshield	LTSH	−	0	−	V	
Substrate	SUB	7	V_{AB}	25	V	1, 4
Output Bias Current	I_{OUT}	3	5	7	mA	2
ESD Bias	ESD	−	−10	−	V	3

1. The operating value of the substrate voltage, V_{AB}, will be marked on the shipping container for each device. The substrate is clocked in electronic shutter mode operation. A shutter pulse with voltage less than 50 V for less than 100 μs is allowed. See AC Clock Level Conditions and AC Timing Requirements. Well and substrate biases should be established before other gate and diode potentials are applied.
2. A 1.8 kΩ resistor between V_{OUT} and ground is recommended to obtain I_{OUT} = 5 mA. V_{OUT} must not be shorted to ground.
3. Pins 11 and 13 are biased to –10 V. The ESD bias must be at least 1 V more negative than ϕH1 and ϕH2 during sensor operation AND during camera power turn on.
4. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

AC Operating Conditions

Table 11. CLOCK LEVELS

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
Vertical CCD Clocks − High	ϕV1H, ϕV2H	14.5	14.7	15	V	1
Vertical CCD Clocks − Mid	ϕV1M, ϕV2M	−0.5	−0.2	0	V	1
Vertical CCD Clocks − Low	ϕV1L, ϕV2L	−9	−8	−7	V	1
Horizontal CCD Clocks − High	ϕH1H, ϕH2H	1	2	3	V	1
Horizontal CCD Clocks − Low	ϕH1L, ϕH2L	−10	−9	−8	V	1
Reset Clock − High	ϕRH	7	8	9	V	
Reset Clock − Low	ϕRL	2	3	4	V	
For Electronic Shutter Pulse Only	VES (SUB)	40	42	45	V	2, 3

1. For best results, the CCD clock swings must be maintained at (or greater than) the values indicted by the nominal level conditions noted above.
2. This pulse, used only for electronic shutter mode operation, is applied to the substrate, as described in the Electronic Shutter section of this document. Dynamic resistance is 3 kΩ and typical DC current is 3 mA at VSUB = 40 V.
3. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

Clock Line Capacitances

Table 12. CLOCK LINE CAPACITANCES

Description	Symbol	Typical	Unit
Vertical CCD Clocks − Well	C ϕV1, ϕV2 (A, B combined)	10	nF
VCCD Clock Phase 1 − VCCD Clock Phase 2	C ϕV1 − ϕV2 (A, B combined)	1.5	nF
Horizontal CCD Clocks − Well	C ϕH1, ϕH2	150	pF
HCCD Clock Phase 1 − HCCD Clock Phase 2	C ϕH1 − ϕH2	60	pF
Reset Clock − Well	C ϕR	5	pF
For Electronic Shutter Pulse	C SUB	400	pF

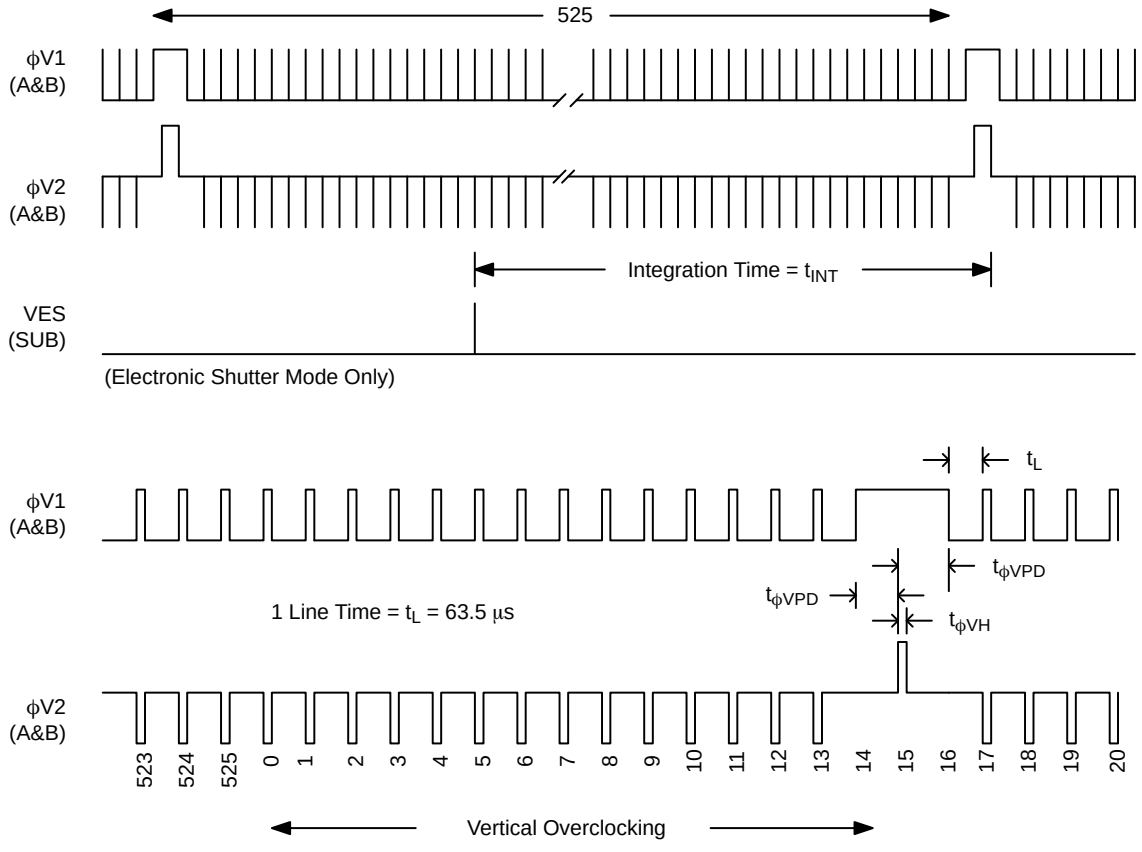
TIMING

Table 13. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
Vertical High Level Duration	$t_{\phi VH}$	5	17	20	μs	
Vertical Transfer Time	$t_{\phi V}$	−	2.8	−	μs	
Vertical Pedestal Delay	$t_{\phi VPD}$	10	−	−	μs	
Horizontal Delay	$t_{\phi HD}$	5.3	−	−	μs	
Reset Duration	$t_{\phi R}$	15	20	25	ns	1
Horizontal Clock Frequency	$f_{\phi H}$	−	−	14.32	MHz	
Line Time	t_L	−	63.5	−	μs	
Vertical Delay	$t_{\phi VD}$	200	−	−	ns	
Horizontal Delay with Electronic Shutter	$t_{\phi HVES}$	1	−	−	μs	
Clamp Delay	t_{CD}	−	−	−	ns	2
Sample Delay	t_{SD}	−	−	−	ns	2
Electronic Shutter Pulse Duration	t_{ES}	4	5	−	μs	3

1. The rising edge of ϕR should be coincident with the rising edge of ϕH2, within ±5 ns.
2. The clamp delay and sample delay should be adjusted for optimum results.
3. This pulse is used only with electronic shuttering and should not be used during horizontal readout. The electronic shutter pulse should be hidden in the horizontal retrace interval.

Frame Timing



NOTE: When no electronic shutter is used, the integration time is equal to the frame time.

Figure 10. Frame Timing

Line Timing

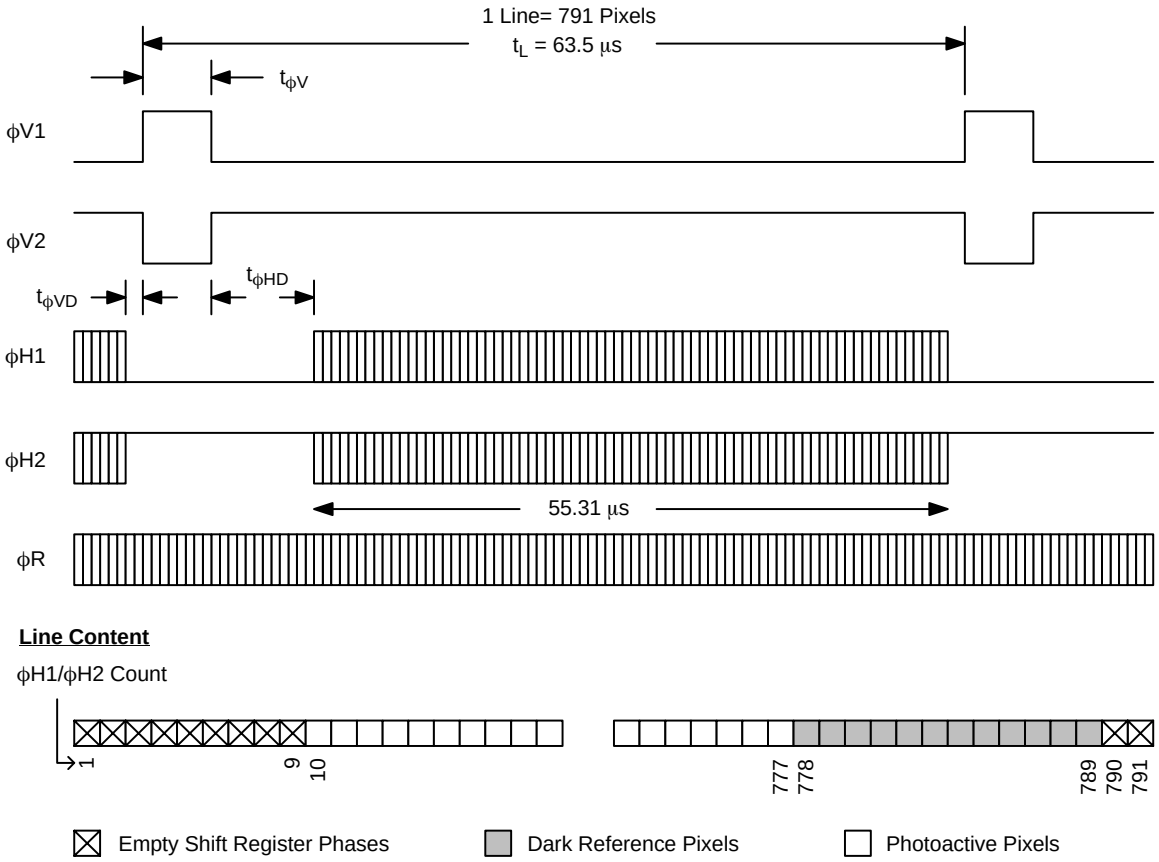


Figure 11. Line Timing

Pixel Timing

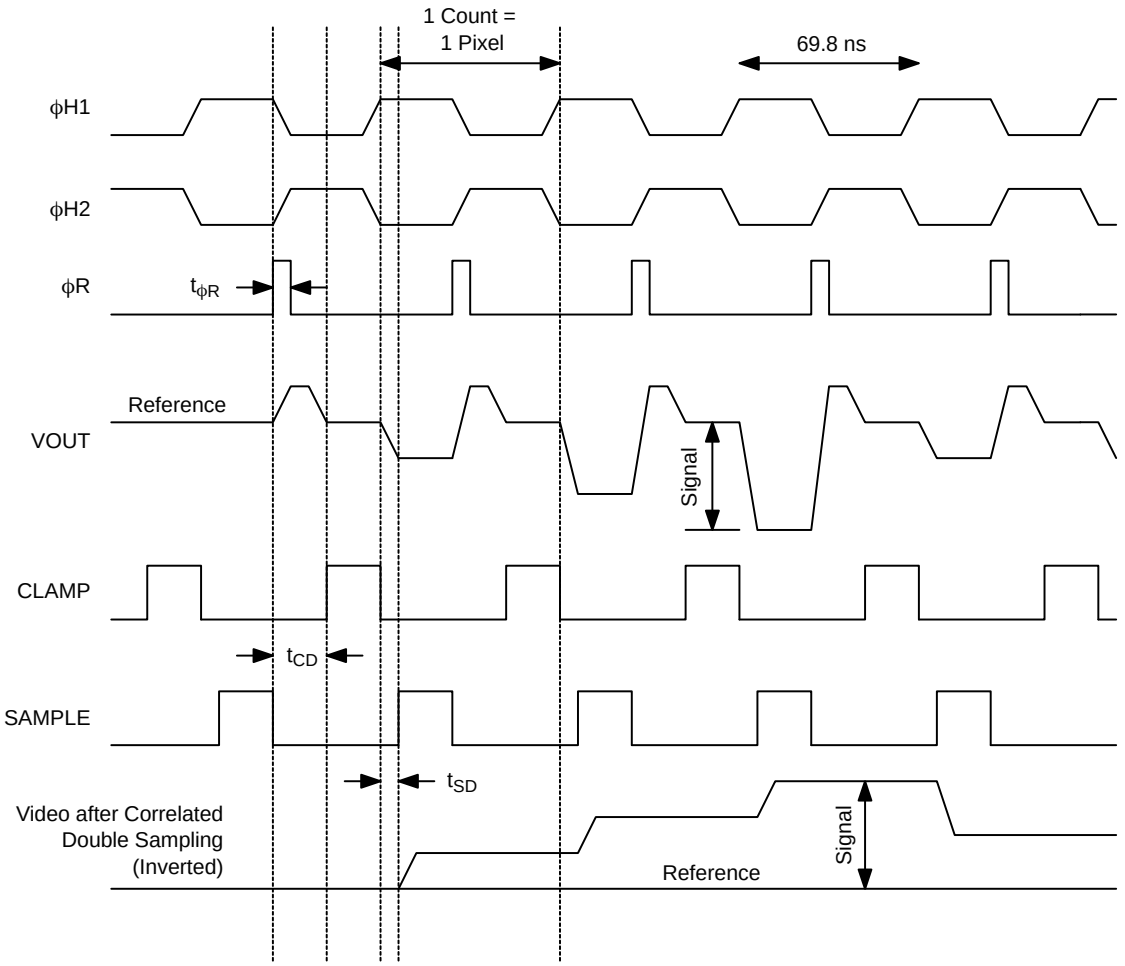


Figure 12. Pixel Timing

Electronic Shutter Timing

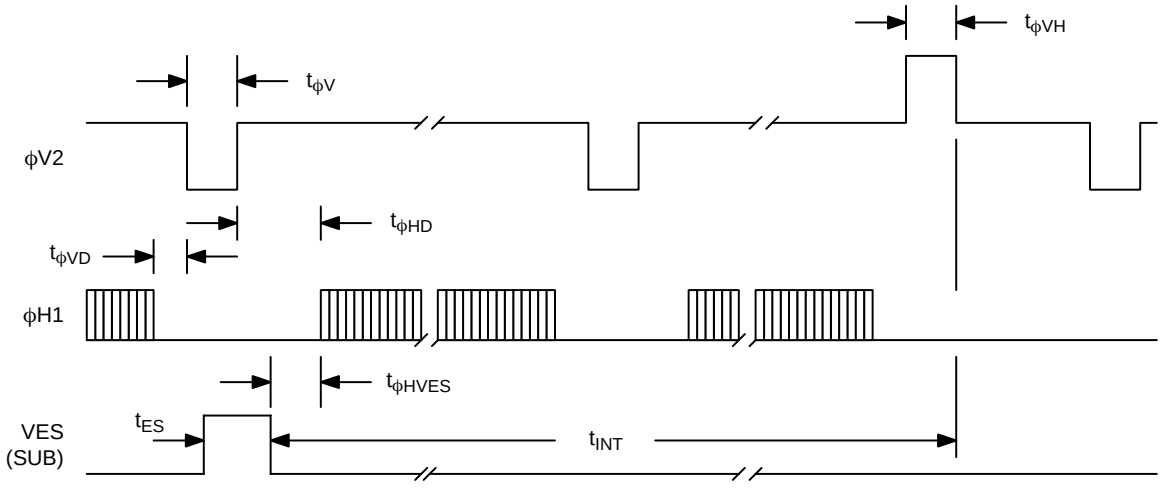


Figure 13. Electronic Shutter Timing

CCD Clock Waveform Conditions

Table 14. CCD CLOCK WAVEFORM CONDITIONS

Description	Symbol	t_{WH}	t_{WL}	t_R	t_F	Unit	Note
Vertical CCD Clocks − Phase 1	ϕV1M	2.8	59.8	0.6	0.3	μs	1
Vertical CCD Clocks − Phase 2	ϕV2M	60	2.5	0.5	0.5	μs	1
Vertical CCD Clocks − Phase 2, High	ϕV2H	17	−	0.5	0.5	μs	1
Horizontal CCD Clocks − Phase 1	ϕH1	25	27	8.5	8.5	ns	1
Horizontal CCD Clocks − Phase 2	ϕH2	25	27	8.5	8.5	ns	1
Reset Clock	ϕR	20	40	4	5	ns	1
For Electronic Shutter Pulse Only	VES (SUB)	5	−	0.2	0.2	μs	1

1. Typical values measured with clocks connected to image sensor device.

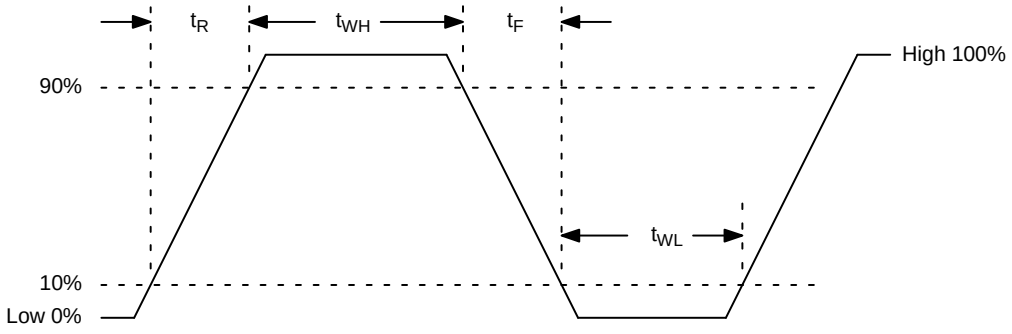


Figure 14. CCD Clock Waveform

STORAGE AND HANDLING

Table 15. STORAGE CONDITIONS

Item	Description	Min.	Max.	Unit	Conditions	Notes
Operation to Specification	Temperature	25	40	°C	@ 10% ±5% RH	1, 2
	Humidity	10±5	86±5	% RH	@ 36±2°C Temp.	1, 2
Operation without Damage	Temperature	−25	55	°C	@ 10% ±5% RH	2, 3
Storage	Temperature	−25	70	°C	@ 10% ±5% RH	2, 4
	Humidity	−	90±5	% RH	@ 49±2°C Temp.	2, 4

1. The image sensor shall meet the specifications of this document while operating at these conditions.
2. The tolerance on all relative humidity values is provided due to limitations in measurement instrument accuracy.
3. The image sensor shall continue to function but not necessarily meet the specifications of this document while operating at the specified conditions.
4. The image sensor shall meet the specifications of this document after storage for 15 days at the specified conditions.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on environmental exposure, please download the *Using Interline CCD Image Sensors in High Intensity Lighting Conditions* Application Note (AND9183/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

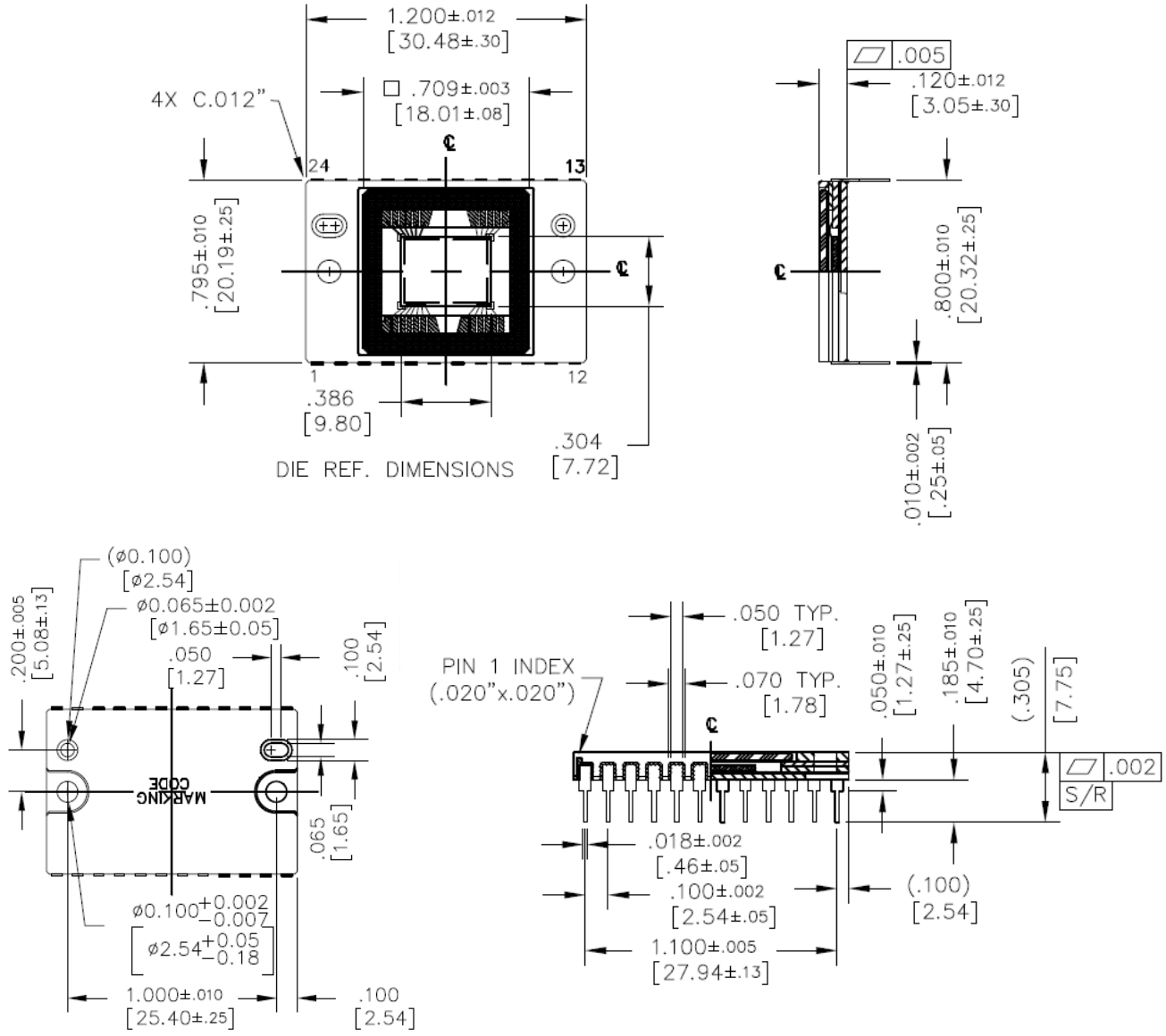
For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

Completed Assembly



Notes:

1. See Ordering Information for Marking Code.
2. Cover Glass is manually placed and visually aligned over die – location accuracy is not guaranteed.
3. Units: Inches [mm].

Figure 15. Completed Assembly

Die to Package Alignment

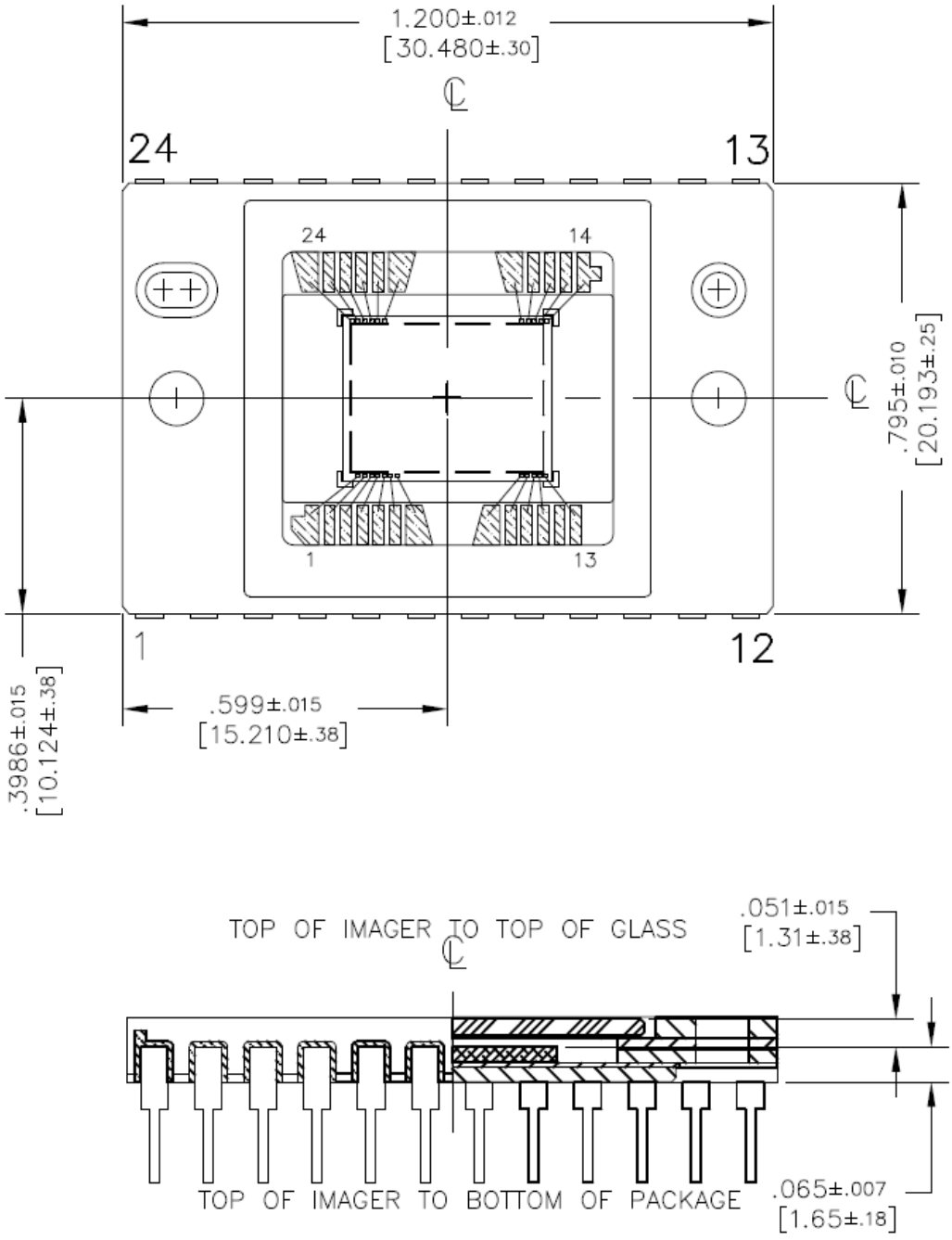
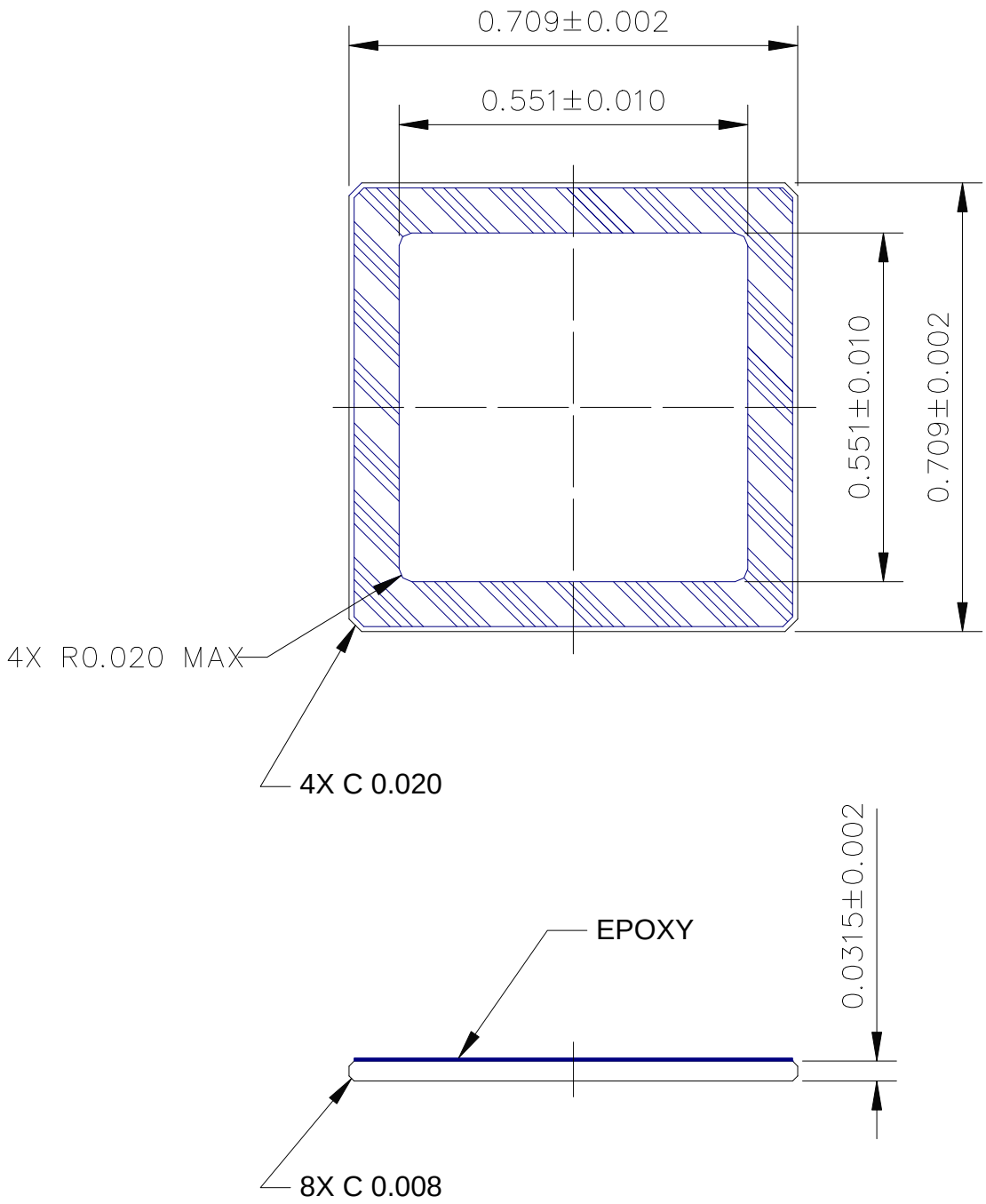


Figure 16. Die to Package Alignment

Glass



Notes:
1. Dust/Scratch Count: 10 microns max
2. Epoxy Thickness: 0.002″ – 0.005″
3. Glass: Schott D−263T eco or equivalent
4. Units: Inches

Figure 17. Glass Drawing

Glass Transmission

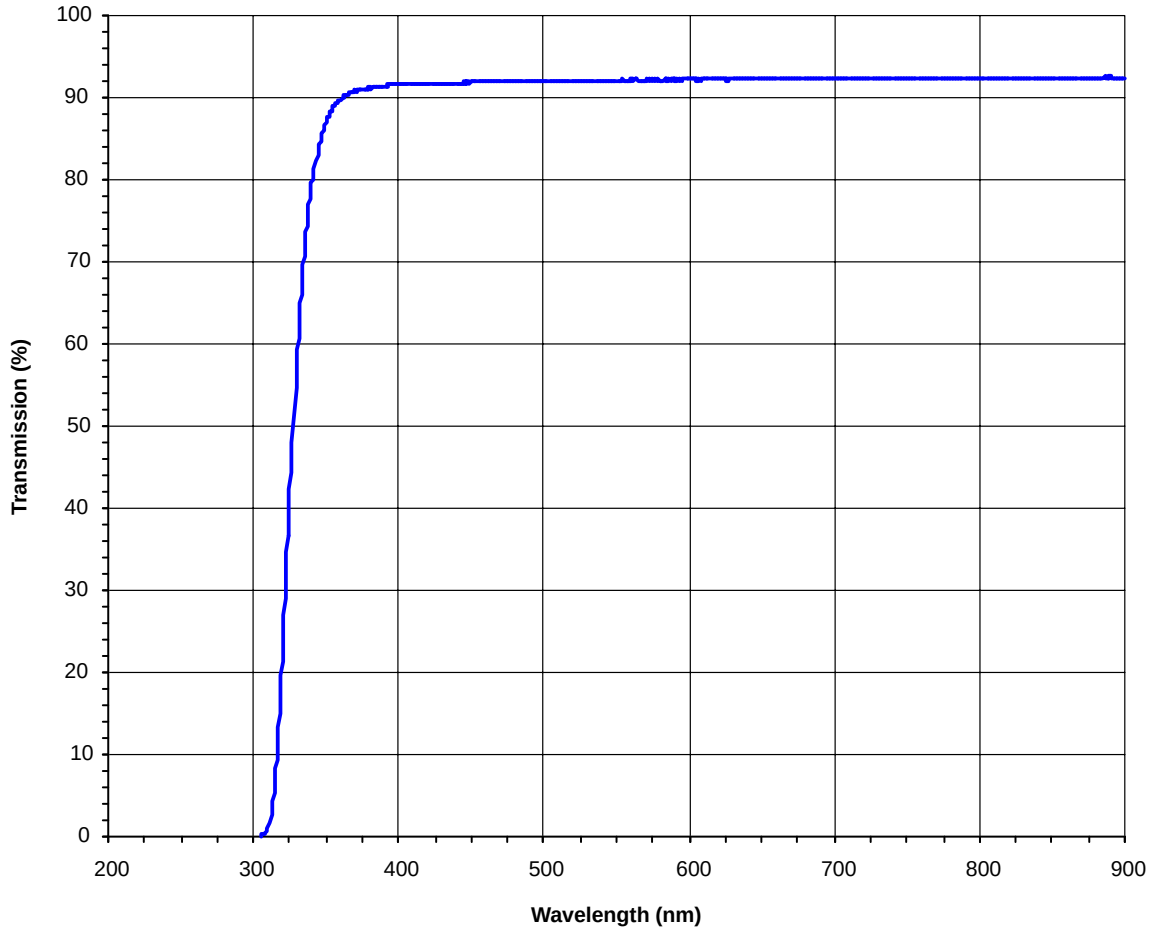


Figure 18. Glass Transmission

PUBLICATION ORDERING INFORMATION

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