

μ A8T26A • μ A8T28 Quad 3-State Bus Transceivers

Interface Products

Description

μ A8T26A and μ A8T28 are Quad 3-State Bus Transceivers featuring MPU or MOS compatibility. Both parts feature high-impedance pnp inputs and high-speed operation made possible by the use of Schottky transistor technology.

These devices are useful as bus extenders in systems employing the F6800, F3870 or other comparable MPU families. Maximum input current of 200 μ A at the device input pins assures proper operation despite limited drive capability of the MPU chip.

The μ A8T26A/28 are identical to the NE8T26A/28 or the MC8T26A/28.

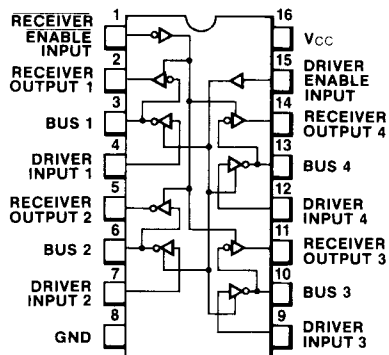
- μ A8T26A—INVERTING BUS
- μ A8T28—NON-INVERTING
- MPU COMPATIBLE
- HIGH-IMPEDANCE pnp INPUTS
- HIGH-SPEED SCHOTTKY TECHNOLOGY
- +5 V SINGLE SUPPLY OPERATION
- 3-STATE DRIVERS AND RECEIVERS

Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Power Supply Voltage (V_{CC})	8.0 V
Input Voltage (V_I)	5.5 V
Junction Temperature (T_{J})	
Ceramic DIP	175°C
Molded DIP	150°C
Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Pin Temperature	
Molded DIP (Soldering, 10 s)	260°C
Ceramic DIP (Soldering, 60 s)	300°C

Connection Diagrams 16-Pin DIP

μ A8T26A



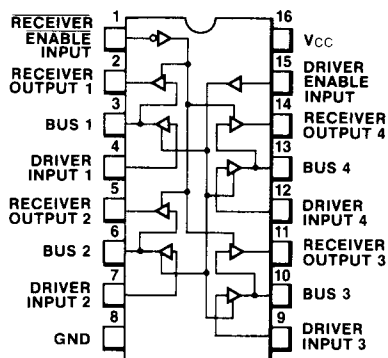
(Top View)

Order Information

Type	Package	Code	Part No.
μ A8T26A	Ceramic DIP	6B	μ A8T26ADM
μ A8T26A	Ceramic DIP	6B	μ A8T26ADC
μ A8T26A	Molded DIP	9B	μ A8T26APC

Connection Diagram

μ A8T28

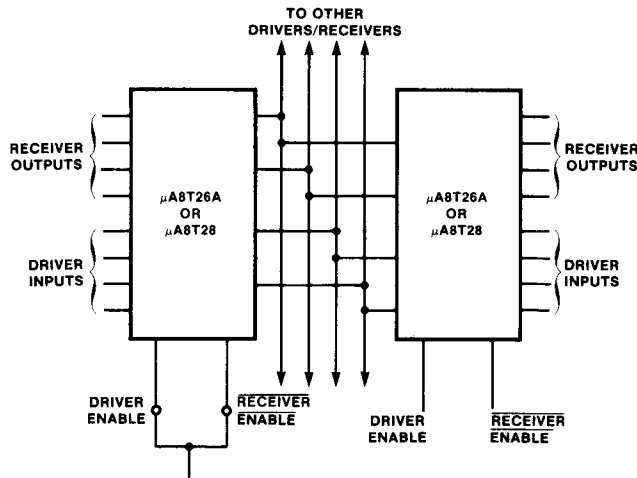


(Top View)

Order Information

Type	Package	Code	Part No.
μ A8T28	Ceramic DIP	6B	μ A8T28DM
μ A8T28	Ceramic DIP	6B	μ A8T28DC
μ A8T28	Molded DIP	9B	μ A8T28PC

Bidirectional Bus Application



DC Characteristics 4.75 V ≤ V_{CC} ≤ 5.25 V for 0°C ≤ T_A ≤ 70°C, and 4.5 V ≤ V_{CC} ≤ 5.5 V for -55°C ≤ T_A ≤ +125°C, unless otherwise noted

Symbol	Characteristic	Min	Typ	Max	Unit
I _{IL} (\overline{RE})	Input Current, LOW Logic State Receiver Enable Input, V _{IL} (RE) = 0.4 V			-200	μA
I _{IL} (DE)	Driver Enable Input, V _{IL} (DE) = 0.4 V			-200	
I _{IL} (D)	Driver Input, V _{IL} (D) = 0.4 V			-200	
I _{IL} (B)	Bus Receiver Input, V _{IL} (B) = 0.4 V			-200	
I _{IL} (D)DIS	Input Disabled Current, LOW Logic State Driver Input, V _{IL} (D) = 0.4 V			-25	μA
I _{IH} (\overline{RE})	Input Current, HIGH Logic State Receiver Enable Input, V _{IH} (RE) = 5.25 V			25	μA
I _{IH} (DE)	Driver Enable Input, V _{IH} (DE) = 5.25 V			25	
I _{IH} (D)	Driver Input, V _{IH} (D) = 5.25 V			25	
I _{IH} (B)	Receiver Input, V _{IH} (B) = 5.25 V (μA8T26 only)			100	
V _{IL} (\overline{RE})	Input Voltage, LOW Logic State Receiver Enable Input			0.85	V
V _{IL} (DE)	Driver Enable Input			0.85	
V _{IL} (D)	Driver Input			0.85	
V _{IL} (B)	Receiver Input			0.85	
V _{IH} (RE)	Input Voltage, HIGH Logic State Receiver Enable Input	2.0			V
V _{IH} (DE)	Driver Enable Input	2.0			
V _{IH} (D)	Driver Input	2.0			
V _{IH} (B)	Receiver Input	2.0			
V _{OL} (B)	Output Voltage, LOW Logic State Bus Driver Output, I _{OL} (B) = 48 mA			0.5	V
V _{OL} (R)	Receiver Output, I _{OL} (R) = 20 mA			0.5	
V _{OH} (B)	Output Voltage, HIGH Logic State Bus Driver Output, I _{OH} (B) = -10 mA	2.4	3.1		V
V _{OH} (R)	Receiver Output, I _{OH} (R) = -2.0 mA	2.4	3.1		
	Receiver Output, I _{OH} (R) = -100 μA, V _{CC} = 5.0 V	3.5			
I _{OHL} (B)	Output Disabled Leakage Current HIGH Logic State Bus Driver Output, V _{OH} (B) = 2.4 V			100	μA
I _{OHL} (R)	Receiver Output, V _{OH} (R) = 2.4 V			100	

DC Characteristics (Cont.) $4.75\text{ V} \leq V_{CC} \leq 5.25\text{ V}$ for $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, and $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted

Symbol	Characteristic	Min	Typ	Max	Unit
$I_{OLL(B)}$ $I_{OLL(R)}$	Output Disabled Leakage Current LOW Logic State Bus Output, $V_{OL(B)} = 0.5\text{ V}$ Receiver Output, $V_{OL(R)} = 0.5\text{ V}$			-100 -100	μA
$V_{IC(DE)}$ $V_{IC(RE)}$ $V_{IC(D)}$	Input Clamp Voltage Driver Enable Input $I_{IC(DE)} = -12\text{ mA}$ Receiver Enable Input $I_{IC(RE)} = -12\text{ mA}$ Driver Input $I_{IC(D)} = -12\text{ mA}$			-1.0 -1.0 -1.0	V
$I_{OS(B)}$ $I_{OS(R)}$	Output Short-Circuit Current, $V_{CC} = 5.25\text{ V}$, Note Bus Driver Output Receiver Output	-50 -30	80 50	-150 -75	mA
I_{CC}	Power Supply Current $V_{CC} = 5.25\text{ V}$		50	87	mA

Note

Only one output may be short-circuited at a time

μA8T26A AC Characteristics Unless otherwise noted, specifications apply at $T_A = 25^\circ\text{C}$ and $V_{CC} = 5.0\text{ V}$.

Symbol	Characteristic	Figure	Typ	Max	Unit
$t_{PLH(R)}$	Propagation Delay Time from Receiver (Bus) Input to HIGH Logic State Receiver Output	1	9	14	ns
$t_{PHL(R)}$	Propagation Delay Time from Receiver (Bus) Input to LOW Logic State Receiver Output	1	6	14	ns
$t_{PLH(D)}$	Propagation Delay Time from Driver Input to HIGH Logic State Driver (Bus) Output	2	10	14	ns
$t_{PHL(D)}$	Propagation Delay Time from Driver Input to LOW Logic State Driver (Bus) Output	2	10	14	ns
$t_{PLZ(RE)}$	Propagation Delay Time from Receiver Enable Input to HIGH Impedance (Open) Logic State Receiver Output	3	10	15	ns
$t_{PZL(RE)}$	Propagation Delay Time from Receiver Enable Input to LOW Logic Level Receiver Output	3	15	20	ns
$t_{PLZ(DE)}$	Propagation Delay Time from Driver Enable Input to HIGH Impedance Logic State Driver (Bus) Output	4	15	20	ns
$t_{PZL(DE)}$	Propagation Delay Time from Driver Enable Input to LOW Logic State Driver (Bus) Output	4	19	25	ns

μA8T28 AC Characteristics $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$ unless otherwise specified.

Symbol	Characteristic	Figure	Typ	Max	Unit
$t_{PLH(R)}$ $t_{PHL(R)}$	Propagation Delay Time—Receiver ($C_L = 30\text{ pF}$)	5	-12 -9	17 17	ns
$t_{PLH(D)}$ $t_{PHL(D)}$	Propagation Delay Time—Driver ($C_L = 300\text{ pF}$)	6	-13 -13	17 17	ns
$t_{PZL(RE)}$	Propagation Delay Time—Receiver Enable ($C_L = 30\text{ pF}$)	7	-18	23	ns
$t_{PLZ(RE)}$			-13	18	
$t_{PZL(DE)}$	Propagation Delay Time—Driver Enable ($C_L = 300\text{ pF}$)	8	-21	28	ns
$t_{PLZ(DE)}$			-18	23	

Fig. 1 μ A8T26A Test Circuit and Waveforms for Propagation Delay Time from Bus (Receiver) Input to Receiver Output, $t_{PLH(R)}$ and $t_{PHL(R)}$

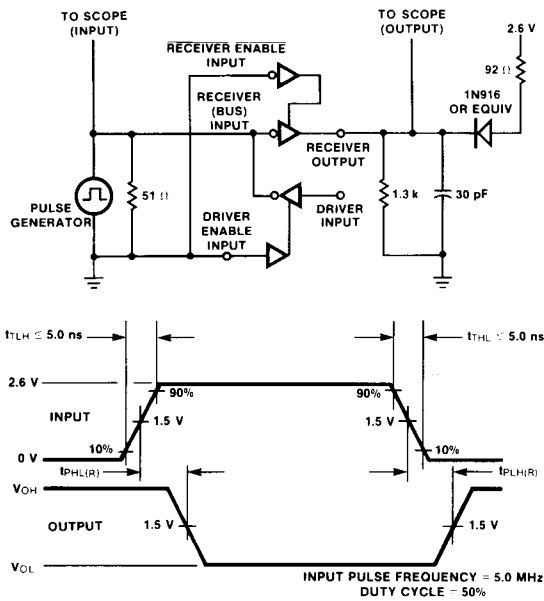


Fig. 3 μ A8T26A Test Circuit and Waveforms for Propagation Delay Time from Receiver Enable Input to Receiver Output, $t_{PLZ(RE)}$ and $t_{PZL(RE)}$

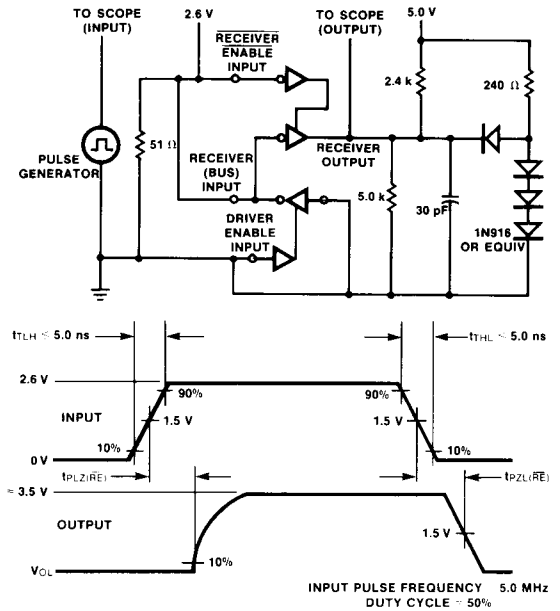


Fig. 2 μ A8T26A Test Circuit and Waveforms for Propagation Delay Time from Driver Input to Bus (Driver) Output, $t_{PLH(D)}$ and $t_{PHL(D)}$

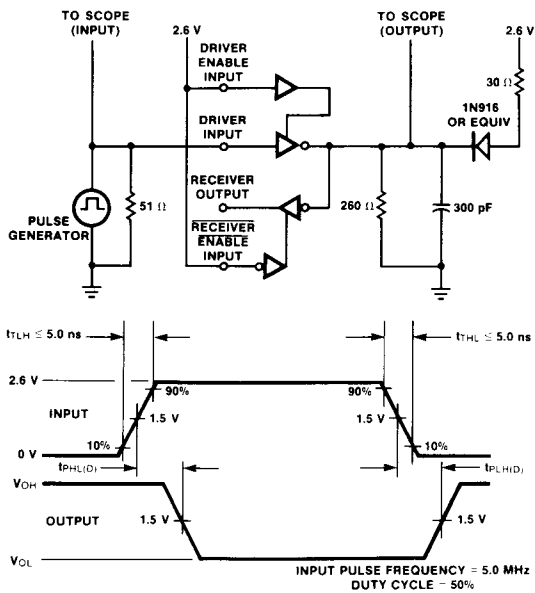


Fig. 4 μ A8T26A Test Circuit and Waveforms for Propagation Delay Time from Driver Enable Input to Driver (Bus) Output, $t_{PLZ(DE)}$ and $t_{PZL(DE)}$

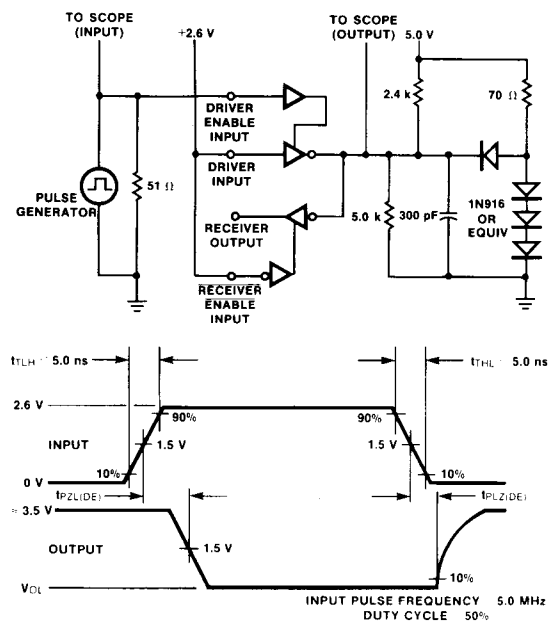


Fig. 5 μ A8T28 Test Circuit and Waveforms for Propagation Delay Time from Bus (Receiver) Input to Receiver Output, $t_{PLH(R)}$ and $t_{PHL(R)}$

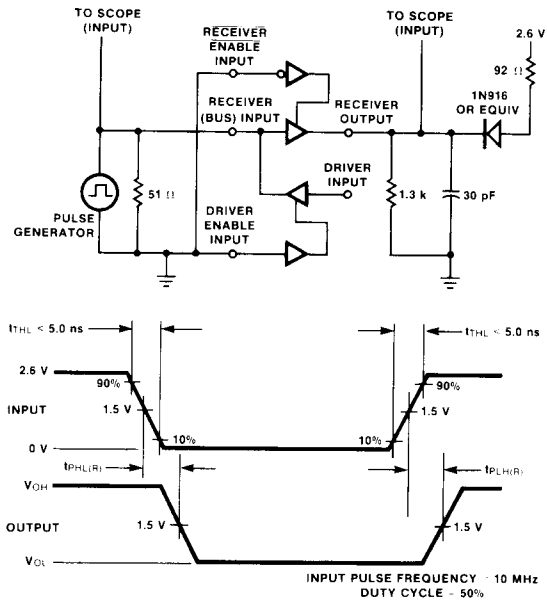


Fig. 6 μ A8T28 Test Circuit and Waveforms for Propagation Delay Time from Driver Input to Bus (Driver) Output, $t_{PLH(D)}$ and $t_{PHL(D)}$

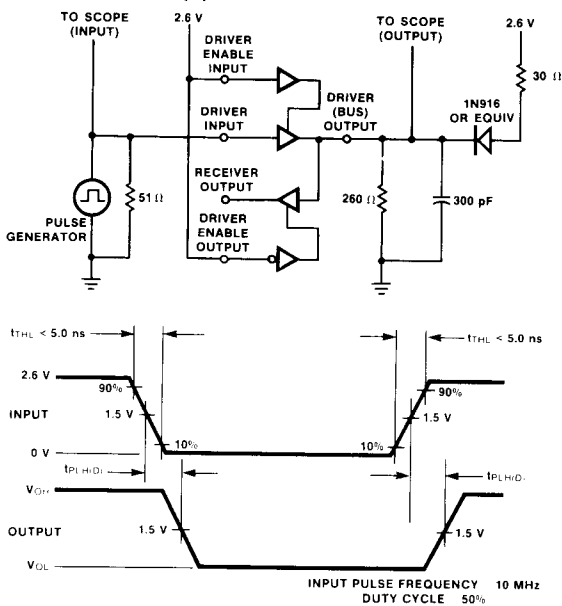


Fig. 7 μ A8T28 Test Circuit and Waveforms for Propagation Delay Time from Receiver Enable Input to Receiver Output, $t_{PLZ(RE)}$ and $t_{PZL(RE)}$

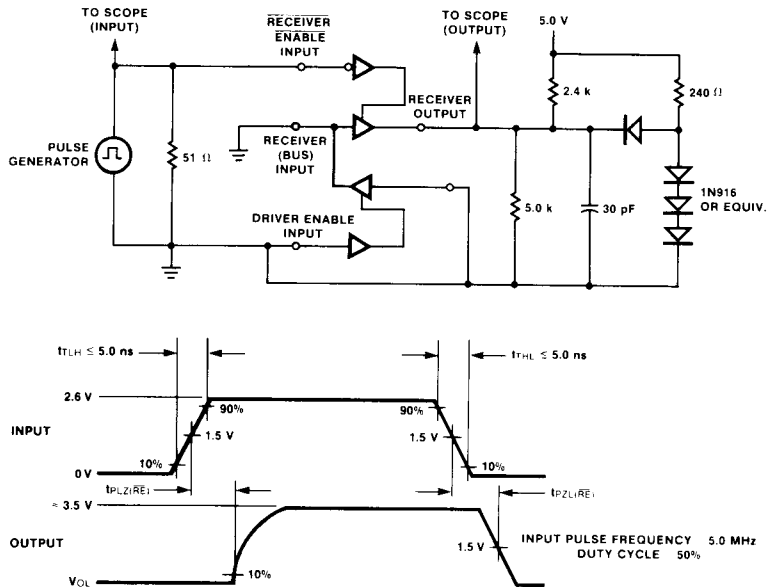


Fig. 8 μ A8T28 Test Circuit and Waveforms for Propagation Delay Time from Driver Enable Input to Driver (Bus) Output, $t_{pLZ(DE)}$ and $t_{pZL(DE)}$

