

This IC is a protection IC for lithium-ion rechargeable batteries, which includes high-accuracy voltage detection circuits and delay circuits. It is suitable for protecting 4-serial or 5-serial cell lithium-ion rechargeable battery packs from overcharge, overdischarge, and overcurrent.

■ Features

- High-accuracy voltage detection for each cell

| | | |
|-----------------------------------|----------------------------------|------------------|
| Overcharge detection voltage n | 3.900 V to 4.500 V (25 mV step) | Accuracy ±20 mV |
| Overcharge release voltage n | 3.500 V to 4.500 V* ¹ | Accuracy ±50 mV |
| Overdischarge detection voltage n | 2.000 V to 3.200 V (100 mV step) | Accuracy ±50 mV |
| Overdischarge release voltage n | 2.000 V to 3.400 V* ² | Accuracy ±100 mV |
- Three-level discharge overcurrent detection

| | | |
|---|------------------------------|-----------------|
| Discharge overcurrent 1 detection voltage | 10 mV to 200 mV (5 mV step) | Accuracy ±5 mV |
| Discharge overcurrent 2 detection voltage | 20 mV to 300 mV (5 mV step) | Accuracy ±10 mV |
| Load short-circuiting detection voltage | 50 mV to 400 mV (10 mV step) | Accuracy ±20 mV |
- Charge overcurrent detection

| | | |
|--------------------------------------|-------------------------------|----------------|
| Charge overcurrent detection voltage | -200 mV to -10 mV (5 mV step) | Accuracy ±5 mV |
|--------------------------------------|-------------------------------|----------------|
- Discharge overcurrent 1 detection delay time is settable by an external capacitor (The other delay time are internally fixed)
- Power saving control by a control pin
- 0 V battery charge: Enabled, inhibited
- Power-down function: Available, unavailable
- Release condition of discharge overcurrent status: Load disconnection, charger connection
- Output voltage of CO and DO pin is limited to VC2 pin voltage. (S-82B5A Series)
- High-withstand voltage: Absolute maximum rating 28.0 V
- Wide operating voltage range: 5.0 V to 24.0 V
- Wide operation temperature range: Ta = -40°C to +85°C
- Low current consumption

| | |
|----------------------|---------------------------------------|
| During operation: | 4.0 μA typ., 8.0 μA max. (Ta = +25°C) |
| During power-down: | 0.1 μA max. (Ta = +25°C) |
| During power-saving: | 0.1 μA max. (Ta = +25°C) |
- Lead-free (Sn 100%), halogen-free

*1. Overcharge release voltage = Overcharge detection voltage – Overcharge hysteresis voltage
(Overcharge hysteresis voltage n can be selected from a range of 0 V to 0.4 V in 50 mV steps.)

*2. Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage n can be selected from a range of 0 V to 0.7 V in 100 mV steps.)

Remark n = 1, 2, 3, 4, 5

■ Applications

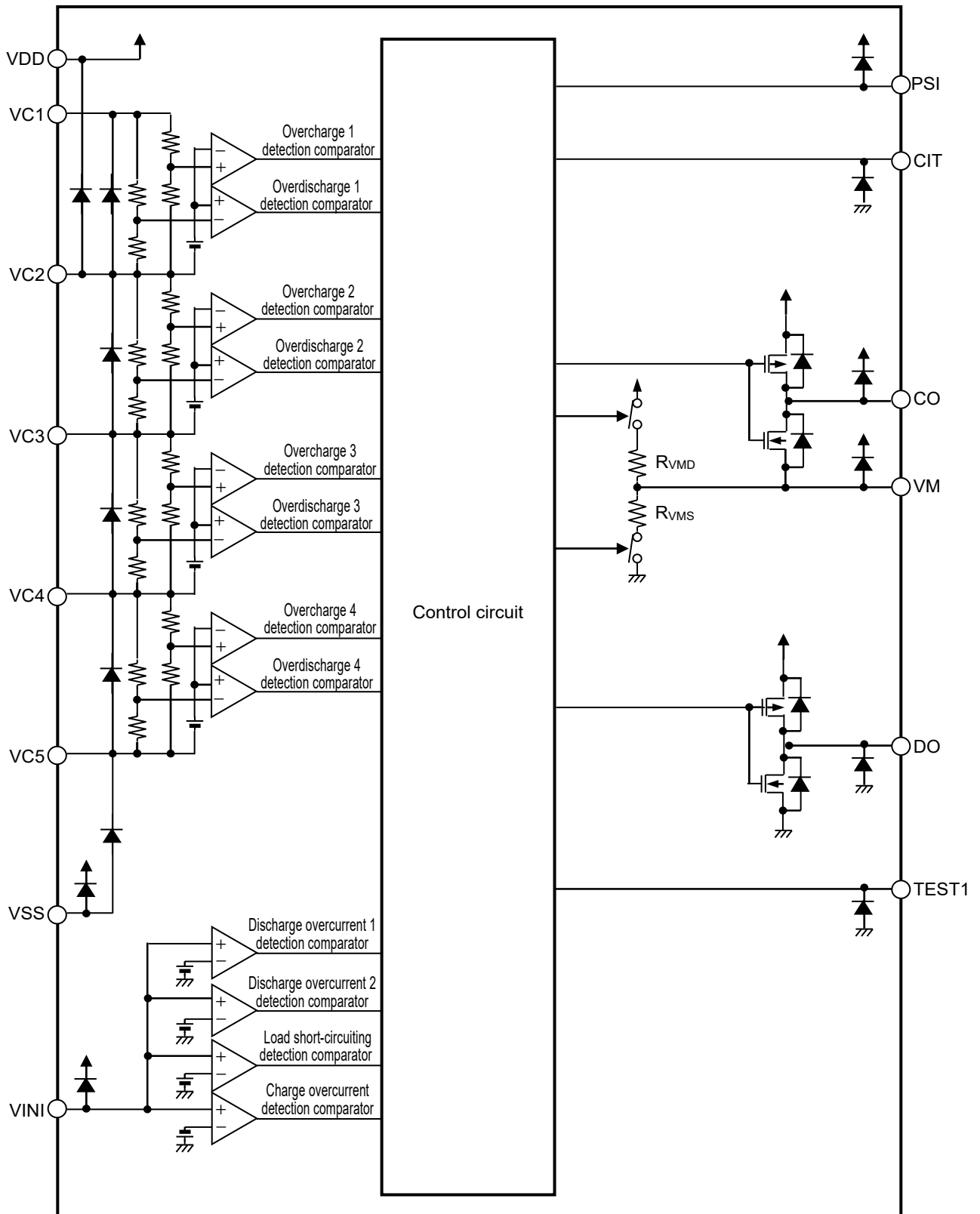
- Lithium-ion rechargeable battery packs

■ Package

- 16-Pin TSSOP

■ **Block Diagram**

1. **S-82B4A Series**



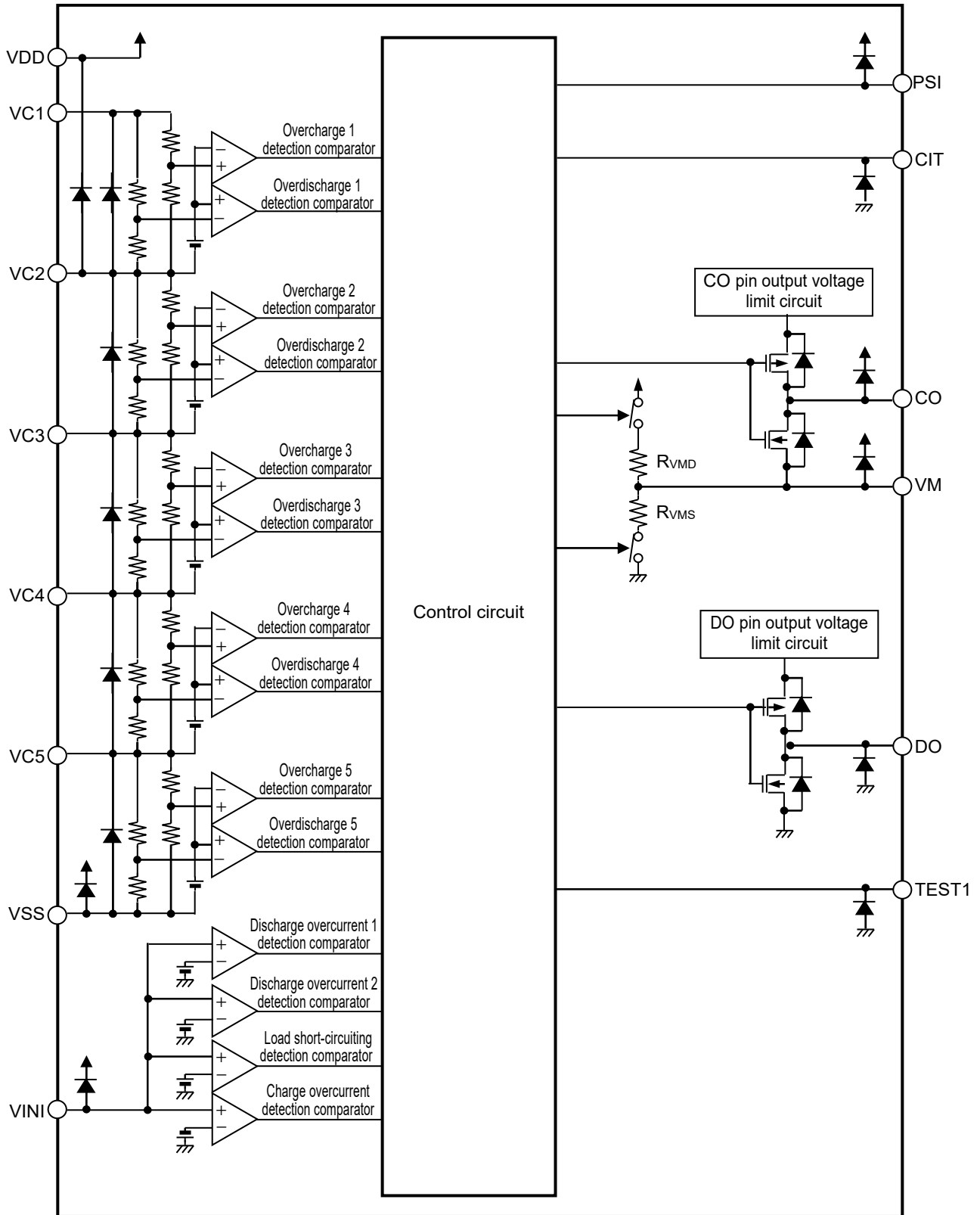
Remark Diodes in the figure are parasitic diodes.

Figure 1
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**BATTERY PROTECTION IC FOR 4-SERIAL OR 5-SERIAL-CELL PACK
S-82B4A/5A Series**

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2. S-82B5A Series

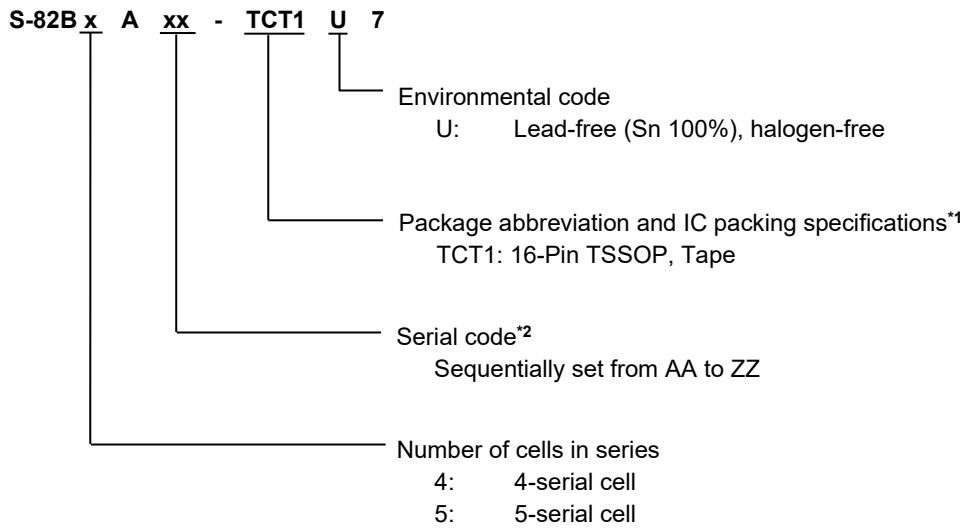


Remark Diodes in the figure are parasitic diodes.

Figure 2

■ **Product Name Structure**

1. **Product name**



*1. Refer to the tape drawing.

*2. Refer to "3. Product name list".

2. **Package**

Table 1 Package Drawing Codes

| Package Name | Dimension | Tape | Reel |
|--------------|--------------|--------------|--------------|
| 16-Pin TSSOP | FT016-A-P-SD | FT016-A-C-SD | FT016-A-R-S1 |

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3. Product name list

3.1 S-82B5A Series

Table 2 (1 / 2)

| Product Name | Overcharge Detection Voltage [V _{CU}] | Overcharge Release Voltage [V _{CL}] | Overdischarge Detection Voltage [V _{DL}] | Overdischarge Release Voltage [V _{DU}] | Discharge Overcurrent 1 Detection Voltage [V _{DIOV1}] | Discharge Overcurrent 2 Detection Voltage [V _{DIOV2}] | Load Short-circuiting Detection Voltage [V _{SHORT}] | Charge Overcurrent Detection Voltage [V _{CIOV}] |
|------------------|---|---|--|--|---|---|---|---|
| S-82B5AAA-TCT1U7 | 4.225 V | 4.025 V | 2.500 V | 2.500 V | 50 mV | 100 mV | 400 mV | -50 mV |

Table 2 (2 / 2)

| Product Name | Delay Time Combination*1 | 0 V Battery Charge | Power-down Function | Release Condition of Discharge Overcurrent Status*2 |
|------------------|--------------------------|--------------------|---------------------|---|
| S-82B5AAA-TCT1U7 | (1) | Inhibited | Available | Load disconnection |

*1. Refer to **Table 3** about the details of the delay time combinations.

*2. Release condition of discharge overcurrent status: Load disconnection, charger connection

Remark Please contact our sales representatives for products other than the above.

Table 3

| Delay Time Combination | Overcharge Detection Delay Time [t _{CU}] | Overdischarge Detection Delay Time [t _{DL}] | Discharge Overcurrent 2 Detection Delay Time [t _{DIOV2}] | Charge Overcurrent Detection Delay Time [t _{CIOV}] |
|------------------------|--|---|--|--|
| (1) | 1.0 s | 128 ms | 16 ms | 16 ms |

Remark The delay times can be changed within the range listed in **Table 4**. For details, please contact our sales representatives.

Table 4

| Delay Time | Symbol | Selection Range | | | | | | | Remark |
|--|--------------------|-----------------|--------|--------|--------|--------|--------|--------|-------------------------------|
| Overcharge detection delay time | t _{CU} | 256 ms | 512 ms | 1.0 s | 2.0 s | - | - | - | Select a value from the left. |
| Overdischarge detection delay time | t _{DL} | 32 ms | 64 ms | 128 ms | 256 ms | 512 ms | 1.0 s | - | Select a value from the left. |
| Discharge overcurrent 2 detection delay time | t _{DIOV2} | 4 ms | 8 ms | 16 ms | 32 ms | 64 ms | - | - | Select a value from the left. |
| Charge overcurrent detection delay time | t _{CIOV} | 4 ms | 8 ms | 16 ms | 32 ms | 64 ms | 128 ms | 256 ms | Select a value from the left. |

■ **Pin Configuration**

1. **16-Pin TSSOP**

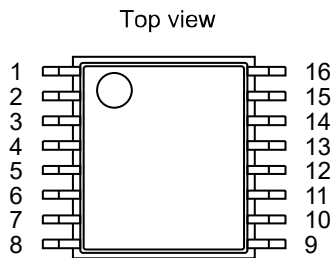


Figure 3

Table 5

| Pin No. | Symbol | Description |
|---------|---------|---|
| 1 | VC1 | Connection pin for battery 1's positive voltage |
| 2 | VC2 | Connection pin for battery 1's negative voltage, Connection pin for battery 2's positive voltage |
| 3 | VC3 | Connection pin for battery 2's negative voltage, Connection pin for battery 3's positive voltage |
| 4 | VC4 | Connection pin for battery 3's negative voltage, Connection pin for battery 4's positive voltage |
| 5 | VC5 | Connection pin for battery 4's negative voltage, Connection pin for battery 5's positive voltage |
| 6 | VSS | Input pin for negative power supply, Connection pin for battery 5's negative voltage |
| 7 | VINI | Voltage detection pin between VSS pin and VINI pin |
| 8 | CIT | Capacitor connection pin for discharge overcurrent 1 detection delay time |
| 9 | NC*1 | No connection |
| 10 | TEST1*2 | Test pin |
| 11 | PSI | Control pin for power-saving |
| 12 | DO | Connection pin of discharge control FET gate (CMOS output) |
| 13 | NC*1 | No connection |
| 14 | CO | Connection pin of charge control FET gate (CMOS output) |
| 15 | VM | Voltage detection pin between VSS pin and VM pin |
| 16 | VDD | Input pin for positive power supply, Connection pin for battery 1's positive voltage |

*1. The NC pin is electrically open. The NC pin can be connected to the VDD pin or the VSS pin.

*2. Set the TEST1 pin open in use.

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■ **Absolute Maximum Ratings**

Table 6

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Applied Pin | Absolute Maximum Rating | Unit |
|---|-------------------|---------------|--|------|
| Input voltage between VDD pin and VSS pin | V _{DS} | VDD | V _{SS} – 0.3 to V _{SS} + 28.0 | V |
| Input pin voltage 1 | V _{IN1} | VC1 | V _{VC2} – 0.3 to V _{VC2} + 6.0 | V |
| | | VC3 | V _{VC4} – 0.3 to V _{DD} + 0.3 ≤ V _{VC4} + 6.0 | V |
| | | VC4 | V _{VC5} – 0.3 to V _{DD} + 0.3 ≤ V _{VC5} + 6.0 | V |
| Input pin voltage 2 | V _{IN2} | VC2 | V _{DD} – 6.0 ≤ V _{VC3} – 0.3 to V _{DD} + 0.3 ≤ V _{VC3} + 6.0 | V |
| Input pin voltage 3 | V _{IN3} | VC5 | V _{SS} – 0.3 to V _{DD} + 0.3 ≤ V _{SS} + 6.0 | V |
| Input pin voltage 4 | V _{IN4} | TEST1, CIT | V _{SS} – 0.3 to V _{SS} + 6.0 | V |
| Input pin voltage 5 | V _{IN5} | PSI, VM, VINI | V _{DD} – 28.0 to V _{DD} + 0.3 | V |
| Output pin voltage 1 | V _{OUT1} | DO | V _{SS} – 0.3 to V _{DD} + 0.3 ≤ V _{SS} + 28.0 | V |
| Output pin voltage 2 | V _{OUT2} | CO | V _{DD} – 28.0 ≤ V _{VM} – 0.3 to V _{DD} + 0.3 | V |
| Operation ambient temperature | T _{opr} | – | –40 to +85 | °C |
| Storage temperature | T _{stg} | – | –55 to +125 | °C |

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ **Thermal Resistance Value**

Table 7

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | |
|--|-----------------|--------------|---------|------|------|------|------|
| Junction-to-ambient thermal resistance*1 | θ _{JA} | 16-Pin TSSOP | Board A | – | 88 | – | °C/W |
| | | | Board B | – | 74 | – | °C/W |
| | | | Board C | – | – | – | °C/W |
| | | | Board D | – | – | – | °C/W |
| | | | Board E | – | – | – | °C/W |

*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ Power Dissipation" and "Test Board" for details.

■ **Electrical Characteristics**

Table 8 (1 / 2)
(V1 = V2 = V3 = V4 = V5 = 3.5 V, Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|-----------------------------|------------------------------|--------------------------|--------------------|--------------------------|------|--------------|
| Detection Voltage | | | | | | | |
| Overcharge detection voltage n | V _{CU_n} | – | V _{CU} – 0.020 | V _{CU} | V _{CU} + 0.020 | V | 1 |
| Overcharge release voltage n | V _{CL_n} | – | V _{CL} – 0.050 | V _{CL} | V _{CL} + 0.050 | V | 1 |
| Overdischarge detection voltage n | V _{DL_n} | – | V _{DL} – 0.050 | V _{DL} | V _{DL} + 0.050 | V | 1 |
| Overdischarge release voltage n | V _{DU_n} | – | V _{DU} – 0.100 | V _{DU} | V _{DU} + 0.100 | V | 1 |
| Discharge overcurrent 1 detection voltage | V _{DIOV1} | – | V _{DIOV1} – 5 | V _{DIOV1} | V _{DIOV1} + 5 | mV | 1 |
| Discharge overcurrent 2 detection voltage | V _{DIOV2} | – | V _{DIOV2} – 10 | V _{DIOV2} | V _{DIOV2} + 10 | mV | 1 |
| Load short-circuiting detection voltage | V _{SHORT} | – | V _{SHORT} – 20 | V _{SHORT} | V _{SHORT} + 20 | mV | 1 |
| Charge overcurrent detection voltage | V _{CIOV} | – | V _{CIOV} – 5 | V _{CIOV} | V _{CIOV} + 5 | mV | 1 |
| Delay Time | | | | | | | |
| CIT pin charge current | I _{CIT} | – | 80 | 120 | 170 | nA | 1 |
| CIT pin detection voltage | V _{CIT} | – | 1.1 | 1.2 | 1.3 | V | 1 |
| Overcharge detection delay time | t _{CU} | – | t _{CU} × 0.7 | t _{CU} | t _{CU} × 1.3 | – | 1 |
| Overdischarge detection delay time | t _{DL} | – | t _{DL} × 0.7 | t _{DL} | t _{DL} × 1.3 | – | 1 |
| Discharge overcurrent 2 detection delay time | t _{DIOV2} | – | t _{DIOV2} × 0.7 | t _{DIOV2} | t _{DIOV2} × 1.3 | – | 1 |
| Load short-circuiting detection delay time | t _{SHORT} | Internally fixed delay time | 100 | 300 | 600 | μs | 1 |
| Charge overcurrent detection delay time | t _{CIOV} | – | t _{CIOV} × 0.7 | t _{CIOV} | t _{CIOV} × 1.3 | – | 1 |
| PSI pin response time | t _{PSI} | – | 1.4 | 2.0 | 2.6 | ms | 1 |
| 0 V Battery Charge | | | | | | | |
| 0 V battery charge starting charger voltage | V _{0CHA} | 0 V battery charge enabled | – | 0.8 | 1.5 | V | 1 |
| 0 V battery charge inhibition battery voltage n | V _{0INH} | 0 V battery charge inhibited | 1.0 | 1.2 | 1.5 | V | 1 |

Remark n = 1, 2, 3, 4, 5

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Table 8 (2 / 2)
(V1 = V2 = V3 = V4 = V5 = 3.5 V, Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|-------------------|---|------|------------------------|------------------|------|--------------|
| Internal Resistance | | | | | | | |
| Resistance between VDD pin and VM pin | R _{VMD} | – | 0.5 | 1 | 1.5 | MΩ | 1 |
| Resistance between VM pin and VSS pin | R _{VMS} | – | 7.5 | 15 | 30 | kΩ | 1 |
| Input Voltage | | | | | | | |
| Operation voltage between VDD pin and VSS pin | V _{DSOP} | Fixed output voltage of DO pin and CO pin | 5.0 | – | 24.0 | V | 1 |
| External control input pin | | | | | | | |
| PSI pin reverse voltage "H" | V _{PSIH} | – | 0.8 | 1.0 | 1.3 | V | 1 |
| PSI pin reverse voltage "L" | V _{PSIL} | – | 0.5 | 0.8 | 1.0 | V | 1 |
| Input Current | | | | | | | |
| Current consumption during operation | I _{OP} | – | – | 4 | 8 | μA | 1 |
| Current consumption during power-down | I _{PDN} | – | – | – | 0.1 | μA | 1 |
| Current consumption during power-saving | I _{PSV} | – | – | – | 0.1 | μA | 1 |
| VC1 pin current | I _{VC1} | – | – | 0.25 | 0.4 | μA | 1 |
| VC2 pin current | I _{VC2} | – | –0.4 | 0.05 | 0.4 | μA | 1 |
| VC3 pin current | I _{VC3} | – | –0.4 | –0.1 | 0.4 | μA | 1 |
| VC4 pin current | I _{VC4} | – | –0.4 | –0.1 | 0.4 | μA | 1 |
| VC5 pin current | I _{VC5} | – | –0.4 | –0.1 | 0.4 | μA | 1 |
| PSI pin current "H" | I _{PSIH} | – | –400 | –200 | –100 | nA | 1 |
| PSI pin current "L" | I _{PSIL} | – | 100 | 200 | 400 | nA | 1 |
| Output pin | | | | | | | |
| CO pin voltage "H" | V _{COH} | 4-serial cell | – | – | V _{DD} | V | 1 |
| | | 5-serial cell | – | V _{VC2} – 0.5 | V _{VC2} | V | 1 |
| DO pin voltage "H" | V _{DOH} | 4-serial cell | – | – | V _{DD} | V | 1 |
| | | 5-serial cell | – | V _{VC2} – 0.5 | V _{VC2} | V | 1 |
| CO pin source current | I _{COH} | – | 10 | – | – | μA | 1 |
| CO pin sink current | I _{COL} | – | 180 | 200 | – | μA | 1 |
| DO pin source current | I _{DOH} | – | 10 | – | – | μA | 1 |
| DO pin sink current | I _{DOL} | – | 1700 | 2000 | – | μA | 1 |

■ **Test Circuits**

Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) and DO pin (V_{DO}) are judged as follows.

L: $[V_{CO}, V_{DO}] \leq V_{DS} \times 0.1 \text{ V}$

H: $[V_{CO}, V_{DO}] > V_{DS} \times 0.1 \text{ V}$

Remark V_{DS} : Input voltage between VDD pin and VSS pin ($V1 + V2 + V3 + V4 + V5$)

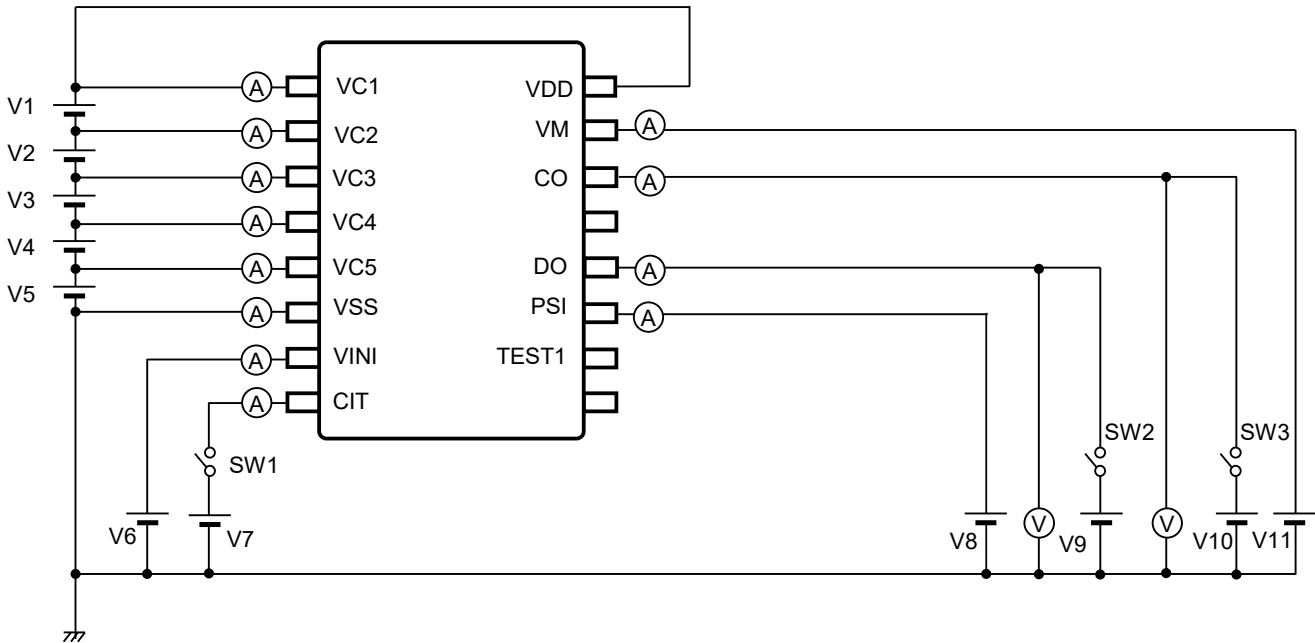


Figure 4 Test circuit 1

This section provides explanations of Test items using Test circuit 1. Perform each test after setting as shown in **Table 9**.

Table 9 Initial Setting of Test Circuit 1 (1 / 2)

| Symbol | V1 | V2 | V3 | V4 | V5 | V6 | V7 | V8 | V9 | V10 | V11 | SW1 | SW2 | SW3 |
|---------|-------|-------|-------|-------|-------|-----|-----|----------|----|-----|-----|-----|-----|-----|
| Setting | 3.5 V | 3.5 V | 3.5 V | 3.5 V | 3.5 V | 0 V | 0 V | V_{DS} | - | - | 0 V | ON | OFF | OFF |

1. Overcharge detection voltage n (V_{CU_n}), overcharge release voltage n (V_{CL_n})

Overcharge detection voltage 1 (V_{CU1}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased after setting $V1 = V2 = V3 = V4 = V5 = V_{CU_n} - 0.05 \text{ V}$. Overcharge release voltage 1 (V_{CL1}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when the voltage V1 is then gradually decreased after setting $V2 = V3 = V4 = V5 = V_{CL_n} - 0.05 \text{ V}$, $V11 = 0.2 \text{ V}$.

Overcharge detection voltage n (V_{CU_n}) and overcharge release voltage n (V_{CL_n}) (n = 2 to 5) can be determined in the same way as when n = 1.

2. Overdischarge detection voltage n (V_{DL_n}), overdischarge release voltage n (V_{DU_n})

Overdischarge detection voltage 1 (V_{DL1}) is defined as the voltage V1 at which V_{DO} goes from "H" to "L" when the voltage V1 is gradually decreased. Overdischarge release voltage 1 (V_{DU1}) is defined as the voltage V1 at which V_{DO} goes from "L" to "H" when the voltage V1 is then gradually increased after setting $V11 = 0.2 \text{ V}$. Overdischarge detection voltage n (V_{DL_n}) and overdischarge release voltage n (V_{DU_n}) (n = 2 to 5) can be determined in the same way as when n = 1.

3. Discharge overcurrent 1 detection voltage (V_{DIOV1})

Discharge overcurrent 1 detection voltage (V_{DIOV1}) is defined as the voltage V6 at which CIT pin current changes from the direction of flowing into the IC to the direction of flowing out from the IC when the voltage V6 is gradually increased after setting V7 = 0.01 V.

4. Discharge overcurrent 2 detection voltage (V_{DIOV2})

Discharge overcurrent 2 detection voltage (V_{DIOV2}) is defined as the voltage V6 at which V_{DO} goes from "H" to "L" when the voltage V6 is gradually increased after setting V11 = 0.5 V.

5. Load short-circuiting detection voltage (V_{SHORT})

Load short-circuiting detection voltage (V_{SHORT}) is defined as the voltage V6 at which delay time from when V6 is increased after setting V11 = 0.5 V to when V_{DO} goes from "H" to "L" is load short-circuiting detection delay time (t_{SHORT}).

6. Charge overcurrent detection voltage (V_{CIOV})

Charge overcurrent detection voltage (V_{CIOV}) is defined as the voltage V6 at which V_{CO} goes from "H" to "L" when the voltage V6 is gradually decreased after setting V11 = -0.1 V.

7. CIT pin charge current (I_{CIT}), CIT pin detection voltage (V_{CIT})

CIT pin charge current (I_{CIT}) is defined as the CIT pin current when setting $V6 = (V_{DIOV1} + V_{DIOV2}) / 2$.

CIT pin detection voltage (V_{CIT}) is defined as the voltage V7 at which V_{DO} goes from "H" to "L" when the voltage V7 is then gradually increased.

8. Overcharge detection delay time (t_{CU})

Overcharge detection delay time (t_{CU}) is the time period from when the voltage V1 exceeds V_{CU1} after setting V1 = V2 = V3 = V4 = V5 = 3.5 V till when V_{CO} goes from "H" to "L".

9. Overdischarge detection delay time (t_{DL})

Overdischarge detection delay time (t_{DL}) is the time period from when the voltage V1 falls below V_{DL1} after setting V1 = V2 = V3 = V4 = V5 = 3.5 V till when V_{DO} goes from "H" to "L".

10. Discharge overcurrent 2 detection delay time (t_{DIOV2})

Discharge overcurrent 2 detection delay time (t_{DIOV2}) is the time period from when the voltage V6 exceeds V_{DIOV2} after setting V11 = 0.5 V till when V_{DO} changes from "H" to "L".

11. Load short-circuiting detection delay time (t_{SHORT})

Load short-circuiting detection delay time (t_{SHORT}) is the time period from when the voltage V6 exceeds V_{SHORT} after setting V11 = 0.5 V till when V_{DO} changes from "H" to "L".

12. Charge overcurrent detection delay time (t_{CIOV})

Charge overcurrent detection delay time (t_{CIOV}) is the time period from when the voltage V6 falls below V_{CIOV} after setting V11 = -0.1 V till when V_{CO} changes from "H" to "L".

13. PSI pin response time (t_{PSI})

PSI pin response time (t_{PSI}) is the time period from when the voltage V8 is changed to 0 V till when V_{DO} changes from "H" to "L".

14. 0 V battery charge starting charger voltage (V_{0CHA}) (0 V battery charge enabled)

This IC reaches the overdischarge status after setting $V1 = V_{DL1} - 0.1$ V. Then set $V1 = V2 = V3 = V4 = V5 = 0$ V. 0 V battery charge starting charger voltage (V_{0CHA}) is defined as the absolute value of voltage V11 at which I_{CO} exceeds 1.0 μ A when the voltage V11 is then gradually decreased after setting SW3 ON and $V10 = V11 = -0.5$ V.

15. 0 V battery charge inhibition battery voltage n (V_{0INHn}) (0 V battery charge inhibited)

0 V battery charge inhibition battery voltage 1 (V_{0INH1}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually decreased after setting $V1 = V2 = V3 = V4 = V5 = V_{DLn} - 0.1$ V.

0 V battery charge inhibition battery voltage n (V_{0INHn}) (n = 2 to 5) can be determined in the same way as when n = 1.

16. Resistance between VM pin and VDD pin (R_{VMD})

Resistance between VM pin and VDD pin (R_{VMD}) is defined by $R_{VMD} = (V_{DS} + 0.1) / I_{VM}$ using I_{VM} when setting $V1 = V2 = V3 = V4 = V5 = 1.5$ V and $V11 = -0.1$ V.

17. Resistance between VM pin and VSS pin (R_{VMS})

Resistance between VM pin and VSS pin (R_{VMS}) is defined by $R_{VMS} = V11 / I_{VM}$ using I_{VM} when setting $V6 = 1.0$ V and $V11 = 2.0$ V.

18. PSI pin reverse voltage "H" (V_{PSIH})

PSI pin reverse voltage "H" (V_{PSIH}) is defined as the voltage V8 at which V_{DO} goes from "L" to "H" when the voltage V8 is gradually increased after setting $V8 = 0$ V.

19. PSI pin reverse voltage "L" (V_{PSIL})

PSI pin reverse voltage "L" (V_{PSIL}) is defined as the voltage V8 at which V_{DO} goes from "H" to "L" when the voltage V8 is gradually decreased.

20. Current consumption during operation (I_{OPE})

Current consumption during operation (I_{OPE}) is defined as the sum of VSS pin current, VM pin current and VINI pin current after setting SW1 OFF.

21. Current consumption during power-down (I_{PDN})

Current consumption during power-down (I_{PDN}) is defined as I_{VSS} under the setting conditions of $V1 = V2 = V3 = V4 = V5 = 1.5$ V and $V11 = V_{DS}$.

22. Current consumption during power-saving (I_{PSV})

Current consumption during power-saving (I_{PSV}) is defined as I_{VSS} under the setting conditions of $V8 = 0$ V and $V11 = V_{DS}$.

23. PSI pin current "H" (I_{PSIH}), PSI pin current "L" (I_{PSIL})

PSI pin current "H" (I_{PSIH}) is defined as I_{PSI} when setting $V8 = V_{DS} - 1$ V after setting $V8 = V_{DS}$.

PSI pin current "L" (I_{PSIL}) is defined as I_{PSI} when setting $V8 = (V_{PSIH} + V_{PSIL}) / 2$ after setting $V8 = 0$ V.

24. CO pin voltage "H" (V_{COH}), CO pin source current (I_{COH})

CO pin voltage "H" (V_{COH}) is defined as CO pin voltage (V_{CO}) in the settings shown in **Table 9**. CO pin source current (I_{COH}) is defined as I_{CO} when setting $V10 = V_{COH} - 0.5$ V and SW3 ON.

25. CO pin sink current (I_{COL})

CO pin sink current (I_{COL}) is defined as I_{CO} when setting $V1 = V_{CU1} + 0.1$ V, $V10 = 0.5$ V and SW3 ON.

26. DO pin voltage "H" (V_{DOH}), DO pin source current (I_{DOH})

DO pin voltage "H" (V_{DOH}) is defined as DO pin voltage (V_{DO}) in the settings shown in **Table 9**. DO pin source current (I_{DOH}) is defined as I_{DO} when setting $V9 = V_{DOH} - 0.5$ V and SW2 ON.

27. DO pin sink current (I_{DOL})

DO pin sink current (I_{DOL}) is defined as I_{DO} when setting $V1 = V_{DL1} - 0.1$ V, $V9 = 0.5$ V and SW2 ON.

■ Operation

Remark Refer to "■ Battery Protection IC Connection Example".

1. Normal status

The status when the CO pin output voltage (V_{CO}) = "H" and DO pin output voltage (V_{DO}) = "H" is the normal status. CO pin voltage "H" (V_{COH}) is the voltage V_{CO} when the V_{CO} is "H". DO pin voltage "H" (V_{DOH}) is the voltage V_{DO} when the V_{DO} is "H".

All the conditions mentioned below should be satisfied for returning to the normal status.

- The voltage of each of the batteries is in the range from the overcharge detection voltage n (V_{CU_n}) to overdischarge detection voltage n (V_{DL_n}).
- The VINI pin voltage is in the range of the charge overcurrent detection voltage (V_{CIOV}) to discharge overcurrent 1 detection voltage (V_{DIOV1}).
- The PSI pin voltage is higher than the PSI pin reverse voltage "H" (V_{PSIH}).

Caution After a battery is connected, there may be cases when discharging cannot be performed. In this case, this IC returns to the normal status when any of the following conditions is satisfied.

- (1) Connecting a charger
- (2) Shorting between the VM pin and the VSS pin
- (3) Changing the PSI pin voltage to be $V_{DS} \rightarrow 0\text{ V} \rightarrow V_{DS}$

2. Overcharge status

When the voltage of any of the batteries exceeds the overcharge detection voltage n (V_{CU_n}) and the status continues for the overcharge detection delay time (t_{CU})*1 or longer, the CO pin changes to VM pin voltage. This is the overcharge status. In this case, the charge control FET is turned off and charging is stopped.

The overcharge status is released if either condition mentioned below is satisfied.

- (1) $V_{VM} < 0.3\text{ V}$ typ., and voltage of all batteries $\leq V_{CL_n}$
- (2) $V_{VM} \geq 0.3\text{ V}$ typ., and voltage of all batteries $\leq V_{CU_n}$

*1. Refer to "6. Delay time setting" for details.

Remark V_{VM} : VM pin voltage
 V_{CU_n} : Overcharge detection voltage n (n = 1, 2, 3, 4, 5)
 V_{CL_n} : Overcharge release voltage n (n = 1, 2, 3, 4, 5)

3. Overdischarge status

When the voltage of any of the batteries decreases to the overdischarge detection voltage n (V_{DLn}) or lower and the status continues for the overdischarge detection delay time (t_{DL})*¹ or longer, the DO pin changes to the V_{SS} level. This is the overdischarge status. The discharge control FET is turned off and discharging is stopped.

The overdischarge status is released if either condition mentioned below is satisfied.

- (1) $V_{VM} \leq 0$ V typ., and voltage of all batteries $\geq V_{DLn}$
- (2) $V_{VM} > 0$ V typ., and voltage of all battery $\geq V_{DU n}$

*1. Refer to "6. Delay time setting" for details.

Remark V_{VM} : VM pin voltage
 V_{DLn} : Overdischarge detection voltage n ($n = 1, 2, 3, 4, 5$)
 $V_{DU n}$: Overdischarge release voltage n ($n = 1, 2, 3, 4, 5$)

3.1 With power-down function

When this IC reaches the overdischarge status, the VM pin is pulled up to the V_{DD} level by a resistance between VM pin and VDD pin (R_{VMD}). If the VM pin voltage changes to 0.7 V typ. or higher, the power-down function starts to operate and most operations in this IC halt. The CO pin changes to VM pin voltage. In this case, the charge control FET is turned off and charging is stopped.

By connecting a battery charger, the power-down function is released when the VM pin voltage is 0.7 V typ. or lower.

4. Discharge overcurrent status

When the discharge current increases to a certain value or more, the VINI pin voltage increases to the level of discharge overcurrent 1 detection voltage (V_{DIOV1}) or higher. If the condition continues for the discharge overcurrent 1 detection delay time (t_{DIOV1})*¹ or longer, the DO pin changes to the V_{SS} level. This is the discharge overcurrent status. The discharge control FET is turned off and discharging is stopped.

Discharge overcurrent is detected at the following three levels: V_{DIOV1} , V_{DIOV2} , and V_{SHORT} . When discharge overcurrent 2 detection voltage (V_{DIOV2}) and load short-circuiting detection voltage (V_{SHORT}) are detected, the same operations as V_{DIOV1} detection are performed.

4.1 Release condition of discharge overcurrent status "Load disconnection"

Under the discharge overcurrent status, VM pin and VSS pin are shorted by R_{VMS} in this IC. However, the VM pin voltage is the V_{DD} level due to the load as long as the load is connected. When the load is disconnected, the VM pin voltage returns to the V_{SS} level. When the VM pin voltage returns to $V_{DS} / 3$ or lower, this IC releases the discharge overcurrent status.

R_{VMD} is not connected in the discharge overcurrent status.

4.2 Release condition of discharge overcurrent status "Charger connection"

Under the discharge overcurrent status, VDD pin and VM pin are shorted by R_{VMD} in this IC. When a battery is connected to a charger and VM pin voltage returns to V_{DIOV1} or lower, this IC releases the discharge overcurrent status.

R_{VMS} is not connected in the discharge overcurrent status.

5. Charge overcurrent status

When the charge current increases to a certain value or more, the VINI pin voltage decreases to the level of charge overcurrent detection voltage (V_{CIOV}) or lower. If the status continues for the charge overcurrent detection delay time (t_{CIOV})*1 or longer, the CO pin voltage changes to the VM pin voltage. This is the charge overcurrent status. In this case, the charge control FET is turned off and charging is stopped. The VM pin is pulled up to the V_{DD} level by a resistance between VM pin and V_{DD} pin (R_{VMD}).

The charge overcurrent status is released if the VM pin voltage increases 0.3 V typ. or higher.

*1. Refer to "6. Delay time setting" for details.

6. Delay time setting

Users are able to set delay time for the period from when this IC detects change in the voltage of any of the batteries or the VINI pin until when it outputs to the CO pin or DO pin. The discharge overcurrent 1 detection delay time (t_{DIOV1}) is determined by constant current in this IC and an external capacitor. The other detection delay times are fixed internally.

6.1 Other than discharge overcurrent 1 detection delay time (t_{DIOV1})

The detection delay times are determined by dividing a clock of approximately 4 kHz by the counter.

Remark t_{DIOV2} and t_{SHORT} start when V_{DIOV2} is detected. When V_{SHORT} is detected over t_{SHORT} after the detection of V_{DIOV2} , this IC turns the discharge control FET off within t_{DIOV2} or t_{SHORT} of each detection.

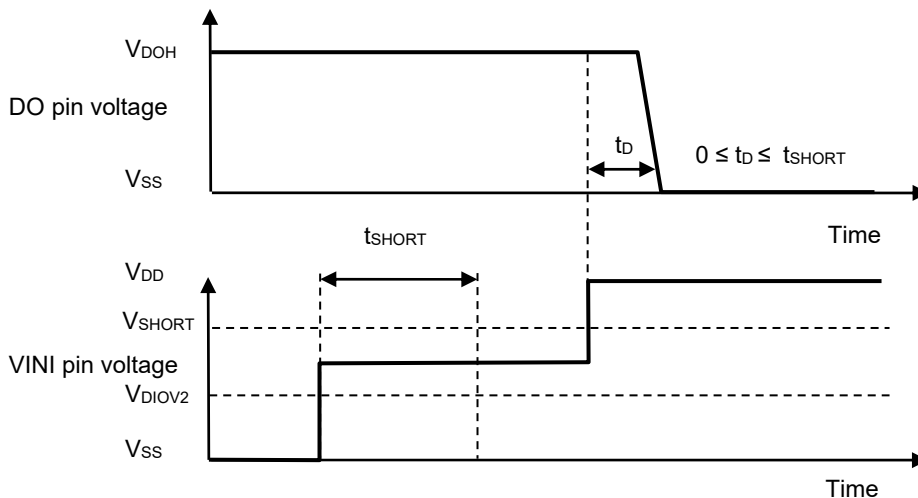


Figure 5

6.2 Discharge overcurrent 1 detection delay time (t_{DIOV1})

In the discharge overcurrent 1 detection, when the VINI pin voltage increases to discharge overcurrent 1 detection voltage (V_{DIOV1}) or higher, the internal circuit of this IC starts charging to an external capacitor connected to the CIT pin via the CIT pin current (I_{CIT}) = 120 nA typ. When the CIT pin voltage increases to the CIT pin detection voltage (V_{CIT}) or higher, the DO pin voltage changes to V_{SS} level. This period is discharge overcurrent 1 detection delay time (t_{DIOV1}).

t_{DIOV1} is calculated by the following formula.

$$t_{DIOV1} [s] = C_{CIT} [F] \times V_{CIT} [V] / I_{CIT} [A]$$

If $C_{CIT} = 0.01 \mu F$, t_{DIOV1} is calculated as follows:

$$t_{DIOV1} [s] = 0.01 \mu F \times 1.2 V \text{ typ.} / 120 nA \text{ typ.} = 100 ms \text{ typ.}$$

7. 0 V Battery charge function

Regarding how to charge a self-discharged battery (0 V battery), users are able to select either function mentioned below.

- (1) 0 V battery charge enabled
A 0 V battery is charged when charger voltage is higher than the 0 V battery charge starting charger voltage (V_{0CHA}).
- (2) 0 V battery charge inhibited
A 0 V battery is not charged when the voltage of any of the batteries is the 0 V battery charge inhibition battery voltage n (V_{0INHn}) or lower.

Caution When the VDD pin voltage is lower than the minimum value of operation voltage between the VDD pin and VSS pin (V_{DSOP}), this IC's operation is not assured.

Remark $n = 1, 2, 3, 4, 5$

8. PSI pin

When the PSI pin is activated, the power-saving function starts to operate, and most operations halt. In this case, the CO pin changes to the VM pin level, and DO pin changes to the VSS level.

Table 10 Status Set by PSI Pin

| PSI pin | CO pin | DO pin |
|--|----------------------|----------------------|
| $V_{PSIH} \leq \text{PSI pin voltage} \leq V_{DD}$ level | "H" | "H" |
| $V_{PSIL} < \text{PSI pin voltage} < V_{PSIH}$ | Maintains the status | Maintains the status |
| V_{SS} level \leq PSI pin voltage $\leq V_{PSIL}$ | VM pin level | VSS level |

This IC is initialized and becomes the normal status by deactivating the PSI pin after activating PSI pin and enabling the power-saving function. As a result, each detection operation is carried out after returning to the normal status.

■ **Timing Charts**

1. **Overcharge detection, overdischarge detection**

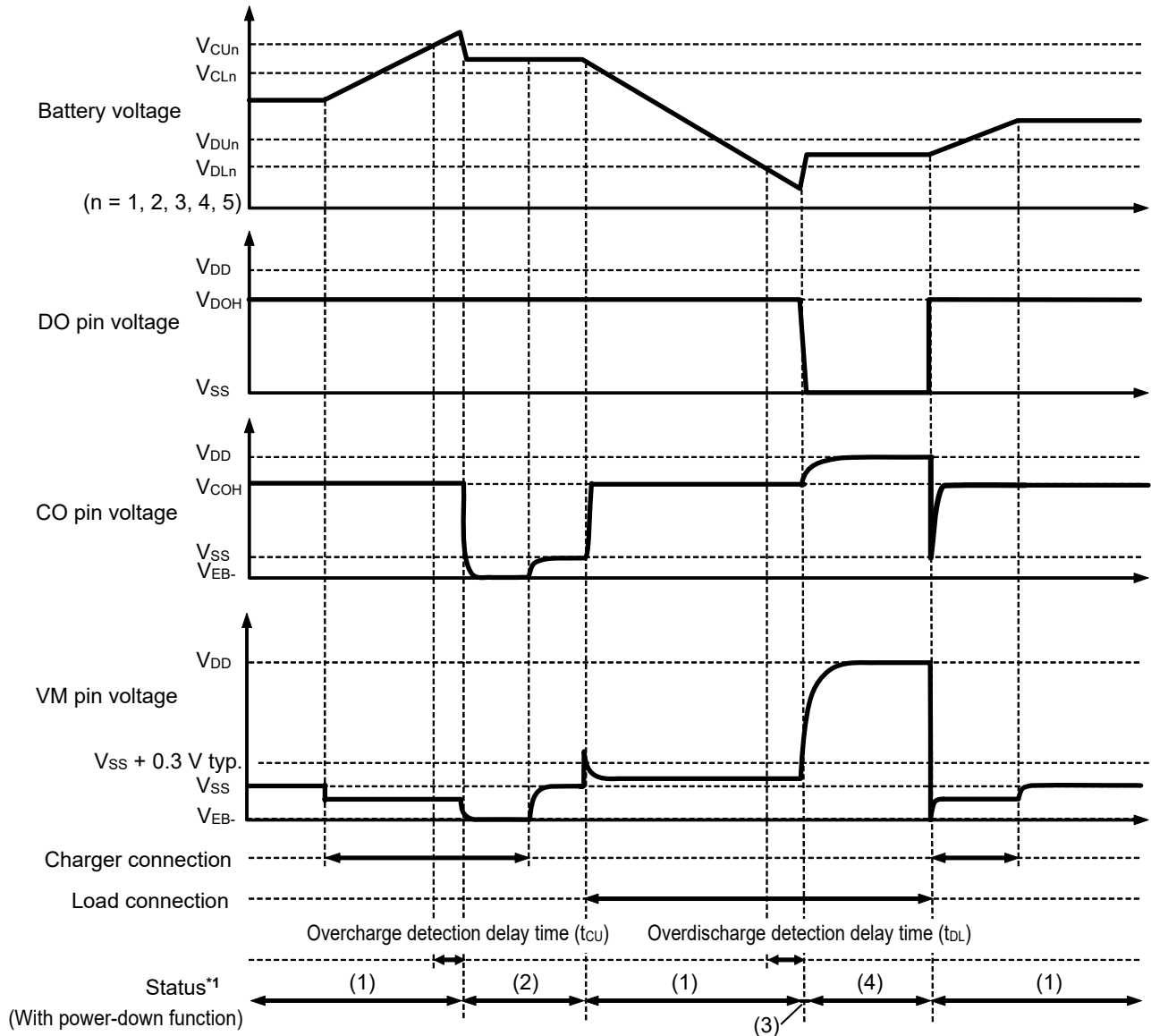


Figure 6

- *1. (1) : Normal status
 (2) : Overcharge status
 (3) : Overdischarge status
 (4) : Power-down status

2. Discharge overcurrent detection

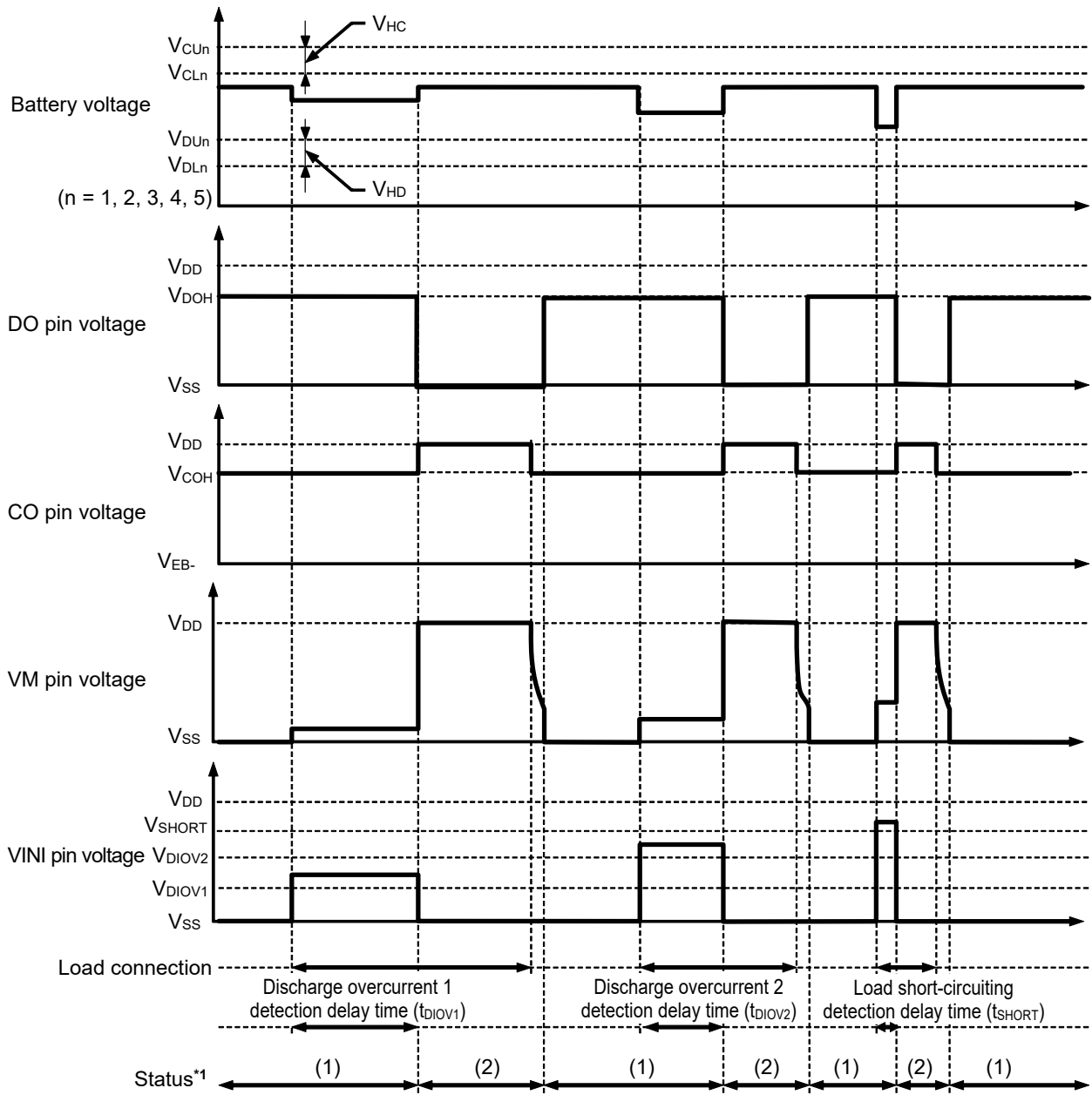


Figure 7

*1. (1) : Normal status
(2) : Discharge overcurrent status

3. Charge overcurrent detection

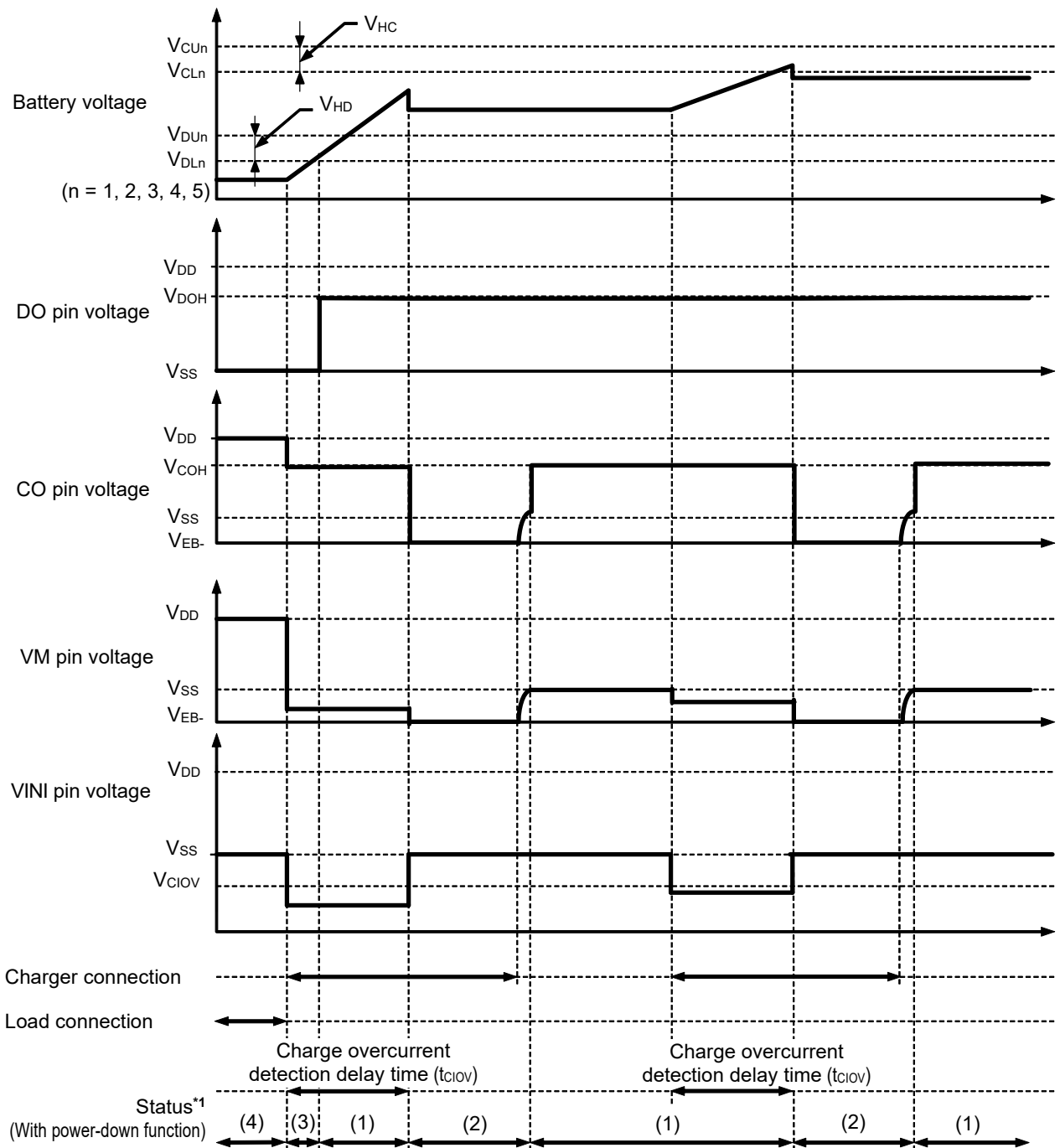


Figure 8

- *1. (1) : Normal status
 (2) : Charge overcurrent status
 (3) : Overdischarge status
 (4) : Power-down status

■ **Connection Examples of Battery Protection IC**

1. S-82B4A Series (4-serial cell)

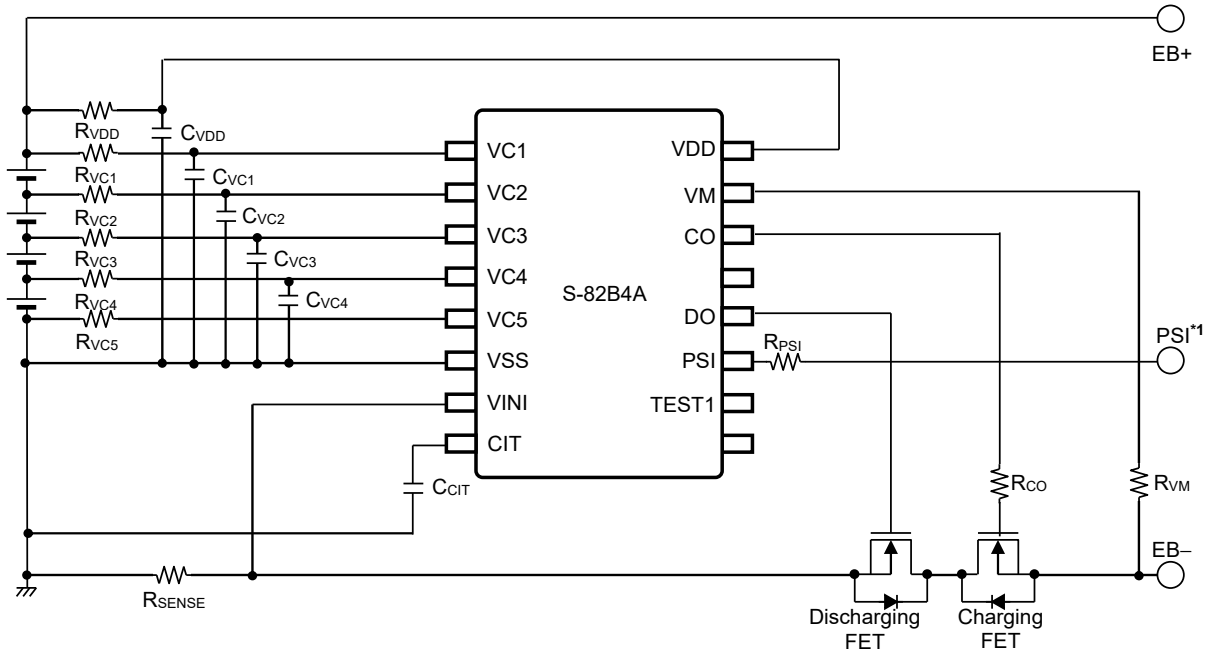


Figure 9

*1. If you do not use the power-saving function, connect the PSI pin to the VDD pin.

Remark Regarding the recommended values for external components, refer to "Table 11 Constants for External Components".

2. S-82B5A Series (5-serial cell)

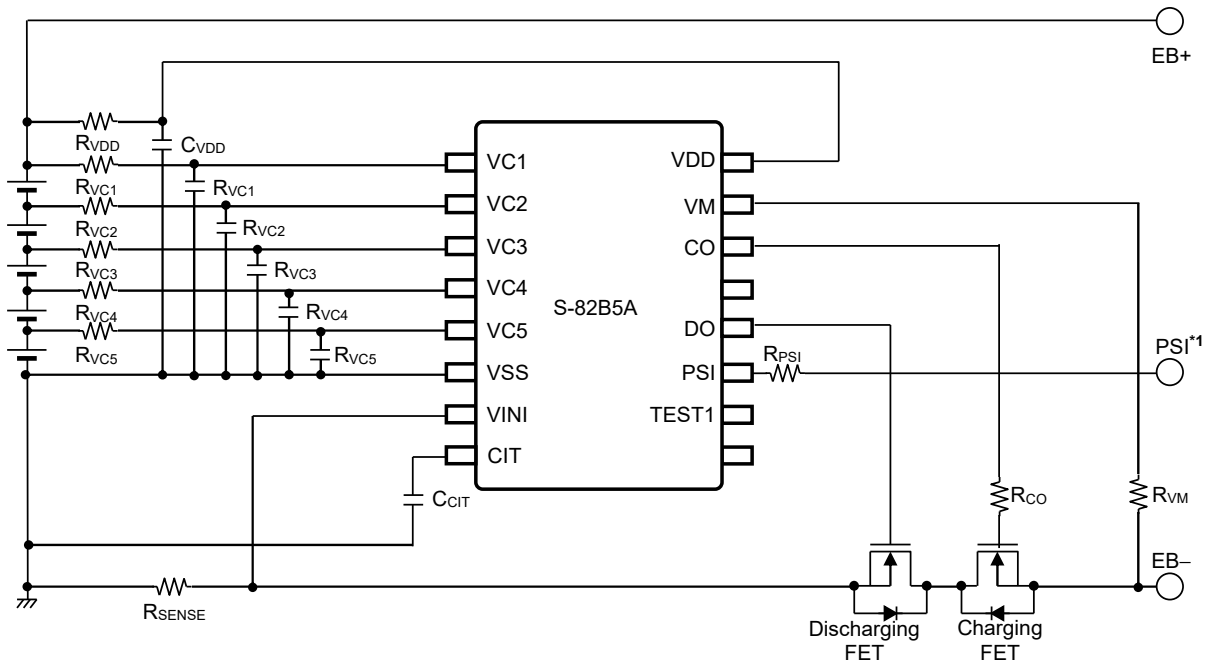


Figure 10

*1. If you do not use the power-saving function, connect the PSI pin to the VDD pin.

Remark Regarding the recommended values for external components, refer to "Table 11 Constants for External Components".

Table 11 Constants for External Components

| Symbol | Typ. | Unit |
|--------------------------------------|--------------|------|
| R _{VDD} | 100 | Ω |
| R _{VCn} (n = 1, 2, 3, 4, 5) | 1 | kΩ |
| R _{PSI} | 1 | kΩ |
| R _{CO} | 1 | kΩ |
| R _{VM} | 1 | kΩ |
| R _{SENSE} | – | mΩ |
| C _{VDD} | 1 | μF |
| C _{VCn} (n = 1, 2, 3, 4, 5) | 0.1 | μF |
| C _{CIT} | 0.01 or more | μF |

- Caution 1.** The constants may be changed without notice.
- 2.** Sufficient evaluation of transient power supply fluctuation and overcurrent protection function with the actual application is needed to determine the proper constants when setting the filter constants between the VDD pin and VSS pin. Contact our sales representatives if setting the constants between the VDD pin and VSS pin to anything other than the recommended values.
 - 3.** It has not been confirmed whether the operation is normal or not in circuits other than the connection examples. In addition, the connection examples and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.

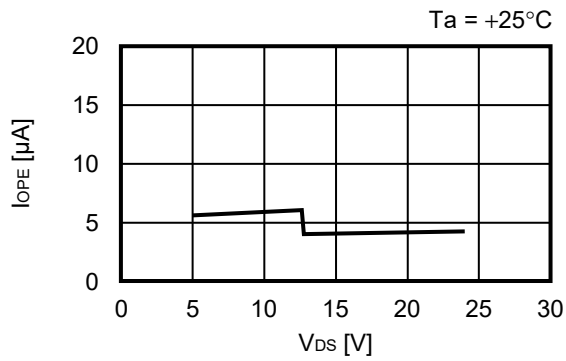
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Batteries can be connected in any order; however, there may be cases when discharging cannot be performed after a battery is connected. In this case, this IC returns to the normal status when any of the following conditions is satisfied.
 - (1) Connecting a charger
 - (2) Shorting between the VM pin and the VSS pin
 - (3) Changing the PSI pin voltage to be $V_{DS} \rightarrow 0\text{ V} \rightarrow V_{DS}$
- If an overcharged battery and an overdischarged battery intermix, this IC will change to the overcharge and overdischarge statuses. Therefore, in this case, both charging and discharging are impossible.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

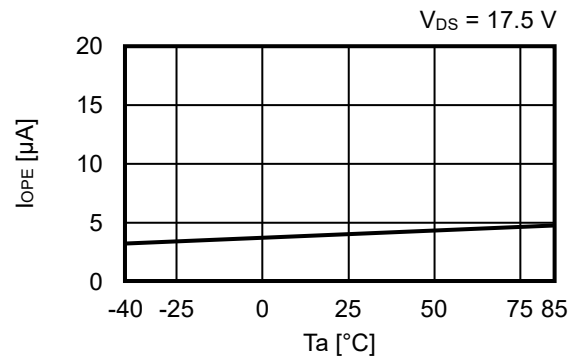
■ **Characteristics (Typical Data)**

1. Current consumption

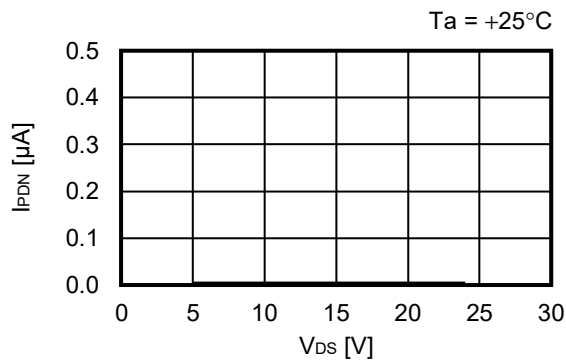
1.1 I_{OPe} vs. V_{Ds}



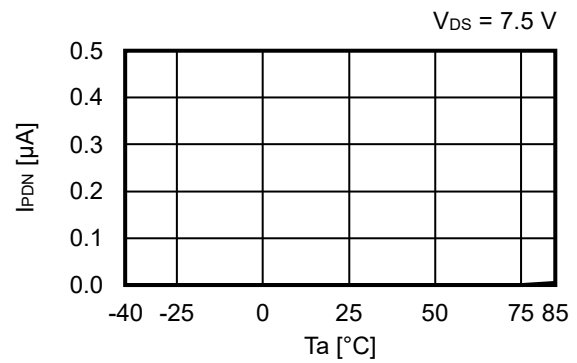
1.2 I_{OPe} vs. Ta



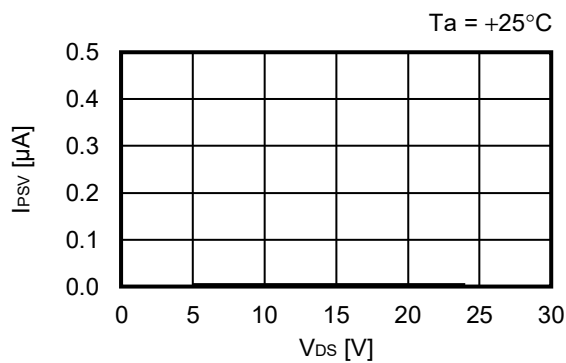
1.3 I_{PDN} vs. V_{Ds}



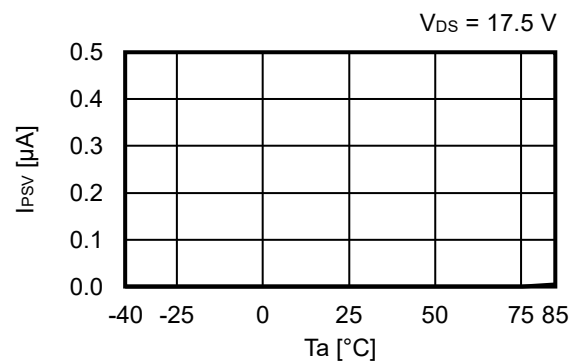
1.4 I_{PDN} vs. Ta



1.5 I_{PSV} vs. V_{Ds}

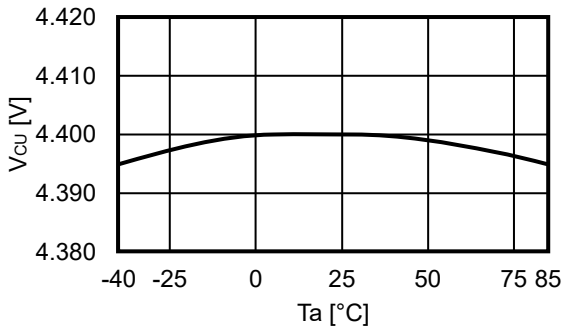


1.6 I_{PSV} vs. Ta

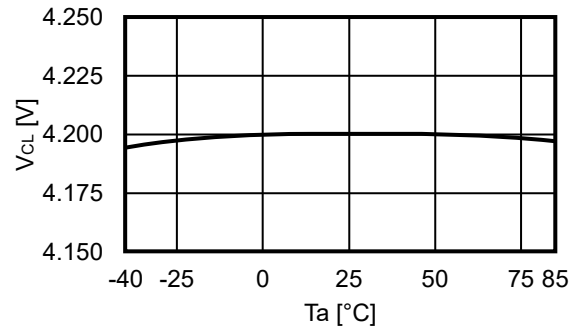


2. Detection voltage, release voltage

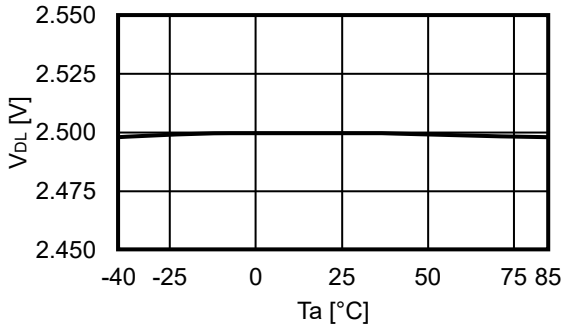
2.1 V_{CU} vs. T_a



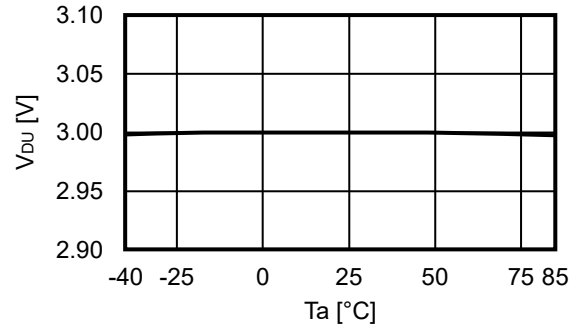
2.2 V_{CL} vs. T_a



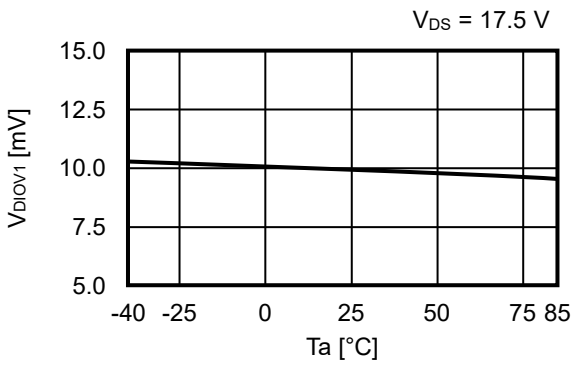
2.3 V_{DL} vs. T_a



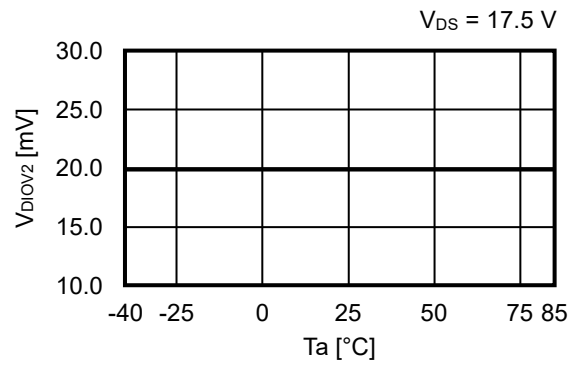
2.4 V_{DU} vs. T_a



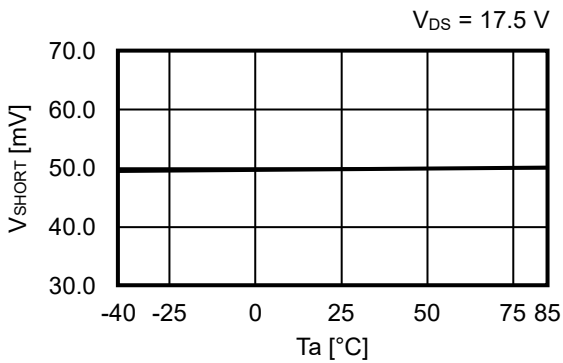
2.5 V_{DIOV1} vs. T_a



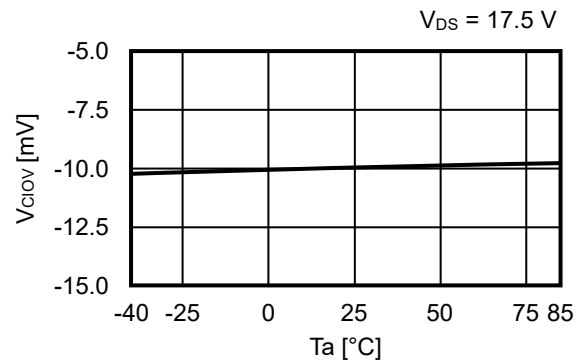
2.6 V_{DIOV2} vs. T_a



2.7 V_{SHORT} vs. T_a

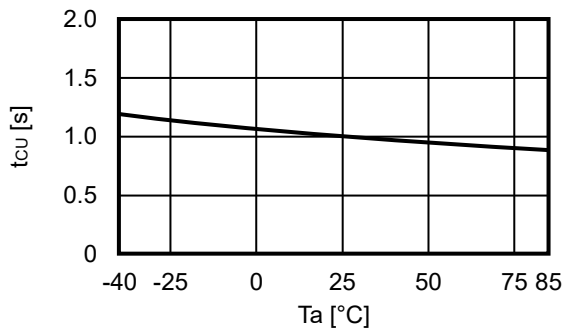


2.8 V_{CIOV} vs. T_a

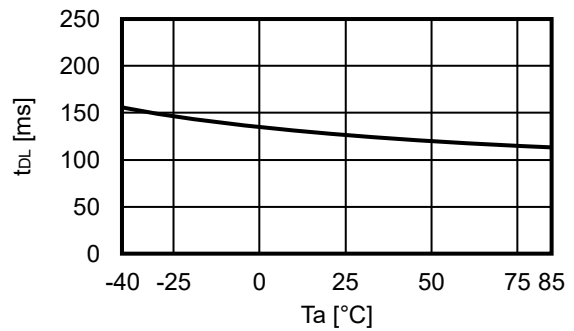


3. Delay time function

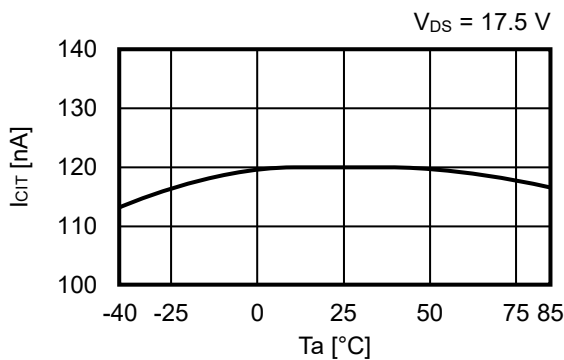
3.1 t_{CU} vs. T_a



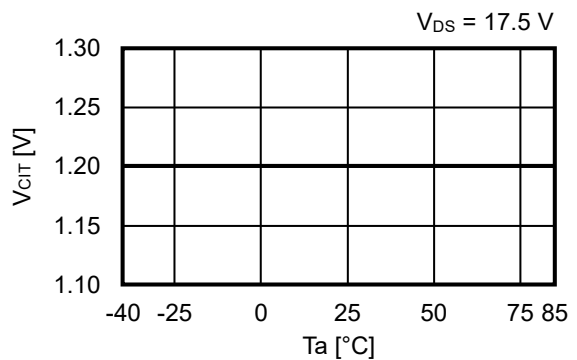
3.2 t_{DL} vs. T_a



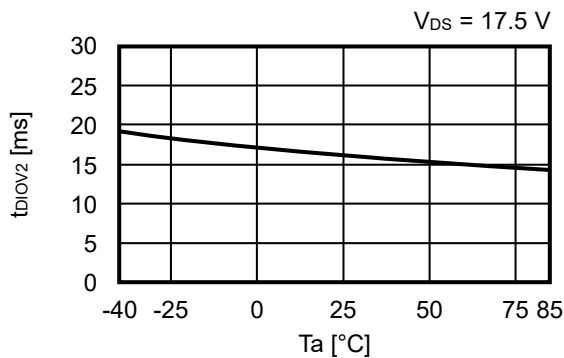
3.3 I_{CIT} vs. T_a



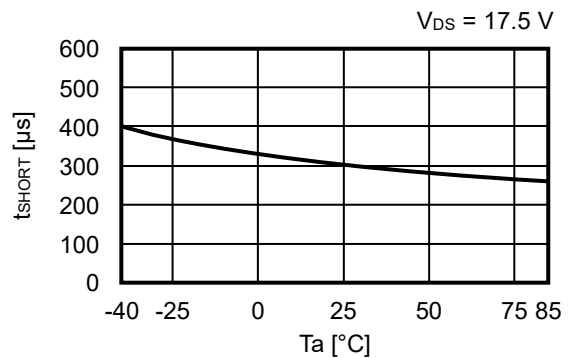
3.4 V_{CIT} vs. T_a



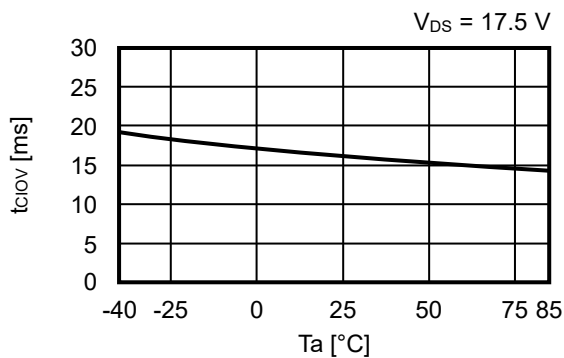
3.5 t_{DIOV2} vs. T_a



3.6 t_{SHORT} vs. T_a

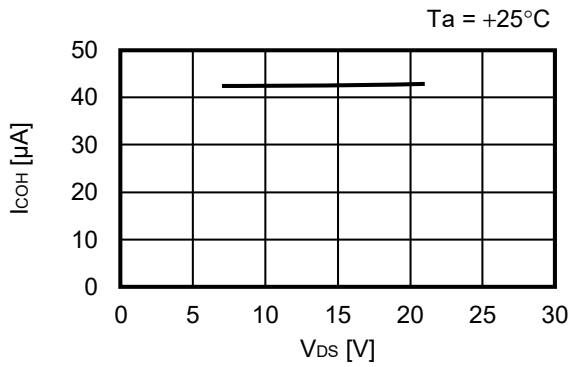


3.7 t_{CIOV} vs. T_a

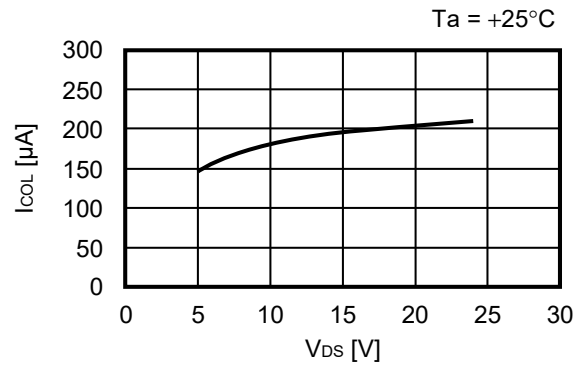


4. Output pin

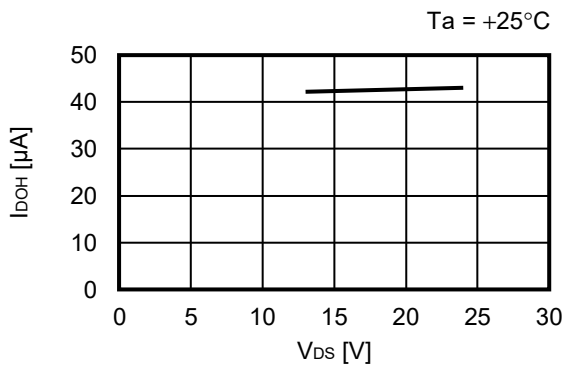
4.1 I_{COH} vs. V_{DS}



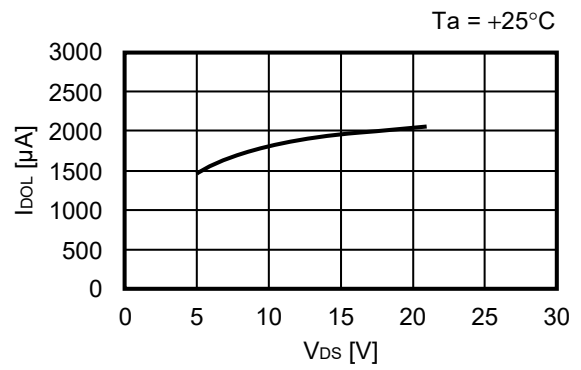
4.2 I_{COL} vs. V_{DS}



4.3 I_{DOH} vs. V_{DS}

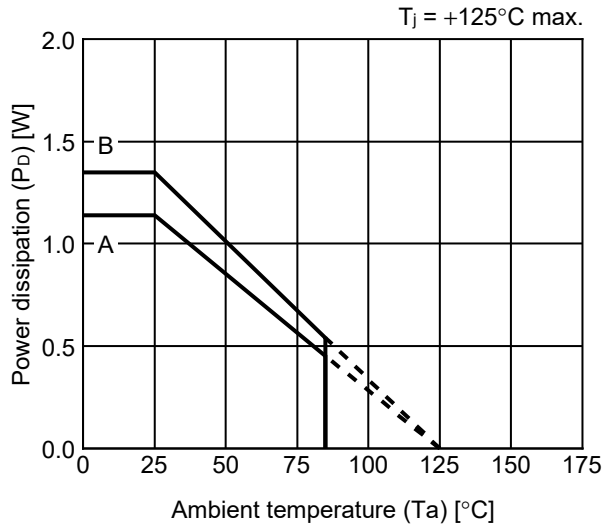


4.4 I_{DOL} vs. V_{DS}



■ **Power Dissipation**


16-Pin TSSOP

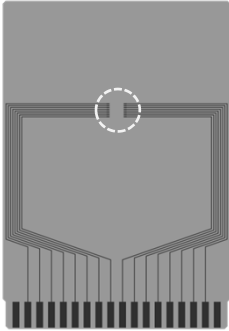


| Board | Power Dissipation (P_D) |
|-------|-----------------------------|
| A | 1.14 W |
| B | 1.35 W |
| C | – |
| D | – |
| E | – |

16-Pin TSSOP Test Board

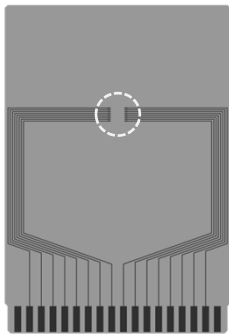
(1) Board A

 IC Mount Area



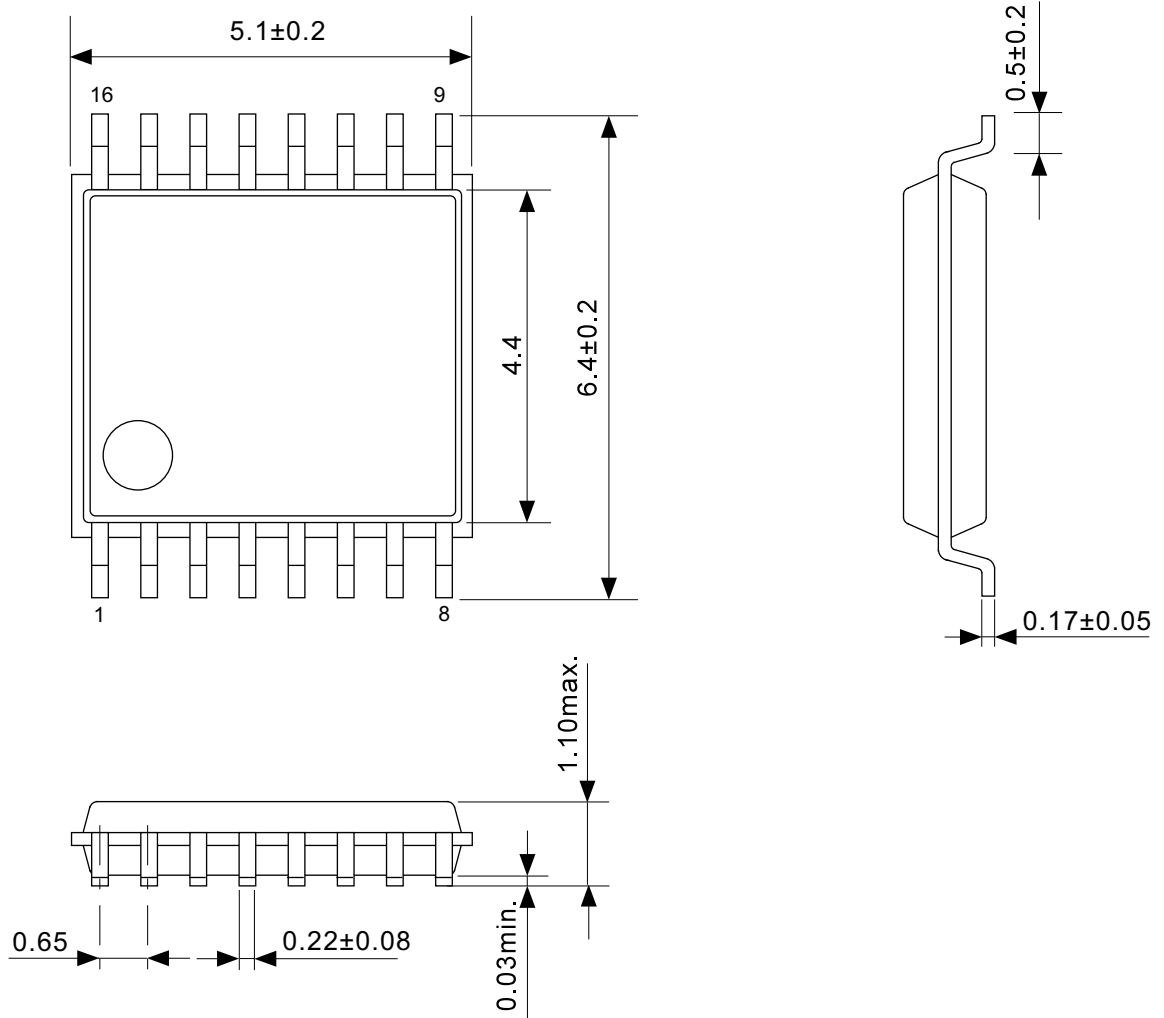
| Item | | Specification |
|-----------------------------|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 2 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | - |
| | 3 | - |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

(2) Board B



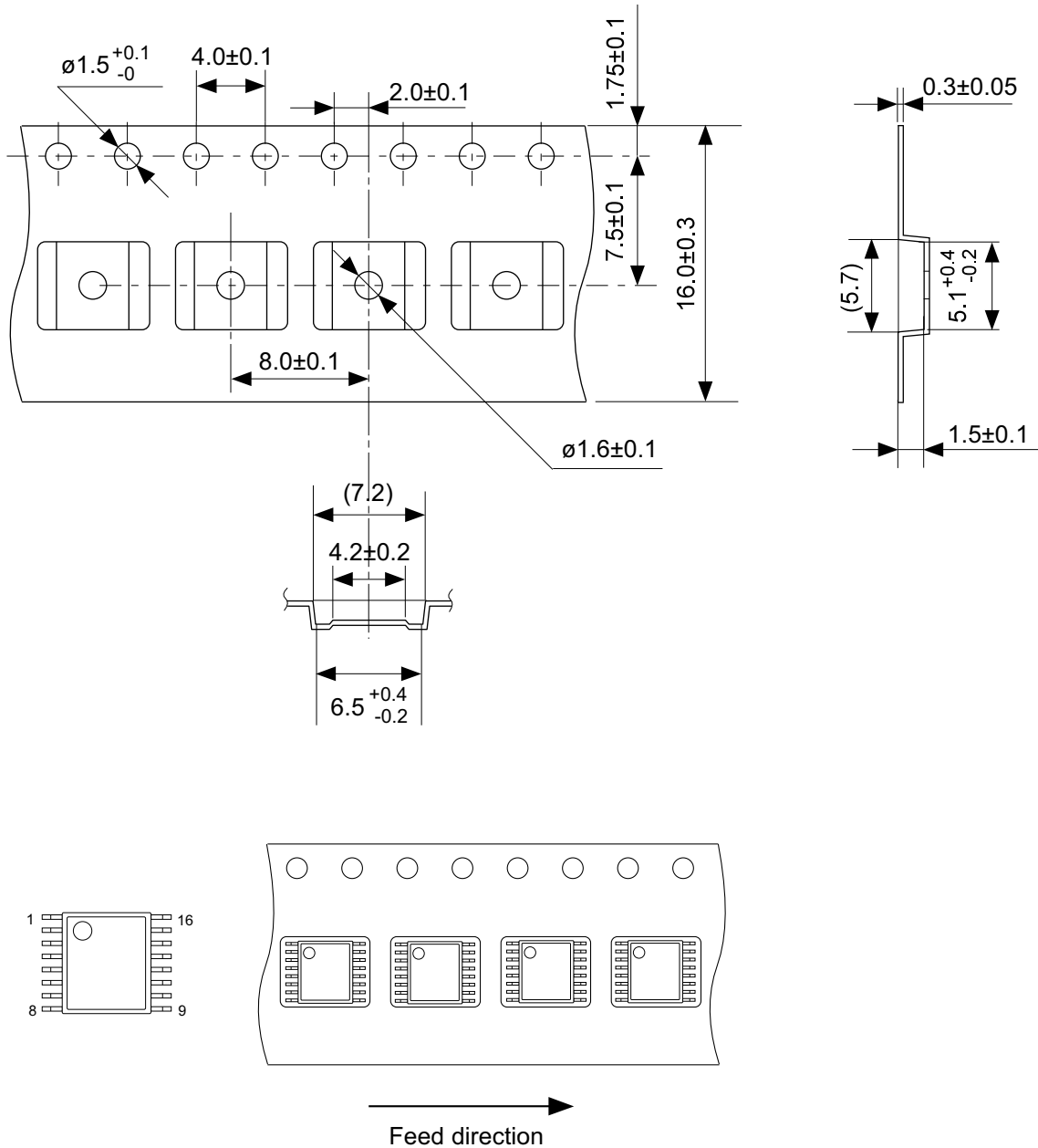
| Item | | Specification |
|-----------------------------|---|---|
| Size [mm] | | 114.3 x 76.2 x t1.6 |
| Material | | FR-4 |
| Number of copper foil layer | | 4 |
| Copper foil layer [mm] | 1 | Land pattern and wiring for testing: t0.070 |
| | 2 | 74.2 x 74.2 x t0.035 |
| | 3 | 74.2 x 74.2 x t0.035 |
| | 4 | 74.2 x 74.2 x t0.070 |
| Thermal via | | - |

No. TSSOP16-A-Board-SD-1.0



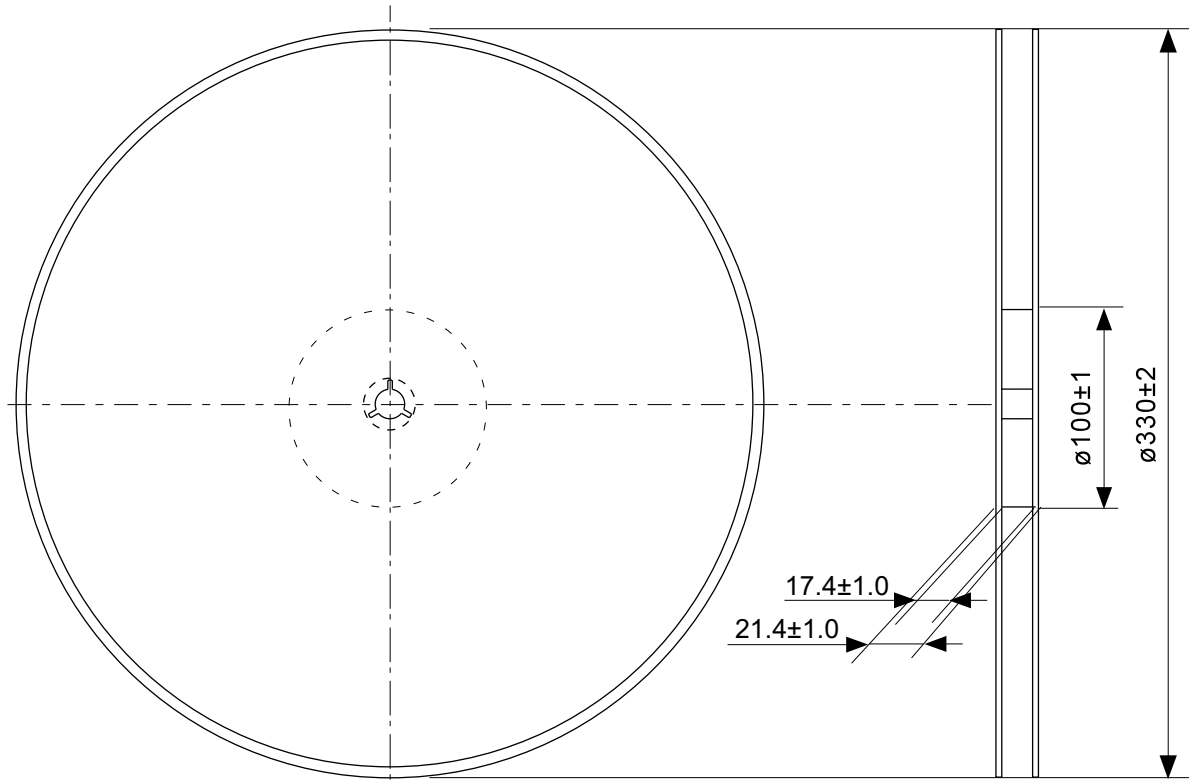
No. FT016-A-P-SD-1.2

| | |
|-------------------|--------------------------|
| TITLE | TSSOP16-A-PKG Dimensions |
| No. | FT016-A-P-SD-1.2 |
| ANGLE | |
| UNIT | mm |
| ABLIC Inc. | |

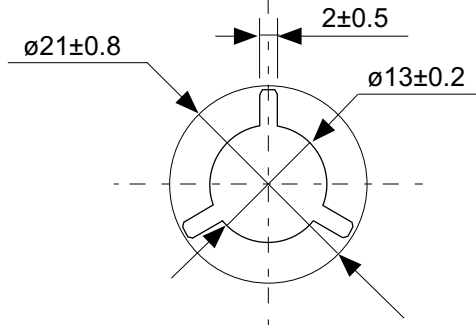


No. FT016-A-C-SD-1.1

| | |
|-------------------|------------------------|
| TITLE | TSSOP16-A-Carrier Tape |
| No. | FT016-A-C-SD-1.1 |
| ANGLE | |
| UNIT | mm |
| ABLIC Inc. | |



Enlarged drawing in the central part



No. FT016-A-R-S1-2.0

| | | | |
|-------------------|------------------|------|-------|
| TITLE | TSSOP16-A- Reel | | |
| No. | FT016-A-R-S1-2.0 | | |
| ANGLE | | QTY. | 4,000 |
| UNIT | mm | | |
| | | | |
| ABLIC Inc. | | | |

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The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
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