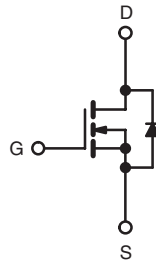
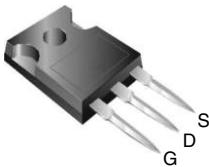


Power MOSFET

| PRODUCT SUMMARY | | |
|---------------------------|-----------------|------|
| V_{DS} (V) | 500 | |
| $R_{DS(on)}$ (Ω) | $V_{GS} = 10$ V | 0.24 |
| Q_g (Max.) (nC) | 124 | |
| Q_{gs} (nC) | 40 | |
| Q_{gd} (nC) | 57 | |
| Configuration | Single | |

TO-247


N-Channel MOSFET

FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Effective C_{OSS} Specified
- Lead (Pb)-free Available


RoHS*
 COMPLIANT

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching

TYPICAL SMPS TOPOLOGIES

- Full Bridge
- Power Factor Correction Boost

| ORDERING INFORMATION | |
|----------------------|--------------|
| Package | TO-247 |
| Lead (Pb)-free | IRFP460NPbF |
| | SiHFP460N-E3 |
| SnPb | IRFP460N |
| | SiHFP460N |


| ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted | | | | |
|--|------------------|------------------|------|----------|
| PARAMETER | SYMBOL | LIMIT | UNIT | |
| Drain-Source Voltage | V_{DS} | 500 | V | |
| Gate-Source Voltage | V_{GS} | ± 30 | | |
| Continuous Drain Current | V_{GS} at 10 V | $T_C = 25$ °C | 20 | A |
| | | $T_C = 100$ °C | 13 | |
| Pulsed Drain Current ^a | I_{DM} | 80 | | |
| Linear Derating Factor | | 2.2 | W/°C | |
| Single Pulse Avalanche Energy ^b | E_{AS} | 340 | mJ | |
| Repetitive Avalanche Current ^a | I_{AR} | 20 | A | |
| Repetitive Avalanche Energy ^a | E_{AR} | 28 | mJ | |
| Maximum Power Dissipation | $T_C = 25$ °C | P_D | 280 | W |
| Peak Diode Recovery dV/dt^c | dV/dt | 5.0 | V/ns | |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | - 55 to + 150 | °C | |
| Soldering Recommendations (Peak Temperature) | for 10 s | 300 ^d | | |
| Mounting Torque | 6-32 or M3 screw | | 10 | lbf · in |
| | | | 1.1 | N · m |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25$ °C, $L = 1.8$ mH, $R_G = 25$ Ω , $I_{AS} = 20$ A (see fig. 12).
- $I_{SD} \leq 20$ A, $dI/dt \leq 140$ A/ μ s, $V_{DD} \leq V_{DS}$, $T_J \leq 150$ °C.
- 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

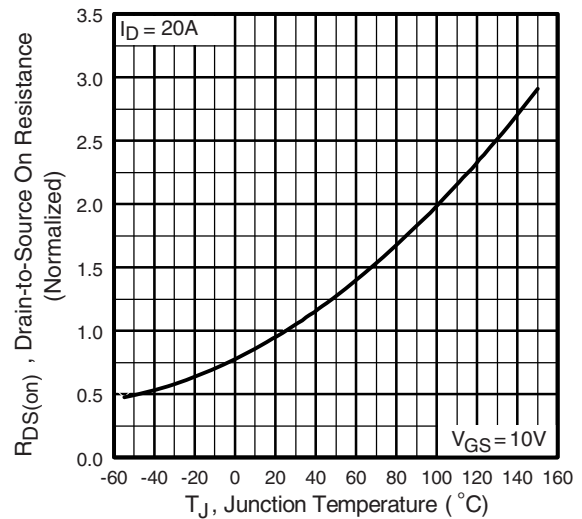
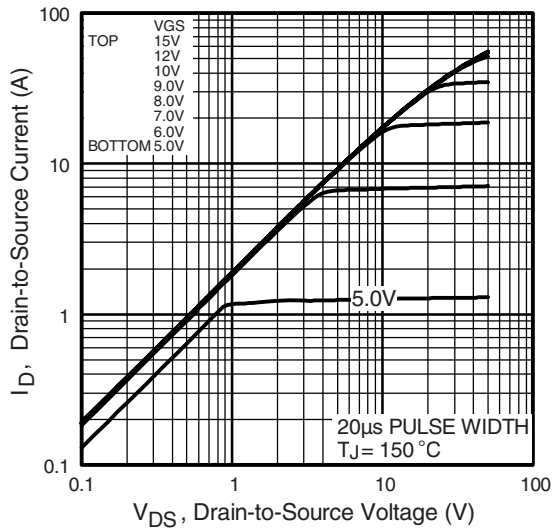
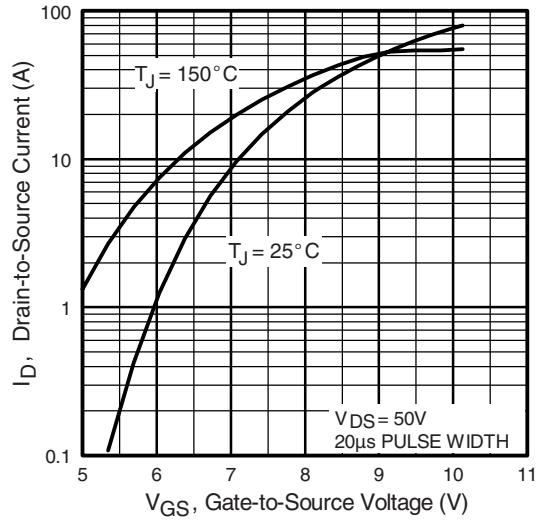
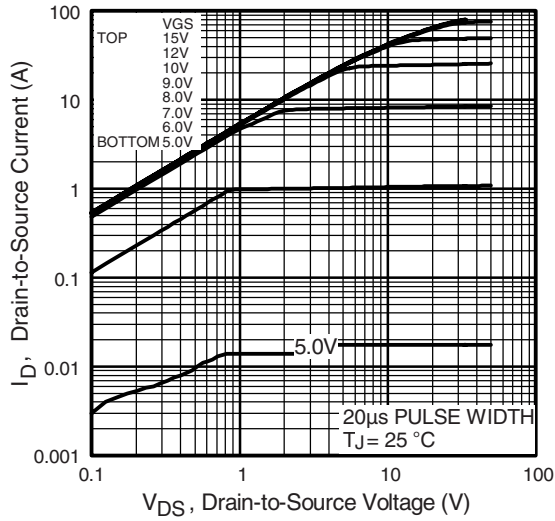
| THERMAL RESISTANCE RATINGS | | | | |
|-------------------------------------|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient | R_{thJA} | - | 40 | °C/W |
| Case-to-Sink, Flat, Greased Surface | R_{thCS} | 0.24 | - | |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 0.45 | |

| SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted | | | | | | | |
|--|-----------------------|--|---|------|-----------|---------------|----|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT | |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$ | 500 | - | - | V | |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$ | - | 580 | - | mV/°C | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 3.0 | - | 5.0 | V | |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 30\text{ V}$ | - | - | ± 100 | nA | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 500\text{ V}$, $V_{GS} = 0\text{ V}$ | - | - | 25 | μA | |
| | | $V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 125\text{ }^\circ\text{C}$ | - | - | 250 | | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$, $I_D = 12\text{ A}^b$ | - | - | 0.24 | Ω | |
| Forward Transconductance | g_{fs} | $V_{DS} = 50\text{ V}$, $I_D = 12\text{ A}$ | 10 | - | - | S | |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5 | - | 3540 | - | pF | |
| Output Capacitance | C_{oss} | | - | 350 | - | | |
| Reverse Transfer Capacitance | C_{rss} | | - | 30 | - | | |
| Output Capacitance | C_{oss} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 1.0\text{ V}$, $f = 1.0\text{ MHz}$ | - | 3930 | - | |
| Effective Output Capacitance | $C_{oss\text{ eff.}}$ | | $V_{DS} = 400\text{ V}$, $f = 1.0\text{ MHz}$ | - | 95 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 20\text{ A}$, $V_{DS} = 400\text{ V}$ see fig. 6 and 13 ^b | - | - | 124 | nC |
| Gate-Source Charge | Q_{gs} | | | - | - | 40 | |
| Gate-Drain Charge | Q_{gd} | | | - | - | 57 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 250\text{ V}$, $I_D = 20\text{ A}$ $R_G = 4.3\text{ }\Omega$, $R_D = 13\text{ }\Omega$, see fig. 10 ^b | - | 23 | - | ns | |
| Rise Time | t_r | | - | 87 | - | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 34 | - | | |
| Fall Time | t_f | | - | 33 | - | | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 20 | A | |
| Pulsed Diode Forward Current ^a | I_{SM} | | - | - | 80 | | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}$, $I_S = 20\text{ A}$, $V_{GS} = 0\text{ V}^b$ | - | - | 1.8 | V | |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}$, $I_F = 20\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$ | - | 550 | 825 | ns | |
| Body Diode Reverse Recovery Charge | Q_{rr} | | - | 7.2 | 10.8 | μC | |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80 % V_{DS} .

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



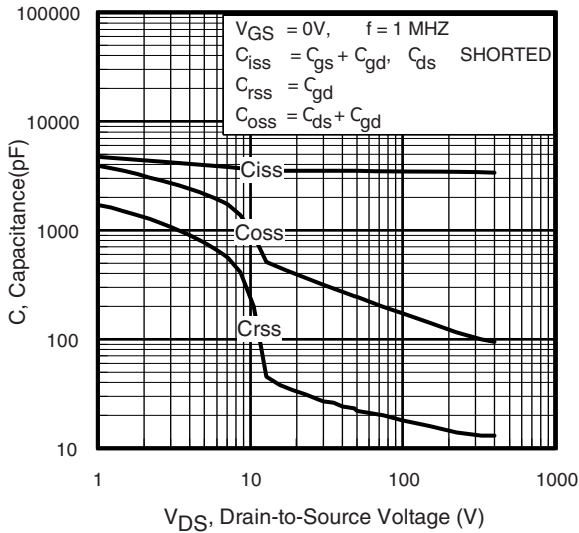


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

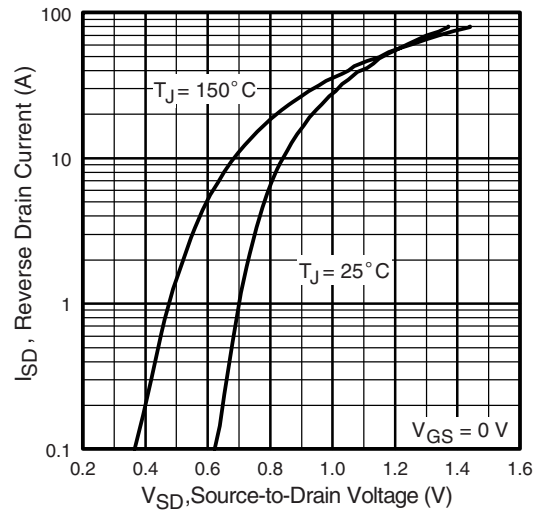


Fig. 7 - Typical Source-Drain Diode Forward Voltage

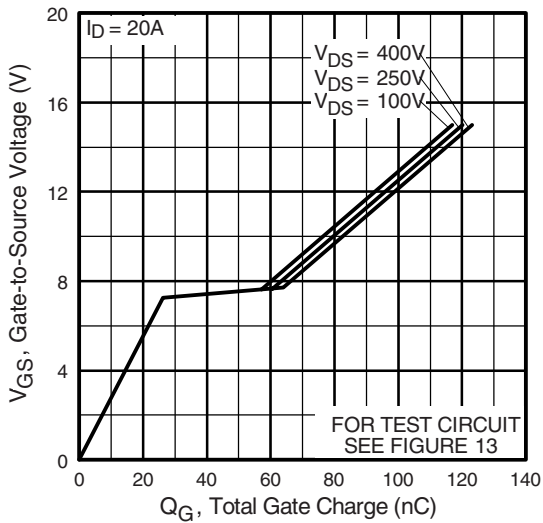


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

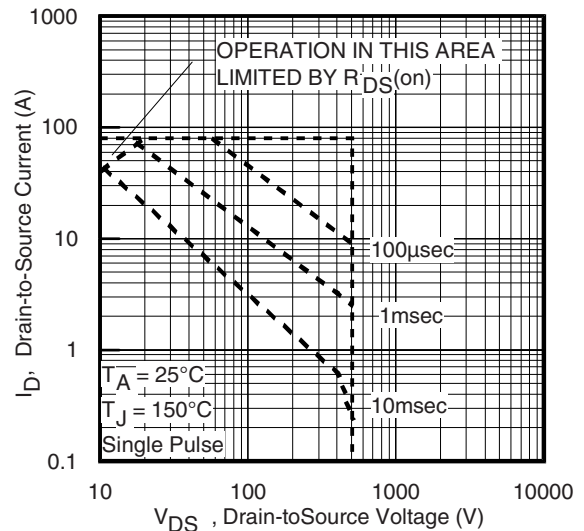


Fig. 8 - Maximum Safe Operating Area

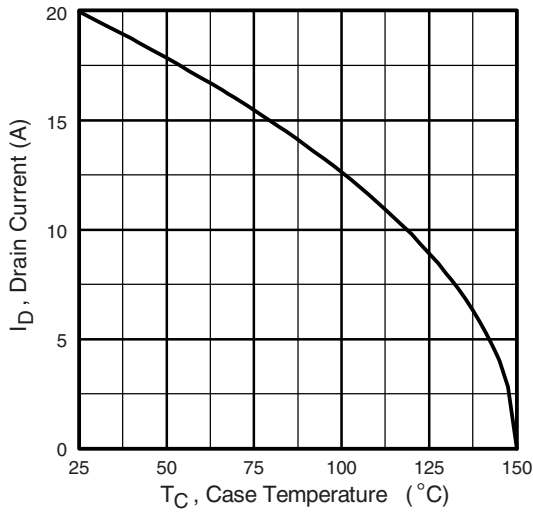


Fig. 9 - Maximum Drain Current vs. Case Temperature

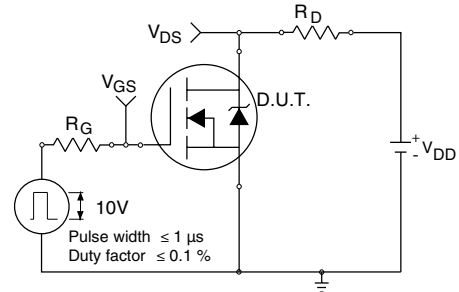


Fig. 10a - Switching Time Test Circuit

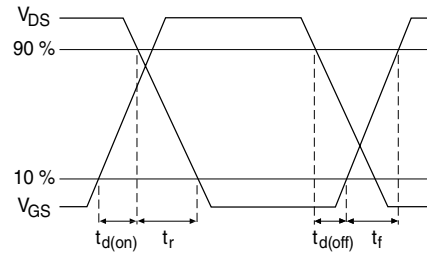


Fig. 10b - Switching Time Waveforms

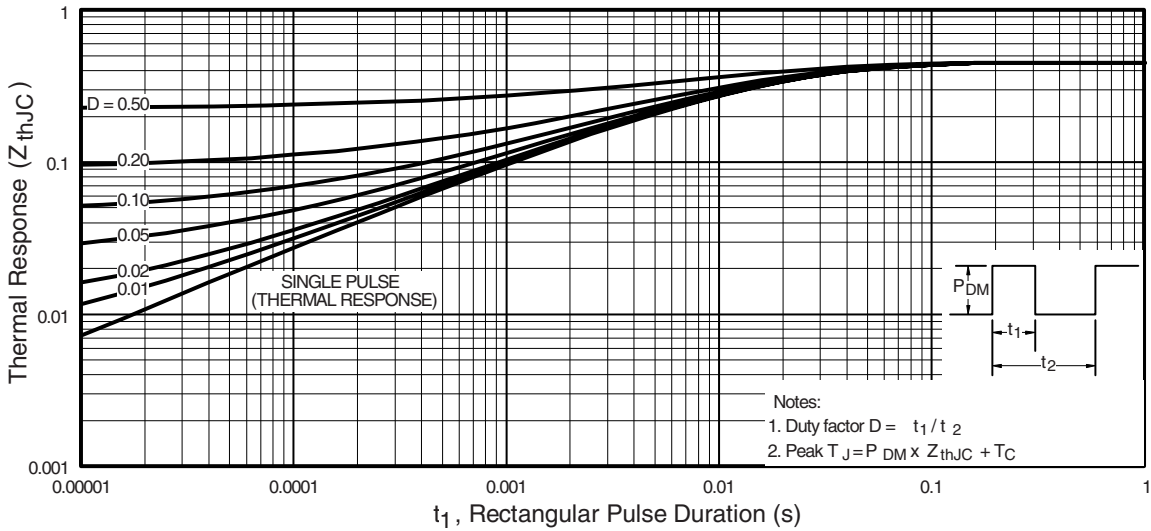


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

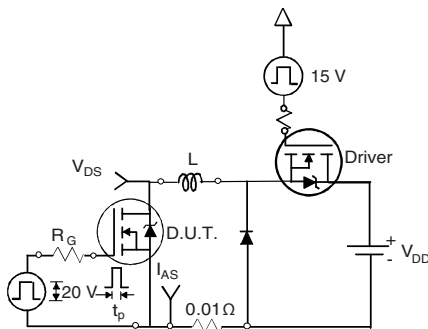


Fig. 12a - Unclamped Inductive Test Circuit

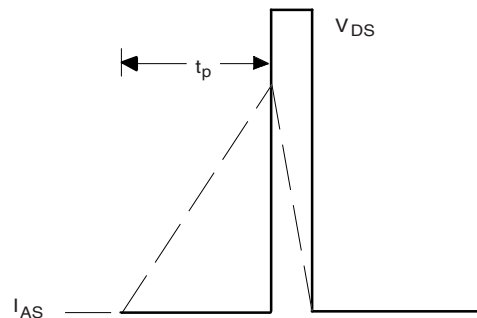


Fig. 12b - Unclamped Inductive Waveforms

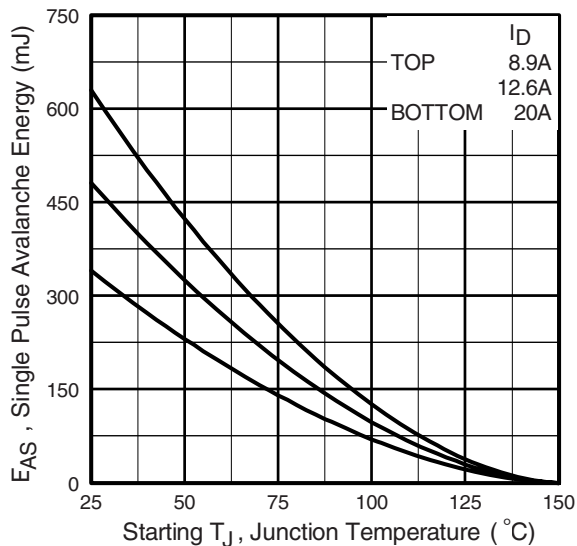


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

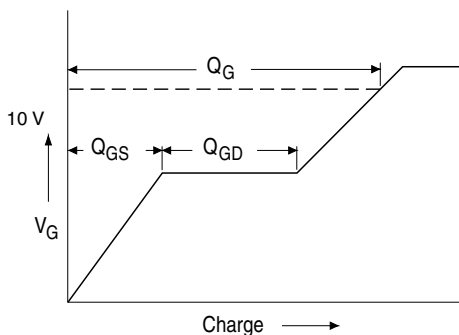


Fig. 13a - Basic Gate Charge Waveform

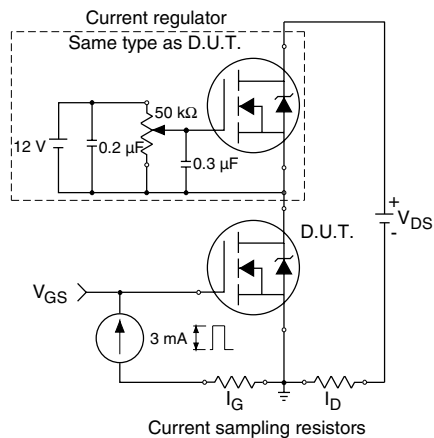
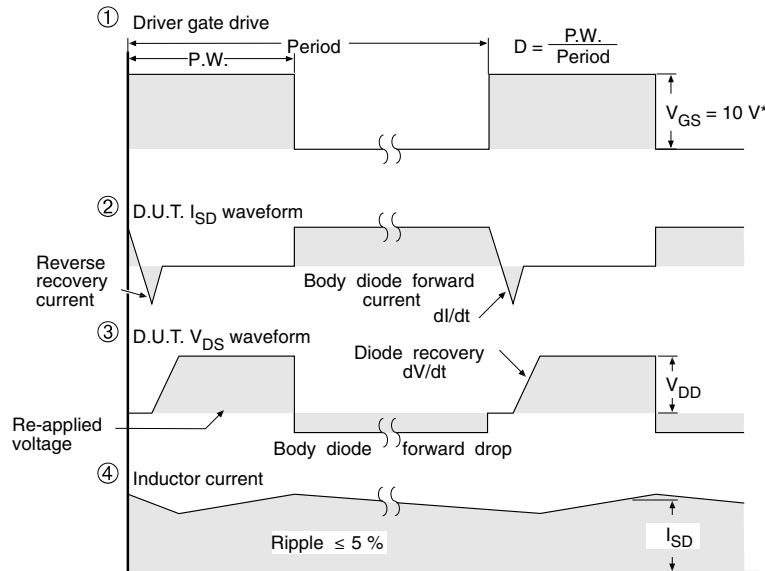
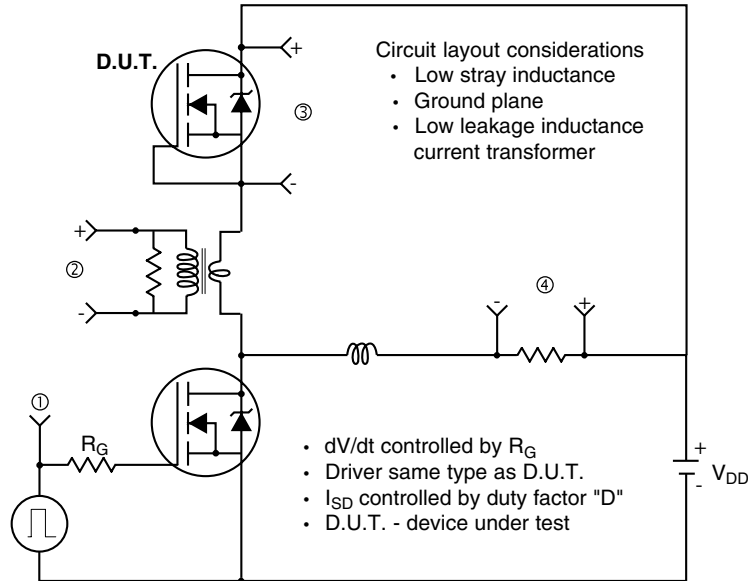


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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