THS309x High-Voltage, Low-Distortion, Current-Feedback Operational Amplifiers

1 Features

- Low distortion:
  - 77-dBc HD2 at 10 MHz, R_L = 1 kΩ
  - 69-dBc HD3 at 10 MHz, R_L = 1 kΩ
- Low noise:
  - 14-pA/√Hz noninverting current noise
  - 17-pA/√Hz inverting current noise
  - 2-nV/√Hz voltage noise
- High slew rate: 7300 V/µs (G = 5, V_O = 20 V_{PP})
- Wide bandwidth: 210 MHz (G = 2, R_L = 100 Ω)
- High output current drive: ±250 mA
- Wide supply range: ±5 V to ±15 V
- Power-down feature: THS3095 only

2 Applications

- High-voltage arbitrary waveform generators
- Power FET drivers
- Pin drivers
- VDSL line drivers

3 Description

The THS3091 and THS3095 are high-voltage, low-distortion, high-speed, current-feedback amplifiers designed to operate over a wide supply range of ±5 V to ±15 V for applications requiring large, linear output signals such as pin drivers, power FET drivers & arbitrary waveform generators.

The THS3095 features a power-down pin ($\overline{PD}$) that puts the amplifier in low power standby mode, and lowers the quiescent current from 9.5 mA to 500 µA.

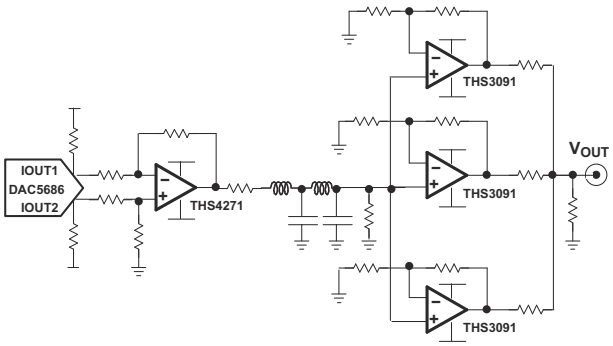
The wide supply range, combined with total harmonic distortion as low as –69 dBc at 10 MHz, in addition to the high slew rate of 7300 V/µs makes the THS309x ideally suited for high-voltage arbitrary waveform driver applications. Moreover, having the ability to handle large voltage swings driving into high-resistance and high-capacitance loads while maintaining good settling time performance makes the devices ideal for Pin driver and Power FET driver applications.

The THS3091 and THS3095 are offered in an 8-pin SOIC (D), and the 8-pin SOIC (DDA) packages with PowerPAD™. The THS3091 is also offered in an additional 8-pin HVSSOP (DGN) package.

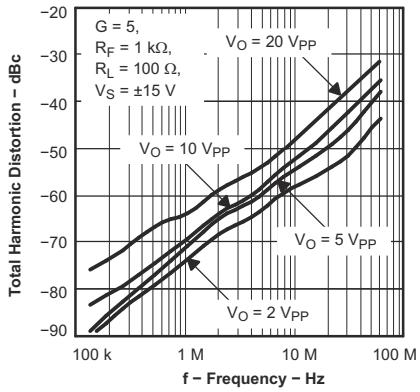
Package Information(1)(3)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
THS309x	D (SOIC, 8)	4.90 mm × 3.91 mm
	DDA (SO PowerPAD, 8)	4.89 mm × 3.90 mm
	DGN (HVSSOP, 8)(2)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Preview package
(3) See *Device Comparison Table*



Typical Arbitrary Waveform Generator Output Drive Circuit



Total Harmonic Distortion vs Frequency

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (October 2015) to Revision I (December 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added the *DGN* package information to the data sheet	1
• Added the *Device Comparison Table* section	3
• Updated *Thermal Information* table	5

Changes from Revision G (February, 2007) to Revision H (October 2015)	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

Changes from Revision F (February, 2007) to Revision G (February, 2007)	Page
• Changed common-mode rejection ratio specifications from 78 dB (typ) to 69 dB (typ); from 68 dB at +25°C to 62 dB; from 65 dB at (0°C to +70°C) and (–40°C to +85°C) to 59 dB	6
• Corrected load resistor value for output current specification (sourcing and sinking) from R_L = 40 Ω to R_L = 10 Ω	8
• Changed output current (sourcing) specifications from 200 mA (typ) to 180 mA (typ); from 160 mA at +25°C to 140 mA; from 140 mA at (0°C to +70°C) and (–40°C to +85°C) to 120 mA	8
• Corrected output current (sinking) specifications from 180 mA (typ) to –160 mA (typ); from 150 mA at +25°C to –140 mA; from 125 mA at (0°C to +70°C) and (–40°C to +85°C) to –120 mA	8

5 Device Comparison Table

DEVICE	SUPPLY, V_S (V)	SSBW, A_V = 5 (MHz)	MAXIMUM ICC AT 25°C (mA)	INPUT NOISE V_n (nV/√Hz)	HD2/3, 10 V_{PP} AT 50 MHz, G = 5 V/V (dBc)	SLEW RATE (V/µs)	LINEAR OUTPUT CURRENT (mA)
THS3491	±15	900	17.3	1.7	–76/–75	7100(1)	±420
THS3095	±15	190	9.5	1.6	–40/–42	1200(2)	±250
THS3001	±15	350	9	1.6	N/A	1400(3)	±120
THS3061	±15	260	8.3	2.6	N/A	1060(4)	±140

(1) Slew rate from FPBW of 320 MHz, 10 V_{PP}
(2) Slew rate from FPBW of 135 MHz, 4 V_{PP}
(3) Slew rate from FPBW of 32 MHz, 20 V_{PP}
(4) Slew rate from FPBW of 120 MHz, 4 V_{PP}

6 Pin Configuration and Functions

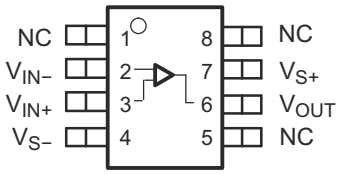


Figure 6-1. D, DGN, or DDA Package, 8-Pin SOIC, HVSSOP, or SO-PowerPAD THS3091 (Top View)

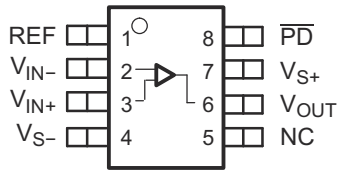


Figure 6-2. D or DDA Package, 8-Pin SOIC or SO-PowerPAD THS3095 (Top View)

Table 6-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	NO.			
	THS3091	THS3095		
NC	1, 5, 8	5	—	No connection
$\overline{PD}$	—	8	I	Amplifier power down, LOW – Amplifier disabled, HIGH (default) – Amplifier enabled
REF	—	1	I	Voltage reference input to set $\overline{PD}$ threshold level
V_{OUT}	6	6	O	Output of amplifier
V_{IN-}	2	2	I	Inverting input
V_{IN+}	3	3	I	Noninverting input
V_{S-}	4	4	POW	Negative power supply
V_{S+}	7	7	POW	Positive power supply

(1) I= input, O = output, POW= power, and NC = no internal connection

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{S-} to V_{S+}	Supply voltage		33	V
V_I	Input voltage			$\pm V_S$
V_{ID}	Differential input voltage		4	±V
I_O	Output current		350	mA
	Continuous power dissipation	See *Section 7.2*		
T_J	Maximum junction temperature		150	°C
T_J (2)	Maximum junction temperature, continuous operation, long-term reliability		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply voltage		Dual supply	±5	±15	±16	V
		Single supply	10	30	32	
T_A	Operating free-air temperature		–40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		THS309x			UNIT
		D (SOIC)	DDA (SO PowerPAD)	DGN (HVSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.5	51.8	60.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.7	58.3	87.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.2	32.3	32.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.5	12.2	7.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.7	32.2	32.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	7.8	17.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics THS3091

V_S = ±15 V, R_F = 1.21 kΩ, R_L = 100 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
AC PERFORMANCE							
Small-signal bandwidth, –3 dB	G = 1, R_F = 1.78 kΩ, V_O = 200 mV_{PP}	T_A = 25°C			235		MHz
	G = 2, R_F = 1.21 kΩ, V_O = 200 mV_{PP}	T_A = 25°C			210		
	G = 5, R_F = 1 kΩ, V_O = 200 mV_{PP}	T_A = 25°C			190		
	G = 10, R_F = 866 Ω, V_O = 200 mV_{PP}	T_A = 25°C			180		
0.1-dB Bandwidth flatness	G = 2, R_F = 1.21 kΩ, V_O = 200 mV_{PP}	T_A = 25°C			95		
Large-signal bandwidth	G = 5, R_F = 1 kΩ , V_O = 4 V_{PP}	T_A = 25°C			135		
Slew rate (25% to 75% level)	G = 2, V_O = 10-V step, R_F = 1.21 kΩ	T_A = 25°C			5000		V/µs
	G = 5, V_O = 20-V step, R_F = 1 kΩ	T_A = 25°C			7300		
Rise and fall time	G = 2, V_O = 5-V_{PP}, R_F = 1.21 kΩ	T_A = 25°C			5		ns
Settling time to 0.1%	G = –2, V_O = 2 V_{PP} step	T_A = 25°C			42		ns
Settling time to 0.01%	G = –2, V_O = 2 V_{PP} step	T_A = 25°C			72		
HARMONIC DISTORTION							
2nd Harmonic distortion	G = 2, R_F = 1.21 kΩ, V_O = 2 V_{PP}, f = 10 MHz	R_L = 100 Ω	T_A = 25°C		66		dBc
		R_L = 1 kΩ	T_A = 25°C		77		
3rd Harmonic distortion		R_L = 100 Ω	T_A = 25°C		74		
		R_L = 1 kΩ	T_A = 25°C		69		
Input voltage noise	f > 10 kHz		T_A = 25°C		2		nV / √Hz
Noninverting input current noise	f > 10 kHz		T_A = 25°C		14		pA / √Hz
Inverting input current noise	f > 10 kHz		T_A = 25°C		17		pA / √Hz
Differential gain	G = 2, R_L = 150 Ω, R_F = 1.21 kΩ	NTSC	T_A = 25°C		0.013%		
		PAL	T_A = 25°C		0.011%		
Differential phase		NTSC	T_A = 25°C		0.020°		
		PAL	T_A = 25°C		0.026°		
DC PERFORMANCE							
Transimpedance	V_O = ±7.5 V, Gain = 1		T_A = 25°C		850		kΩ
			T_A = 25°C	350			
			T_A = 0°C to 70°C	300			
			T_A = –40°C to 85°C	300			
Input offset voltage	V_{CM} = 0 V		T_A = 25°C		0.9		mV
			T_A= 25°C			3	
			T_A = 0°C to 70°C			4	
			T_A = –40°C to 85°C			4	
Average offset voltage drift	V_{CM} = 0 V		T_A = 0°C to 70°C		±10		µV/°C
			T_A = –40°C to 85°C		±10		
Noninverting input bias current	V_{CM} = 0 V		T_A = 25°C		4		µA
			T_A= 25°C			15	
			T_A = 0°C to 70°C			20	
			T_A = –40°C to 85°C			20	
Average bias current drift	V_{CM} = 0 V		T_A = 0°C to 70°C		±20		nA/°C
			T_A = –40°C to 85°C		±20		
Inverting input bias current	V_{CM} = 0 V		T_A = 25°C		3.5		µA
			T_A= 25°C			15	
			T_A = 0°C to 70°C			20	
			–40°C to 85°C			20	
Average bias current drift	V_{CM} = 0 V		T_A = 0°C to 70°C		±20		nA/°C
			T_A = –40°C to 85°C		±20		

7.5 Electrical Characteristics THS3091 (continued)

V_S = ±15 V, R_F = 1.21 kΩ, R_L = 100 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset current	V_{CM} = 0 V	T_A = 25°C		1.7		μA
		T_A= 25°C			10	
		T_A = 0°C to 70°C			15	
		T_A = –40°C to 85°C			15	
Average offset current drift	V_{CM} = 0 V	T_A = 0°C to 70°C		±20		nA/°C
		T_A = –40°C to 85°C		±20		
INPUT CHARACTERISTICS						
Common-mode input range		T_A = 25°C		±13.6		V
		T_A= 25°C	±13.3			
		T_A = 0°C to 70°C	±13			
		T_A = –40°C to 85°C	±13			
Common-mode rejection ratio	V_{CM} = ±10 V	T_A = 25°C		69		dB
		T_A= 25°C	62			
		T_A = 0°C to 70°C	59			
		T_A = –40°C to 85°C	59			
Noninverting input resistance		T_A = 25°C		1.3		MΩ
Noninverting input capacitance		T_A = 25°C		0.1		pF
Inverting input resistance		T_A = 25°C		30		Ω
Inverting input capacitance		T_A = 25°C		1.4		pF
OUTPUT CHARACTERISTICS						
Output voltage swing	R_L = 1 kΩ	T_A = 25°C		±13.2		V
		T_A = 25°C	±12.8			
		T_A = 0°C to 70°C	±12.5			
		T_A = –40°C to 85°C	±12.5			
	R_L = 100 Ω	T_A = 25°C		±12.5		
		T_A= 25°C	±12.1			
		T_A = 0°C to 70°C	±11.8			
		T_A = –40°C to 85°C	±11.8			
Output current (sourcing)	R_L = 40 Ω	T_A= 25°C		280		mA
		T_A = 25°C	225			
		T_A = 0°C to 70°C	200			
		T_A = –40°C to 85°C	200			
Output current (sinking)	R_L = 40 Ω	T_A = 25°C		250		mA
		T_A= 25°C	200			
		T_A = 0°C to 70°C	175			
		T_A = –40°C to 85°C	175			
Output impedance	f = 1 MHz, Closed loop	T_A = 25°C		0.06		Ω
POWER SUPPLY						
Specified operating voltage		T_A = 25°C		±15		V
		T_A= 25°C			±16	
		T_A = 0°C to 70°C			±16	
		T_A = –40°C to 85°C			±16	
Maximum quiescent current		T_A = 25°C		9.5		mA
		T_A= 25°C			10.5	
		T_A = 0°C to 70°C			11	
		T_A = –40°C to 85°C			11	

7.5 Electrical Characteristics THS3091 (continued)

V_S = ±15 V, R_F = 1.21 kΩ, R_L = 100 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Minimum quiescent current		T_A = 25°C		9.5		mA
		T_A= 25°C	8.5			
		T_A = 0°C to 70°C	8			
		T_A = –40°C to 85°C	8			
Power supply rejection (+PSRR)	V_{S+} = 15.5 V to 14.5 V, $V_{S–}$ = 15 V	T_A = 25°C		75		dB
		T_A= 25°C	70			
		T_A = 0°C to 70°C	65			
		T_A = –40°C to 85°C	65			
Power supply rejection (–PSRR)	V_{S+} = 15 V, $V_{S–}$ = –15.5 V to –14.5 V	T_A = 25°C		73		dB
		T_A= 25°C	68			
		T_A = 0°C to 70°C	65			
		T_A = –40°C to 85°C	65			
POWER-DOWN CHARACTERISTICS (THS3091 ONLY)						
REF voltage range(1)		T_A = 25°C		V_{S+} –4		V
		T_A = 25°C		$V_{S–}$		
Power-down voltage level(1)	Enable	T_A = 25°C		$\overline{PD}$ ≥ REF +2		V
	Disable	T_A = 25°C		$\overline{PD}$ ≤ REF +.8		
Power-down quiescent current	$\overline{PD}$ = 0V	T_A = 25°C		500		µA
		T_A= 25°C			700	
		T_A = 0°C to 70°C			800	
		T_A = –40°C to 85°C			800	
V_{PD} quiescent current	V_{PD} = 0 V, REF = 0 V,	T_A = 25°C		11		µA
		T_A= 25°C			15	
		T_A = 0°C to 70°C			20	
		T_A = –40°C to 85°C			20	
	V_{PD} = 3.3 V, REF = 0 V	T_A = 25°C		11		
		T_A= 25°C			15	
		T_A = 0°C to 70°C			20	
		T_A = –40°C to 85°C			20	
Turnon time delay	90% of final value	T_A = 25°C		60		µs
Turnoff time delay	10% of final value	T_A = 25°C		150		

(1) For detailed information on the behavior of the power-down circuit, see the *power-down functionality* and *power-down reference* sections in the Application Information section of this data sheet.

7.6 Electrical Characteristics THS3095

V_S = ±5 V, R_F = 1.15 kΩ, R_L = 100 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE						
Small-signal bandwidth, –3 dB	G = 1, R_F = 1.78 kΩ, V_O = 200 mV_{PP}	T_A= 25°C		190		MHz
	G = 2, R_F = 1.15 kΩ, V_O = 200 mV_{PP}	T_A= 25°C		180		
	G = 5, R_F = 1 kΩ, V_O = 200 mV_{PP}	T_A= 25°C		160		
	G = 10, R_F = 866 Ω, V_O = 200 mV_{PP}	T_A= 25°C		150		
0.1-dB Bandwidth flatness	G = 2, R_F = 1.15 kΩ, V_O = 200 mV_{PP}	T_A= 25°C		65		
Large-signal bandwidth	G = 2, R_F = 1.15 kΩ , V_O = 4 V_{PP}	T_A= 25°C		160		
Slew rate (25% to 75% level)	G = 2, V_O= 5-V step, R_F = 1.21 kΩ	T_A= 25°C		1400		V/µs
	G = 5, V_O= 5-V step, R_F = 1 kΩ	T_A= 25°C		1900		
Rise and fall time	G = 2, V_O = 5-V step, R_F = 1.21 kΩ	T_A= 25°C		5		ns

7.6 Electrical Characteristics THS3095 (continued)

V_S = ±5 V, R_F = 1.15 kΩ, R_L = 100 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Settling time to 0.1%	G = –2, V_O = 2 V_{PP} step	T_A= 25°C			35		ns
Settling time to 0.01%	G = –2, V_O = 2 V_{PP} step	T_A= 25°C			73		
HARMONIC DISTORTION							
2nd Harmonic distortion	G = 2, R_F = 1.15 kΩ, V_O = 2 V_{PP}, f = 10 MHz	R_L = 100 Ω	T_A = 25°C		77		dBc
		R_L = 1 kΩ	T_A = 25°C		73		
3rd Harmonic distortion		R_L = 100 Ω	T_A = 25°C		70		
		R_L = 1 kΩ	T_A = 25°C		68		
Input voltage noise	f > 10 kHz		T_A = 25°C		2		nV / √Hz
Noninverting input current noise	f > 10 kHz		T_A = 25°C		14		pA / √Hz
Inverting input current noise	f > 10 kHz		T_A = 25°C		17		pA / √Hz
Differential gain	G = 2, R_L = 150 Ω, R_F = 1.15 kΩ	NTSC	T_A = 25°C		0.027%		
		PAL	T_A = 25°C		0.025%		
Differential phase		NTSC	T_A = 25°C		0.04°		
		PAL	T_A = 25°C		0.05°		
DC PERFORMANCE							
Transimpedance	V_O = ±2.5 V, Gain = 1	T_A = 25°C			700		kΩ
		T_A= 25°C		250			
		T_A= 0°C to 70°C		200			
		T_A= –40°C to 85°C		200			
Input offset voltage	V_{CM} = 0 V		T_A = 25°C		0.3		mV
			T_A= 25°C			2	
			T_A= 0°C to 70°C			3	
			T_A= –40°C to 85°C			3	
Average offset voltage drift	V_{CM} = 0 V		T_A= 0°C to 70°C		±10		µV/°C
			T_A= –40°C to 85°C		±10		
Noninverting input bias current	V_{CM} = 0 V		T_A = 25°C		2		µA
			T_A= 25°C			15	
			T_A= 0°C to 70°C			20	
			T_A= –40°C to 85°C			20	
Average bias current drift	V_{CM} = 0 V		T_A= 0°C to 70°C		±20		nA/°C
			T_A= –40°C to 85°C		±20		
Inverting input bias current	V_{CM} = 0 V		T_A = 25°C		5		µA
			T_A= 25°C			15	
			T_A= 0°C to 70°C			20	
			T_A= –40°C to 85°C			20	
Average bias current drift	V_{CM} = 0 V		T_A= 0°C to 70°C		±20		nA/°C
			T_A= –40°C to 85°C		±20		

7.6 Electrical Characteristics THS3095 (continued)

V_S = ±5 V, R_F = 1.15 kΩ, R_L = 100 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input offset current	V_{CM} = 0 V	T_A = 25°C		1		µA
		T_A= 25°C			10	
		T_A= 0°C to 70°C			15	
		T_A= –40°C to 85°C			15	
Average offset current drift	V_{CM} = 0 V	T_A= 0°C to 70°C		±20		nA/°C
		T_A= –40°C to 85°C		±20		
INPUT CHARACTERISTICS						
Common-mode input range		T_A = 25°C		±3.6		V
		T_A= 25°C	±3.3			
		T_A= 0°C to 70°C	±3			
		T_A= –40°C to 85°C	±3			
Common-mode rejection ratio	V_{CM} = ±2.0 V, V_O = 0 V	T_A = 25°C		66		dB
		T_A= 25°C	60			
		T_A= 0°C to 70°C	57			
		T_A= –40°C to 85°C	57			
Noninverting input resistance	T_A = 25°C			1.1		MΩ
Noninverting input capacitance	T_A = 25°C			1.2		pF
Inverting input resistance	T_A = 25°C			32		Ω
Inverting input capacitance	T_A = 25°C			1.5		pF

7.6 Electrical Characteristics THS3095 (continued)

V_S = ±5 V, R_F = 1.15 kΩ, R_L = 100 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT CHARACTERISTICS						
Output voltage swing	R_L = 1 kΩ	T_A = 25°C		±3.4		V
		T_A= 25°C	±3.1			
		T_A= 0°C to 70°C	±2.8			
		T_A= –40°C to 85°C	±2.8			
	R_L = 100 Ω	T_A = 25°C		±3.1		
		T_A= 25°C	±2.7			
		T_A= 0°C to 70°C	±2.5			
		T_A= –40°C to 85°C	±2.5			
Output current (sourcing)	R_L = 10 Ω	T_A = 25°C		180		mA
		T_A= 25°C	140			
		T_A= 0°C to 70°C	120			
		T_A= –40°C to 85°C	120			
Output current (sinking)	R_L = 10 Ω	T_A = 25°C		–160		mA
		T_A= 25°C	–140			
		T_A= 0°C to 70°C	–120			
		T_A= –40°C to 85°C	–120			
Output impedance	f = 1 MHz, Closed loop	T_A = 25°C		0.09		Ω
POWER SUPPLY						
Specified operating voltage	T_A = 25°C			±5		V
	T_A= 25°C				±4.5	
	T_A= 0°C to 70°C				±4.5	
	T_A= –40°C to 85°C				±4.5	
Maximum quiescent current	T_A = 25°C			8.2		mA
	T_A= 25°C				9	
	T_A= 0°C to 70°C				9.5	
	T_A= –40°C to 85°C				9.5	
Minimum quiescent current	T_A = 25°C			8.2		mA
	T_A= 25°C		7			
	T_A= 0°C to 70°C		6.5			
	T_A= –40°C to 85°C		6.5			
Power supply rejection (+PSRR)	V_{S+} = 5.5 V to 4.5 V, $V_{S–}$ = 5 V	T_A = 25°C		73		dB
		T_A= 25°C	68			
		T_A= 0°C to 70°C	63			
		T_A= –40°C to 85°C	63			
Power supply rejection (–PSRR)	V_{S+} = 5 V, $V_{S–}$ = –4.5 V to –5.5 V	T_A = 25°C		71		dB
		T_A= 25°C	65			
		T_A= 0°C to 70°C	60			
		T_A= –40°C to 85°C	60			

7.6 Electrical Characteristics THS3095 (continued)

V_S = ±5 V, R_F = 1.15 kΩ, R_L = 100 Ω, and G = 2 (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER-DOWN CHARACTERISTICS (THS3095 ONLY)						
REF voltage range(1)	T_A = 25°C			V_{S+} –4		V
	T_A = 25°C			$V_{S–}$		
Power-down voltage level(1)	Enable	T_A = 25°C		$\overline{PD}$ ≥ REF 2		V
	Disable	T_A = 25°C		$\overline{PD}$ ≤ REF 0.8		
Power-down quiescent current	$\overline{PD}$ = 0V	T_A = 25°C		300		µA
		T_A= 25°C			500	
		T_A= 0°C to 70°C			600	
		T_A= –40°C to 85°C			600	
V_{PD} quiescent current	V_{PD} = 0 V, REF = 0 V,	T_A = 25°C		11		µA
		T_A= 25°C			15	
		T_A= 0°C to 70°C			20	
		T_A–40°C to 85°C			20	
	V_{PD} = 3.3 V, REF = 0 V	T_A = 25°C		11		
		T_A= 25°C			15	
		T_A= 0°C to 70°C			20	
		T_A= –40°C to 85°C			20	
Turnon time delay	90% of final value	T_A = 25°C		60		µs
Turnoff time delay	10% of final value	T_A = 25°C		150		

(1) For detailed information on the behavior of the power-down circuit, see the *power-down functionality* and *power-down reference* sections in the Application Information section of this data sheet.

7.7 Dissipation Ratings Table

PACKAGE	θ_{JC} (°C/W)	θ_{JA} (°C/W)(1)	POWER RATING (2) T_J = 125°C	
			T_A = 25°C	T_A = 85°C
D-8	38.3	97.5	1.02 W	410 mW
DDA-8	9.2	45.8	2.18 W	873 mW

(1) This data was taken using the JEDEC standard High-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability.

7.8 Typical Characteristics (±15 V)

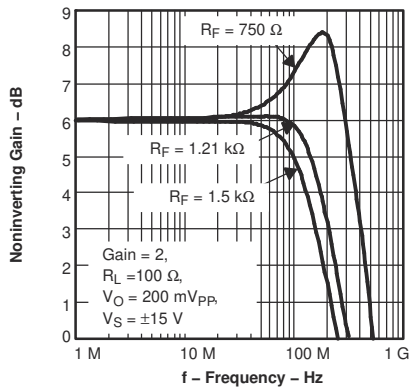


Figure 7-1. Noninverting Small-Signal Frequency Response

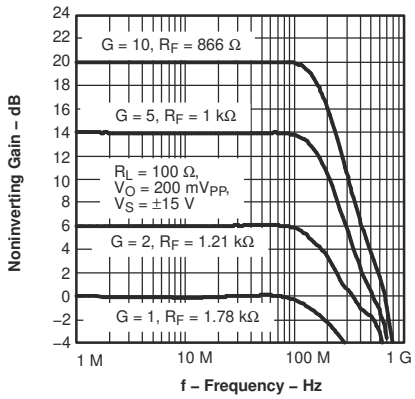


Figure 7-2. Noninverting Small-Signal Frequency Response

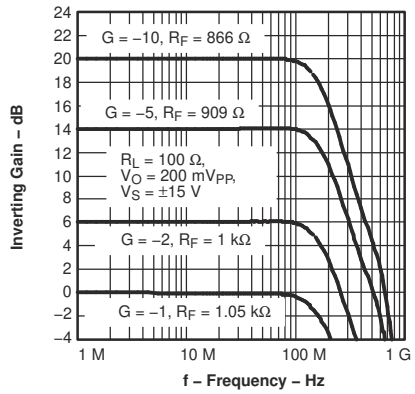


Figure 7-3. Inverting Small-Signal Frequency Response

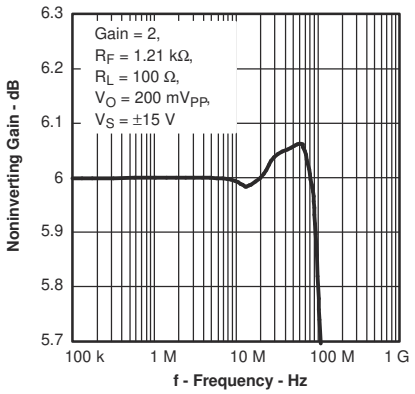


Figure 7-4. 0.1-db Gain Flatness Frequency Response

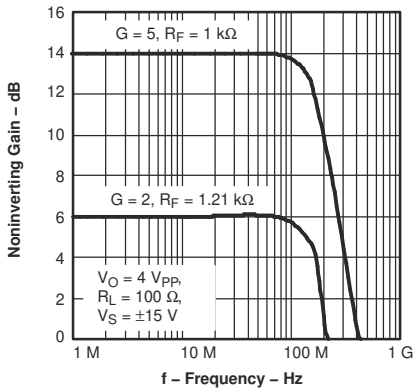


Figure 7-5. Noninverting Large-Signal Frequency Response

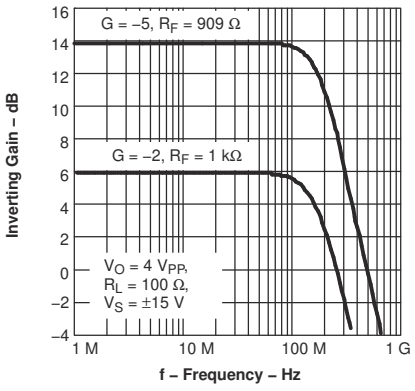


Figure 7-6. Inverting Large-Signal Frequency Response

7.8 Typical Characteristics (±15 V) (continued)

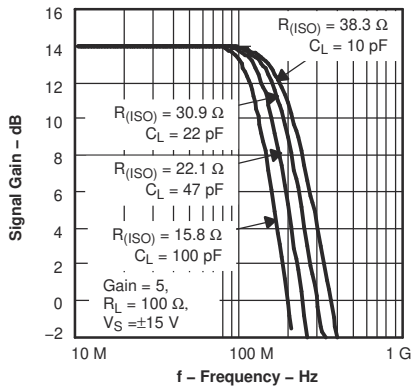


Figure 7-7. Capacitive Load Frequency Response

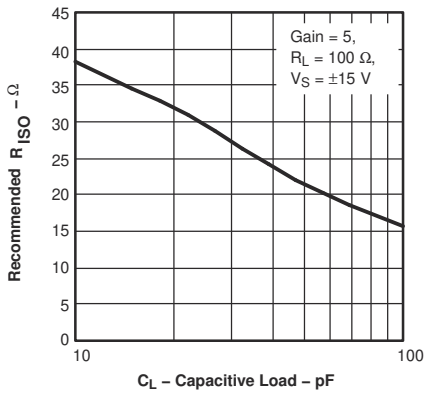


Figure 7-8. Recommended R_{ISO} vs Capacitive Load

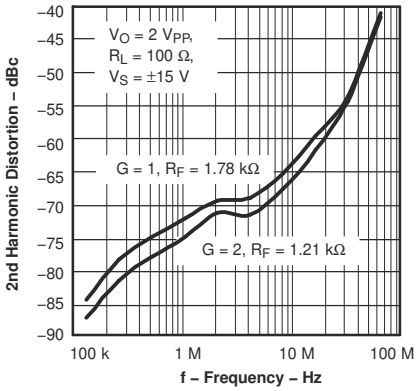


Figure 7-9. 2nd Harmonic Distortion vs Frequency

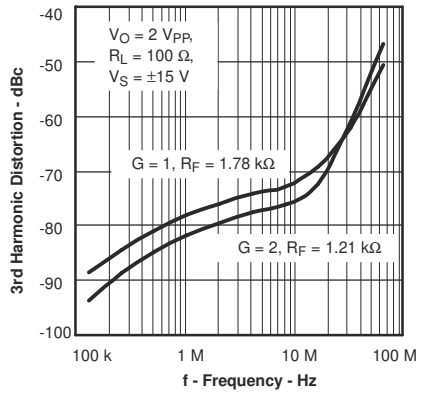


Figure 7-10. 3rd Harmonic Distortion vs Frequency

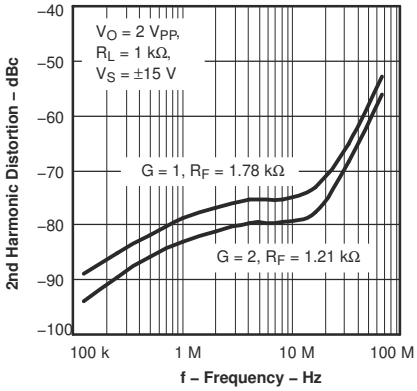


Figure 7-11. 2nd Harmonic Distortion vs Frequency

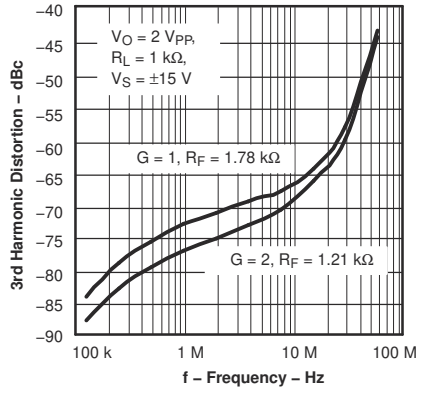


Figure 7-12. 3rd Harmonic Distortion vs Frequency

7.8 Typical Characteristics (±15 V) (continued)

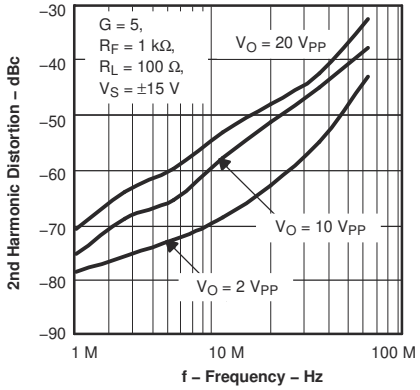


Figure 7-13. 2nd Harmonic Distortion vs Frequency

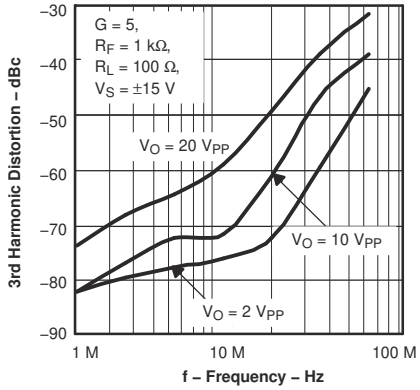


Figure 7-14. 3rd Harmonic Distortion vs Frequency

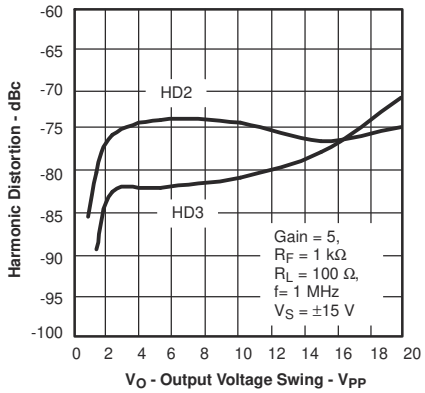


Figure 7-15. Harmonic Distortion vs Output Voltage Swing

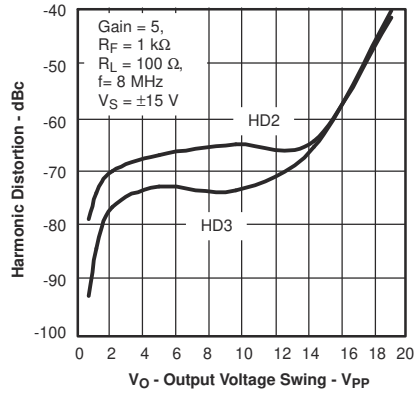


Figure 7-16. Harmonic Distortion vs Output Voltage Swing

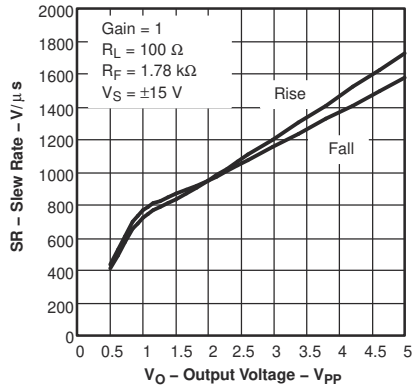


Figure 7-17. Slew Rate vs Output Voltage Step

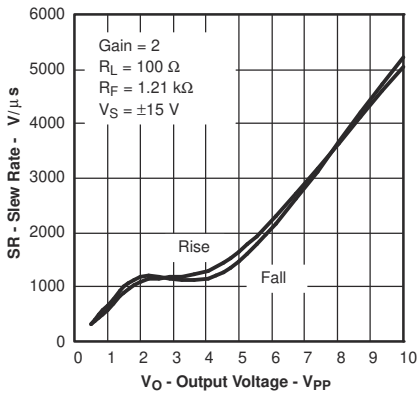


Figure 7-18. Slew Rate vs Output Voltage Step

7.8 Typical Characteristics (±15 V) (continued)

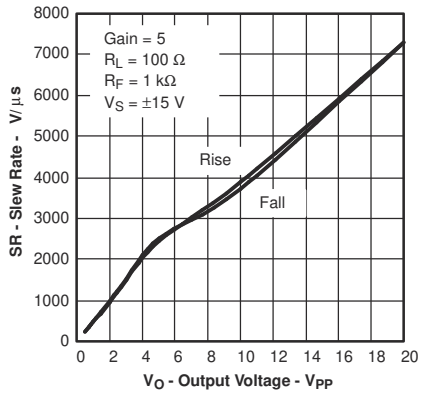


Figure 7-19. Slew Rate vs Output Voltage Step

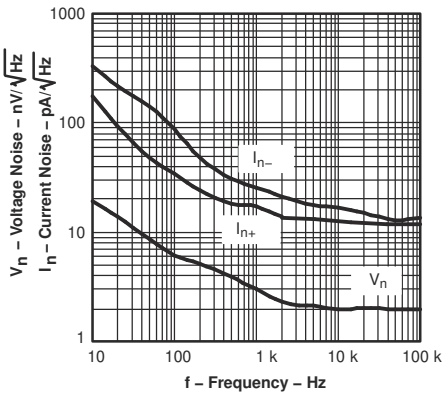


Figure 7-20. Noise vs Frequency

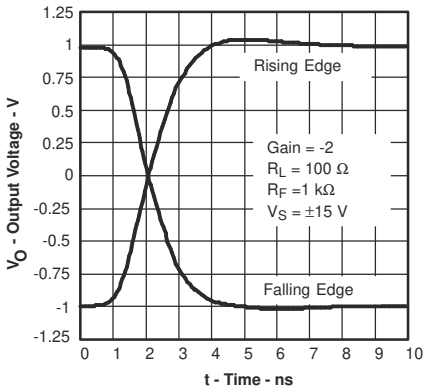


Figure 7-21. Settling Time

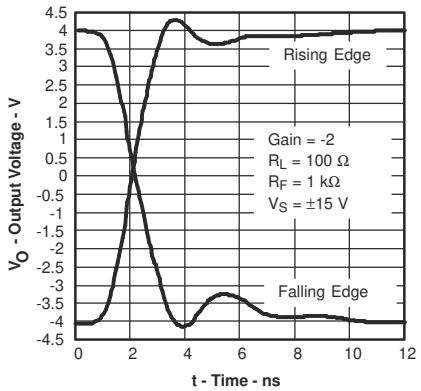


Figure 7-22. Settling Time

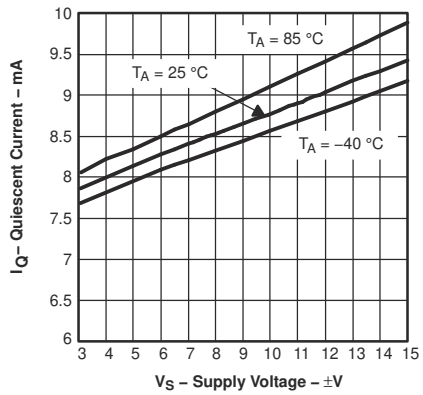


Figure 7-23. Quiescent Current vs Supply Voltage

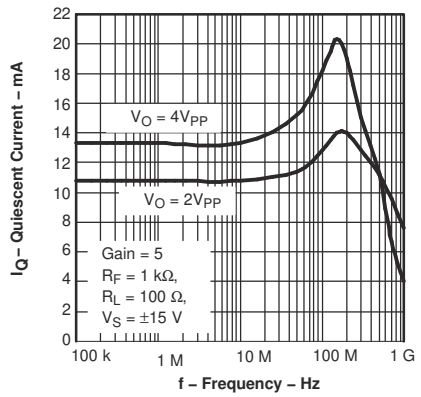


Figure 7-24. Quiescent Current vs Frequency

7.8 Typical Characteristics (±15 V) (continued)

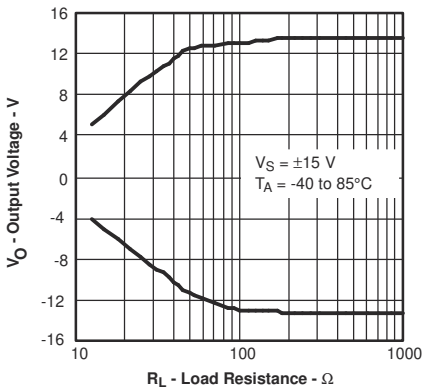


Figure 7-25. Output Voltage vs Load Resistance

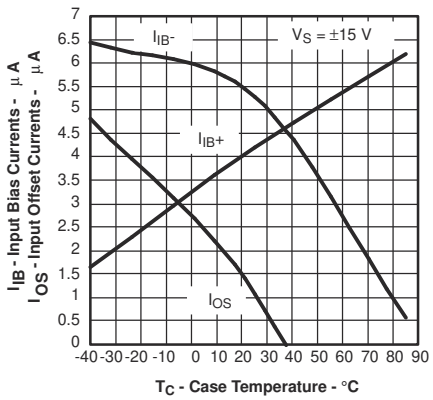


Figure 7-26. Input Bias and Offset Current vs Case Temperature

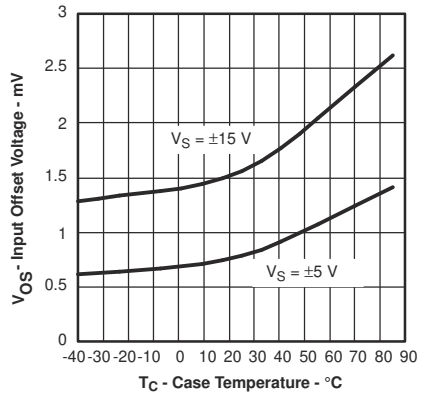


Figure 7-27. Input Offset Voltage vs Case Temperature

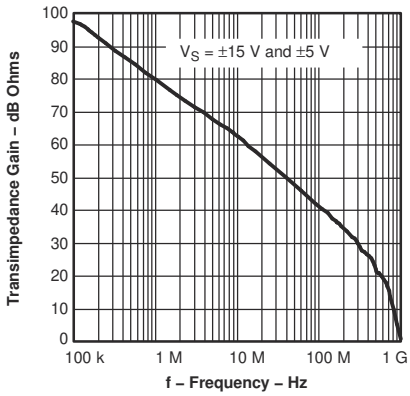


Figure 7-28. Transimpedance vs Frequency

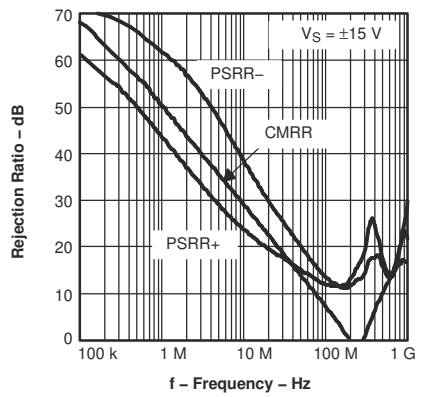


Figure 7-29. Rejection Ratio vs Frequency

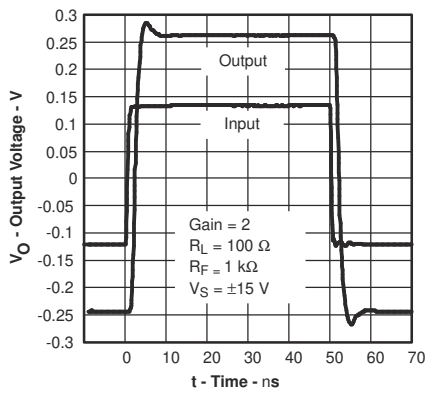


Figure 7-30. Noninverting Small-Signal Transient Response

7.8 Typical Characteristics (±15 V) (continued)

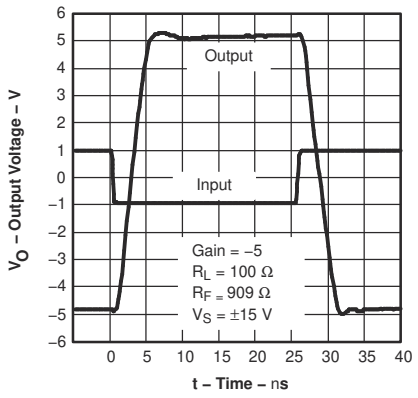


Figure 7-31. Inverting Large-Signal Transient Response

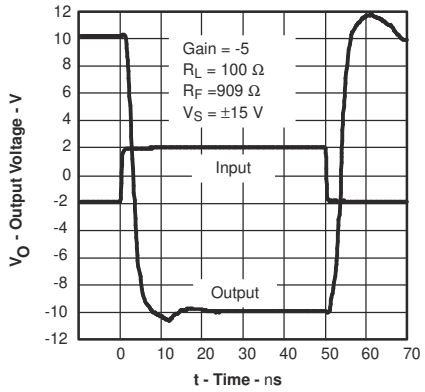


Figure 7-32. Inverting Large-Signal Transient Response

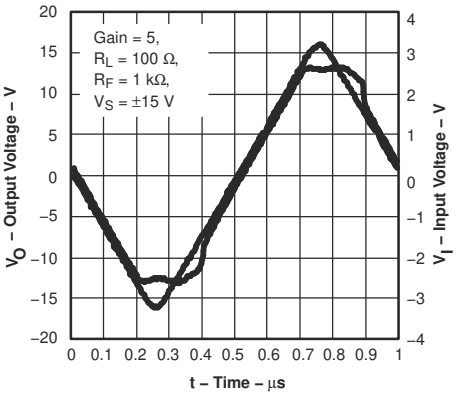


Figure 7-33. Overdrive Recovery Time

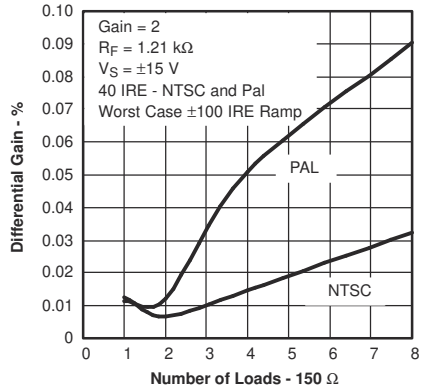


Figure 7-34. Differential Gain vs Number of Loads

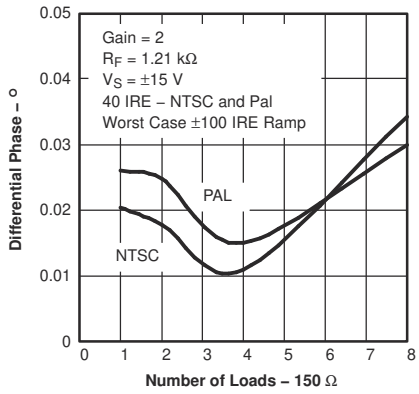


Figure 7-35. Differential Phase vs Number of Loads

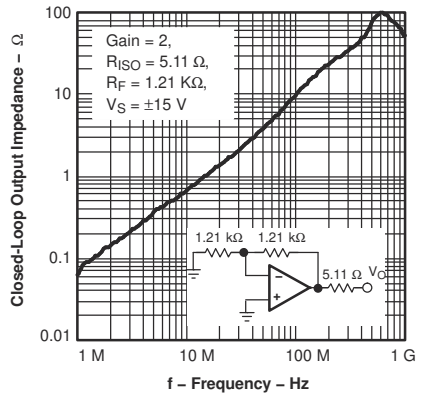


Figure 7-36. Closed-Loop Output Impedance vs Frequency

7.8 Typical Characteristics (±15 V) (continued)

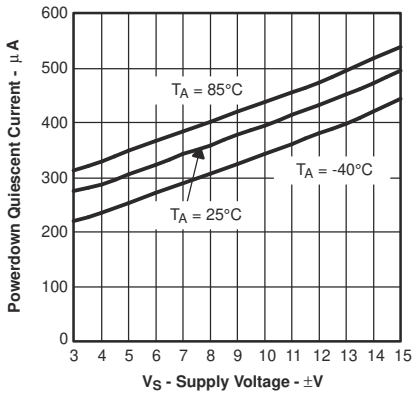


Figure 7-37. Power-Down Quiescent Current vs Supply Voltage

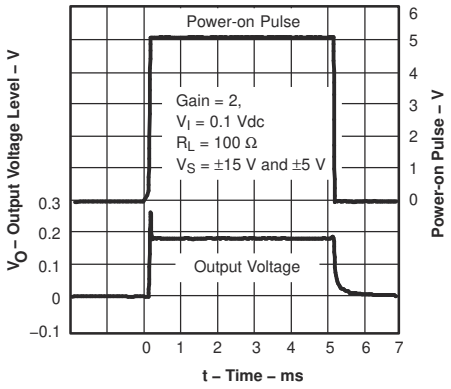


Figure 7-38. Turnon and Turnoff Time Delay

7.9 Typical Characteristics (±5 V)

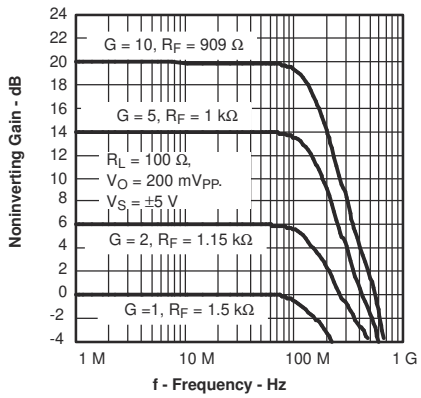


Figure 7-39. Noninverting Small-Signal Frequency Response

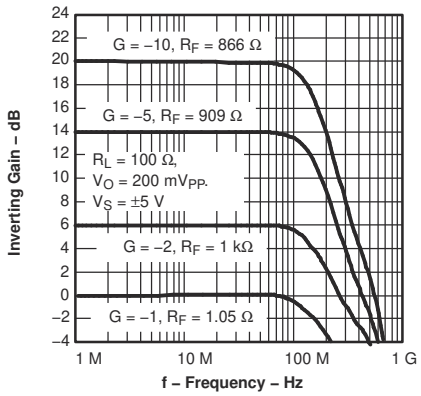


Figure 7-40. Inverting Small-Signal Frequency Response

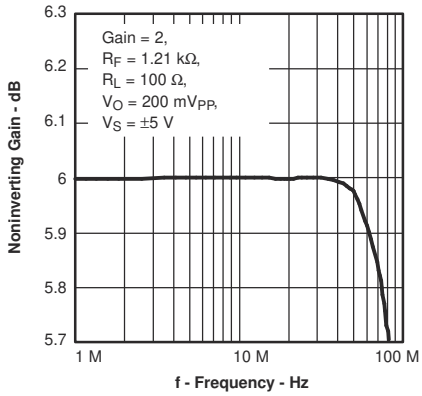


Figure 7-41. 0.1-db Gain Flatness Frequency Response

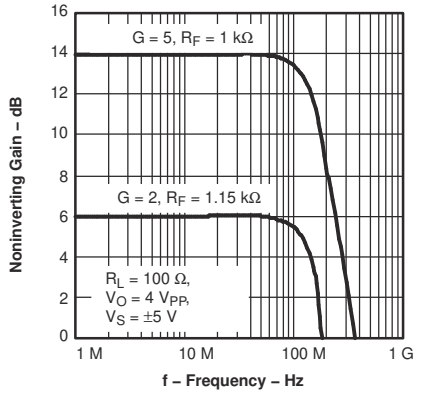


Figure 7-42. Noninverting Large-Signal Frequency Response

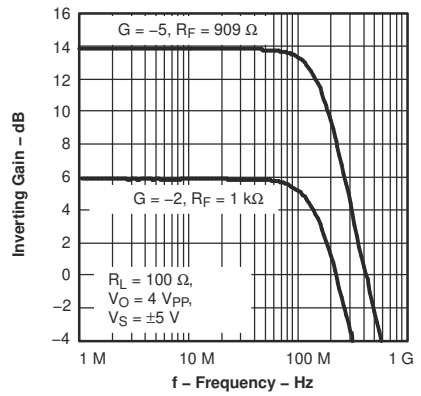


Figure 7-43. Inverting Large-Signal Frequency Response

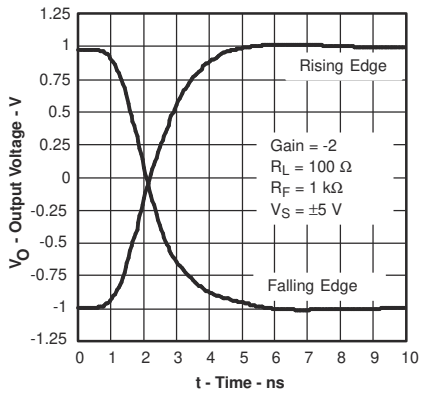


Figure 7-44. Settling Time

7.9 Typical Characteristics (±5 V) (continued)

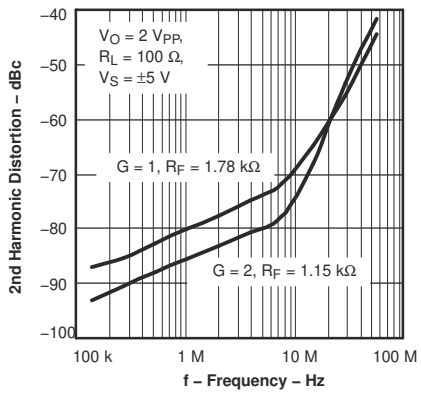


Figure 7-45. 2nd Harmonic Distortion vs Frequency

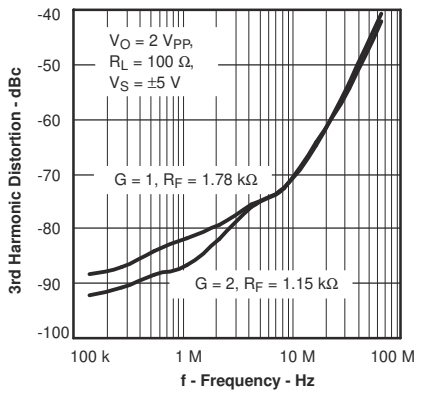


Figure 7-46. 3rd Harmonic Distortion vs Frequency

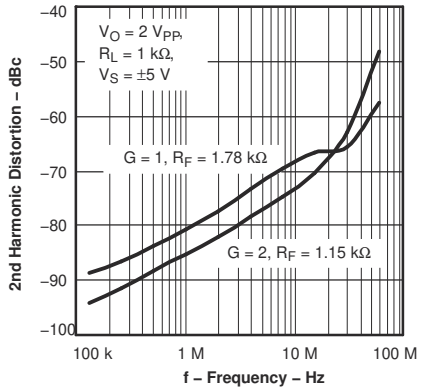


Figure 7-47. 2nd Harmonic Distortion vs Frequency

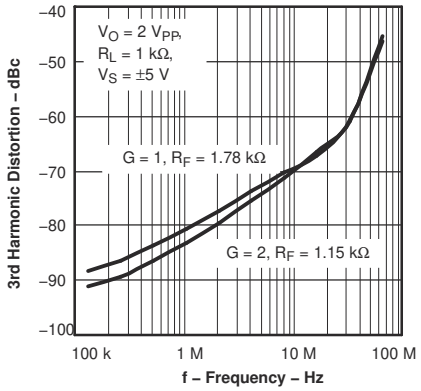


Figure 7-48. 3rd Harmonic Distortion vs Frequency

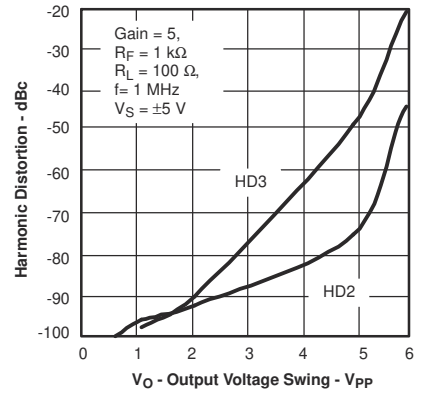


Figure 7-49. Harmonic Distortion vs Output Voltage Swing

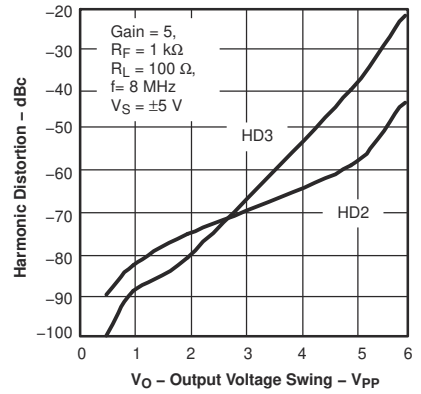


Figure 7-50. Harmonic Distortion vs Output Voltage Swing

7.9 Typical Characteristics (±5 V) (continued)

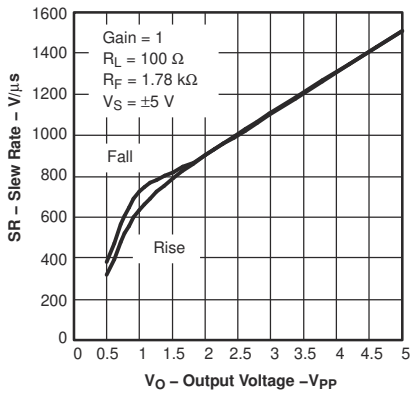


Figure 7-51. Slew Rate vs Output Voltage Step

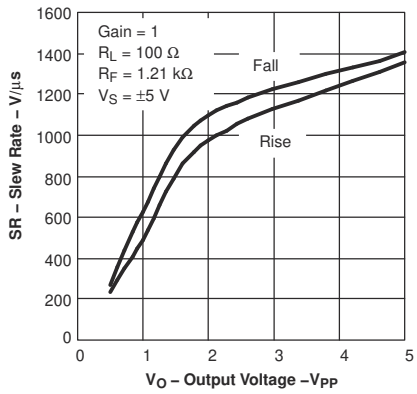


Figure 7-52. Slew Rate vs Output Voltage Step

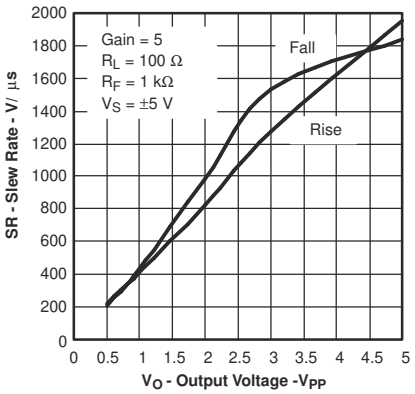


Figure 7-53. Slew Rate vs Output Voltage Step

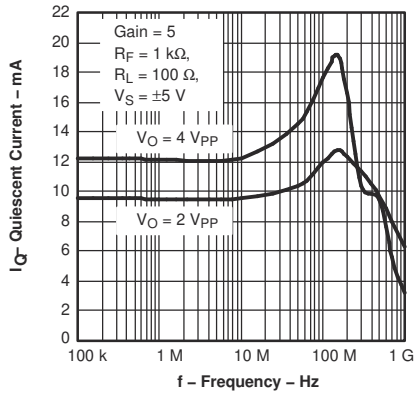


Figure 7-54. Quiescent Current vs Frequency

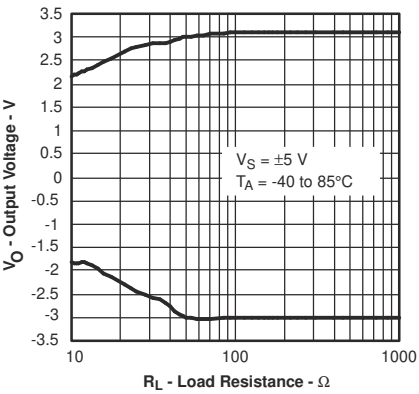


Figure 7-55. Output Voltage vs Load Resistance

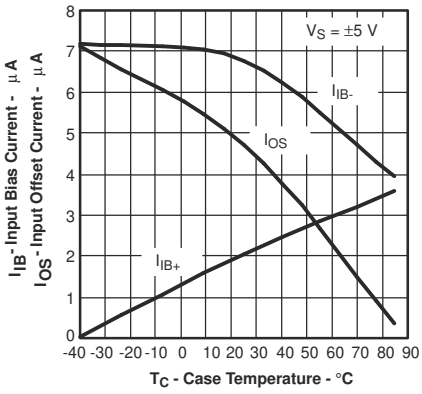


Figure 7-56. Input Bias and Offset Current vs Case Temperature

7.9 Typical Characteristics (±5 V) (continued)

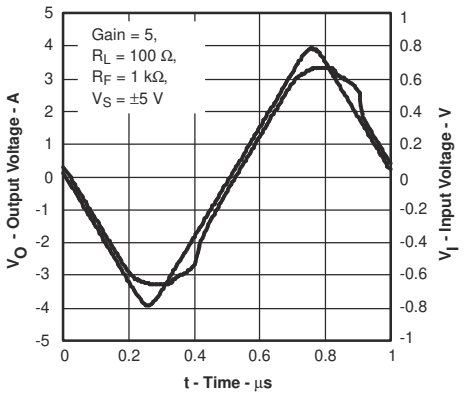


Figure 7-57. Overdrive Recovery Time

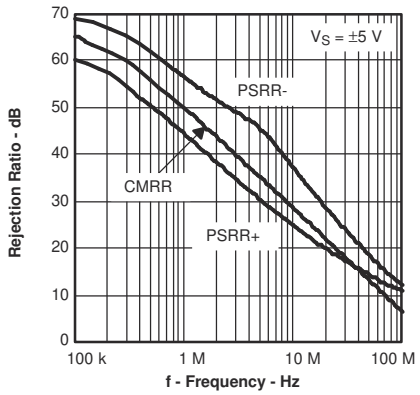


Figure 7-58. Rejection Ratio vs Frequency

8 Detailed Description

8.1 Overview

The THS3091 and THS3095 are high-voltage, low-distortion, high-speed, current feedback amplifiers designed to operate over a wide supply range of ±5 V to ±16 V for applications requiring large, linear output swings such as Arbitrary Waveform Generators.

The THS3095 features a power-down pin that puts the amplifier in low power standby mode, and lowers the quiescent current from 9.5 mA to 500 µA.

8.2 Feature Description

8.2.1 Saving Power With Power-Down Functionality and Setting Threshold Levels With the Reference Pin

The THS3095 features a power-down pin ($\overline{PD}$) which lowers the quiescent current from 9.5 mA down to 500 µA, ideal for reducing system power.

The power-down pin of the amplifier defaults to the positive supply voltage in the absence of an applied voltage, putting the amplifier in the power-on mode of operation. To turn off the amplifier in an effort to conserve power, the power-down pin can be driven towards the negative rail. For information about the threshold voltages for power on and power down are relative to the supply rails, see *Section 7.8* and *Section 7.9*. Above the enable threshold voltage, the device is on. Below the disable threshold voltage, the device is off. Behavior in between these threshold voltages is not specified.

Note that this power-down functionality is just that; the amplifier consumes less power in Power-Down mode. The Power-Down mode is not intended to provide a high-impedance output. In other words, the power-down functionality is not intended to allow use as a 3-state bus driver. When in Power-Down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain-setting resistors, but the output impedance of the device itself varies depending on the voltage applied to the outputs.

Figure 8-1 shows the total system output impedance which includes the amplifier output impedance in parallel with the feedback plus gain resistors, which cumulates to 2380 Ω. Figure 8-2 shows this circuit configuration for reference.

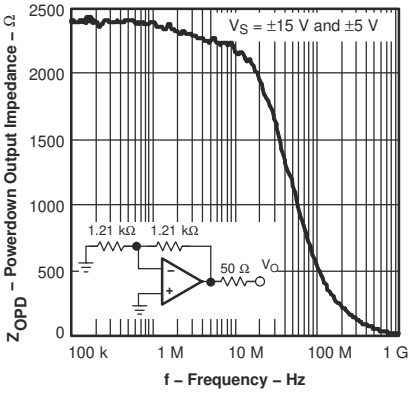


Figure 8-1. Power-Down Output Impedance vs Frequency

As with most current feedback amplifiers, the internal architecture places some limitations on the system when in Power-Down mode. Most notably is the fact that the amplifier actually turns *ON* if there is a ±0.7 V or greater difference between the two input nodes (V+ and V–) of the amplifier. If this difference exceeds ±0.7 V, then the output of the amplifier creates an output voltage equal to approximately [(V+ – V–) –0.7 V] × Gain. This also implies that if a voltage is applied to the output while in Power-Down mode, the V– node voltage is equal to $V_{O(applied)} \times R_G/(R_F + R_G)$. For low gain configurations and a large applied voltage at the output, the amplifier may actually turn *ON* due to the aforementioned behavior.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach either 10% or 90% of the final output voltage. The time delays are in the order of microseconds because the amplifier moves in and out of the linear mode of operation in these transitions.

8.2.2 Power-Down Reference Pin Operation

In addition to the power-down pin, the THS3095 features a reference pin (REF) which allows the user to control the enable or disable power-down voltage levels applied to the $\overline{PD}$ pin. In most split-supply applications, the reference pin is connected to ground. In either case, the user needs to be aware of voltage-level thresholds that apply to the power-down pin. The following tables provide examples and illustrate the relationship between the reference voltage and the power-down thresholds. In the table, the threshold levels are derived by the following equations:

$$\overline{PD} \leq \text{REF} + 0.8\ \text{V for disable} \quad (1)$$

$$\overline{PD} \geq \text{REF} + 2.0\ \text{V for enable} \quad (2)$$

where the usable range at the REF pin is:

$$V_{S-} \leq V_{REF} \leq (V_{S+} - 4\ \text{V}) \quad (3)$$

The recommended mode of operation is to tie the REF pin to midrail, thus setting the enable or disable thresholds to $V_{midrail}$ + 2 V and $V_{midrail}$ + 0.8 V respectively.

Table 8-1. Power-Down Threshold Voltage Levels

SUPPLY VOLTAGE (V)	REFERENCE PIN VOLTAGE (V)	ENABLE LEVEL (V)	DISABLE LEVEL (V)
±15, ±5	0	2	0.8
±15	2	4	2.8
±15	–2	0	–1.2
±5	1	3	1.8
±5	–1	1	–0.2
30	15	17	15.8
10	5	7	5.8

Note that if the REF pin is left unterminated, it will float to the positive rail and will fall outside of the recommended operating range shown in Equation 3 ($V_{S-} \leq$ VREF $\leq V_{S+} - 4$ V). As a result, it will no longer serve as a reliable reference for the $\overline{PD}$ pin and the enable or disable thresholds provided in Table 8-1 will no longer apply. If the $\overline{PD}$ pin is also left unterminated, it will also float to the positive rail and the device will be enabled. If balanced, split supplies are used (±Vs) and the REF and $\overline{PD}$ pins are grounded, the device will be disabled.

8.3 Device Functional Modes

8.3.1 Wideband, Noninverting Operation

The THS309x are unity gain stable 235-MHz current-feedback operational amplifiers, designed to operate from a ±5-V to ±15-V power supply.

Figure 8-2 shows the THS3091 in a noninverting gain of 2-V/V configuration typically used to generate the performance curves. Most of the curves were characterized using signal sources with 50-Ω source impedance, and with measurement equipment presenting a 50-Ω load impedance.

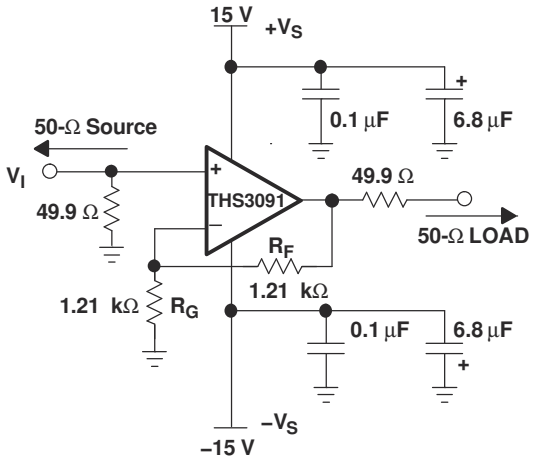


Figure 8-2. Wideband, Noninverting Gain Configuration

Current-feedback amplifiers are highly dependent on the feedback resistor R_F for maximum performance and stability. Table 8-2 shows the optimal gain-setting resistors R_F and R_G at different gains to give maximum bandwidth with minimal peaking in the frequency response. Higher bandwidths can be achieved, at the expense of added peaking in the frequency response, by using even lower values for R_F. Conversely, increasing R_F decreases the bandwidth, but stability is improved.

Table 8-2. Recommended Resistor Values for Optimum Frequency Response

THS3091 and THS3095 R_F and R_G values for minimal peaking with R_L = 100 Ω			
GAIN (V/V)	SUPPLY VOLTAGE (V)	R_G (Ω)	R_F (Ω)
1	±15	—	1.78 k
	±5	—	1.78 k
2	±15	1.21 k	1.21 k
	±5	1.15 k	1.15 k
5	±15	249	1 k
	±5	249	1 k
10	±15	95.3	866
	±5	95.3	866
–1	±15 and ±5	1.05 k	1.05 k
–2	±15 and ±5	499	1 k
–5	±15 and ±5	182	909
–10	±15 and ±5	86.6	866

8.3.2 Wideband, Inverting Operation

Figure 8-3 shows the THS3091 in a typical inverting gain configuration where the input and output impedances and signal gain from Figure 8-2 are retained in an inverting circuit configuration.

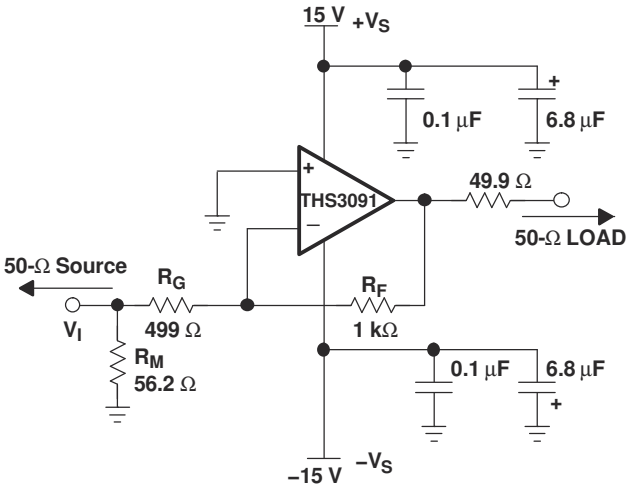


Figure 8-3. Wideband, Inverting Gain Configuration

8.3.3 Single-Supply Operation

The THS309x have the capability to operate from a single-supply voltage ranging from 10 V to 30 V. When operating from a single power supply, biasing the input and output at mid-supply allows for the maximum output voltage swing. The circuits shown in Figure 8-4 show inverting and noninverting amplifiers configured for single-supply operations.

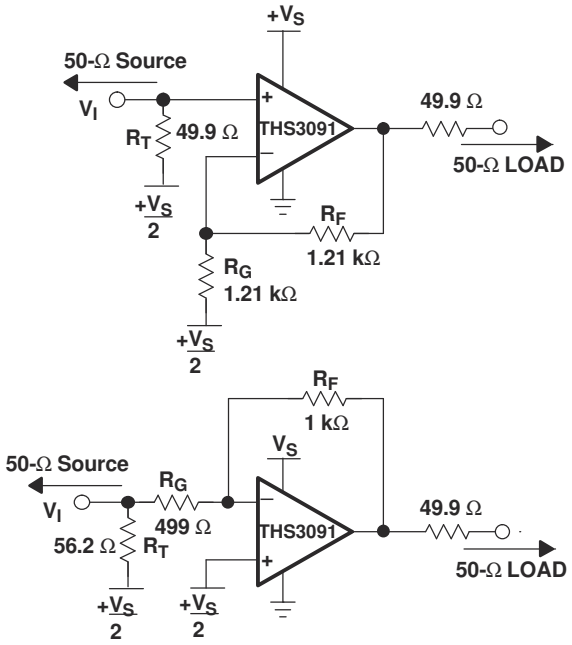


Figure 8-4. DC-Coupled, Single-Supply Operation

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Video Distribution

The wide bandwidth, high slew rate, and high output drive current of the THS309x matches the demands for video distribution for delivering video signals down multiple cables. To ensure high signal quality with minimal degradation of performance, a 0.1-dB gain flatness should be at least 7x the passband frequency to minimize group delay variations from the amplifier. A high slew rate minimizes distortion of the video signal, and supports component video and RGB video signals that require fast transition times and fast settling times for high signal quality.

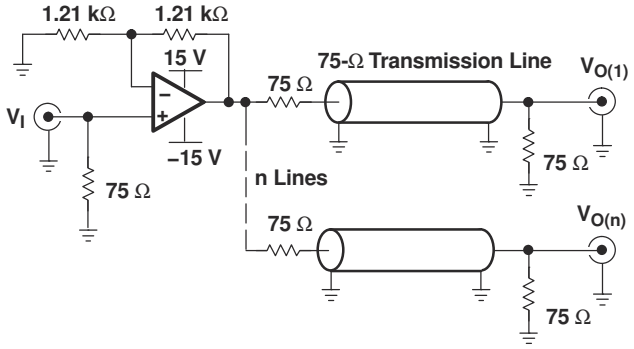


Figure 9-1. Video Distribution Amplifier Application

9.1.2 Driving Capacitive Loads

Applications such as FET line drivers can be highly capacitive and cause stability problems for high-speed amplifiers.

Figure 9-2 through Figure 9-7 show recommended methods for driving capacitive loads. The basic idea is to use a resistor or ferrite chip to isolate the phase shift at high frequency caused by the capacitive load from the amplifier's feedback path. For recommended resistor values versus capacitive load, see *Effect of Parasitic Capacitance in Op Amp Circuits* application note.

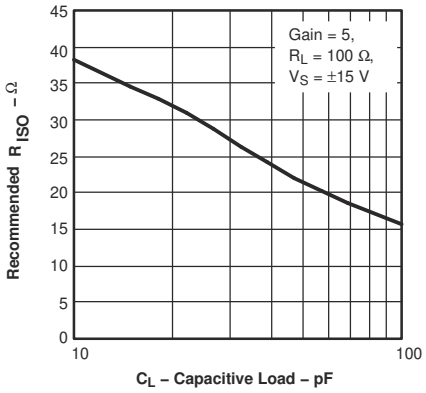


Figure 9-2. Recommended R_{ISO} vs Capacitive Load

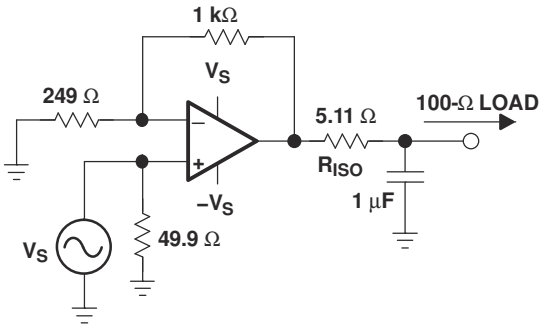


Figure 9-3. Driving a Large Capacitive Load Using an Output Series Isolation Resistor

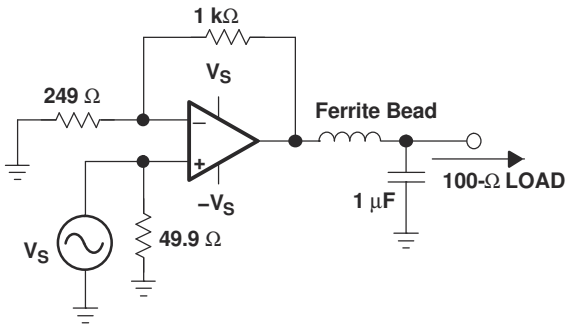


Figure 9-4. Driving a Large Capacitive Load Using an Output Series Ferrite Bead

As shown in Figure 9-3, placing a small series resistor, R_{ISO}, between the amplifier's output and the capacitive load is an easy way of isolating the load capacitance.

As shown in Figure 9-4 using a ferrite chip in place of R_{ISO} is another approach of isolating the output of the amplifier. The ferrite's impedance characteristic versus frequency is useful to maintain the low-frequency load independence of the amplifier while isolating the phase shift caused by the capacitance at high frequency. Use a ferrite with similar impedance to R_{ISO}, 20 Ω to 50 Ω, at 100 MHz and low-impedance at DC.

Figure 9-5 shows another method used to maintain the low-frequency load independence of the amplifier while isolating the phase shift caused by the capacitance at high frequency. At low frequency, feedback is mainly from the load side of R_{ISO}. At high frequency, the feedback is mainly via the 27-pF capacitor. The resistor R_{IN} in series with the negative input is used to stabilize the amplifier and should be equal to the recommended value of R_F at unity gain. As shown in Figure 9-6, replacing R_{IN} with a ferrite of similar impedance at about 100 MHz gives similar results with reduced DC offset and low-frequency noise (for more information, see *Expanding the Usability of Current-Feedback Amplifiers* analog journal).

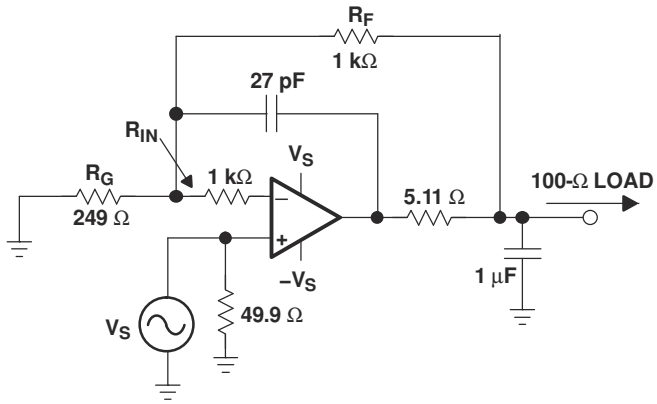


Figure 9-5. Driving a Large Capacitive Load Using a Multiple Feedback Loop With Stabilizing Input Resistor (R_{IN})

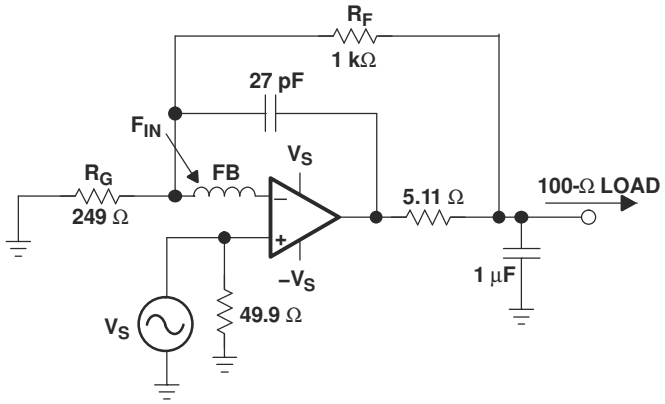


Figure 9-6. Driving a Large Capacitive Load Using a Multiple Feedback Loop With Stabilizing Input Ferrite Bead (F_{IN})

Figure 9-7 is shown using two amplifiers in parallel to double the output drive current to larger capacitive loads. This technique is used when more output current is needed to charge and discharge the load faster like when driving large FET transistors.

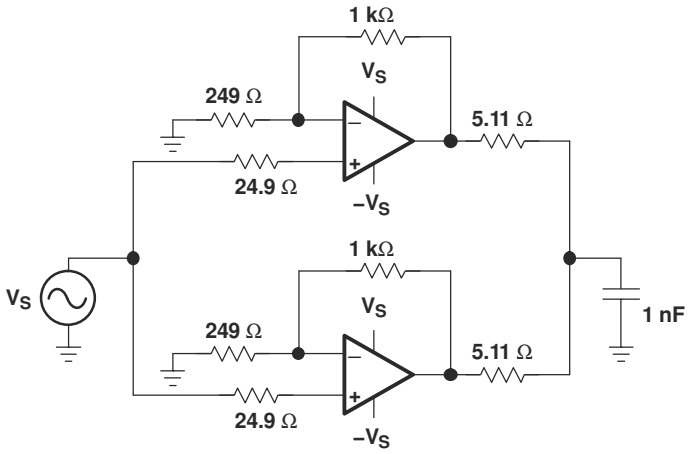


Figure 9-7. Driving a Large Capacitive Load Using 2 Parallel Amplifier Channels

Figure 9-8 shows a push-pull FET driver circuit typical of ultrasound applications with isolation resistors to isolate the gate capacitance from the amplifier.

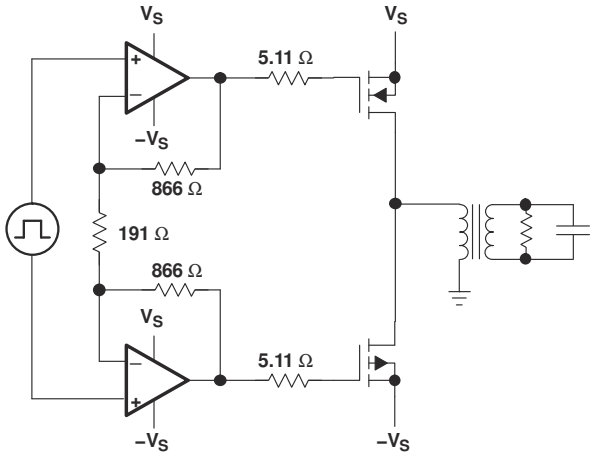


Figure 9-8. PowerFET Drive Circuit

9.2 Typical Application

The fundamental concept of load sharing is to drive a load using two or more of the same operational amplifiers. Each amplifier is driven by the same source. Figure 9-9 shows two THS3091 amplifiers sharing the same load. This concept effectively reduces the curernt load of each amplifier by 1/N, where N is the number of amplifiers.

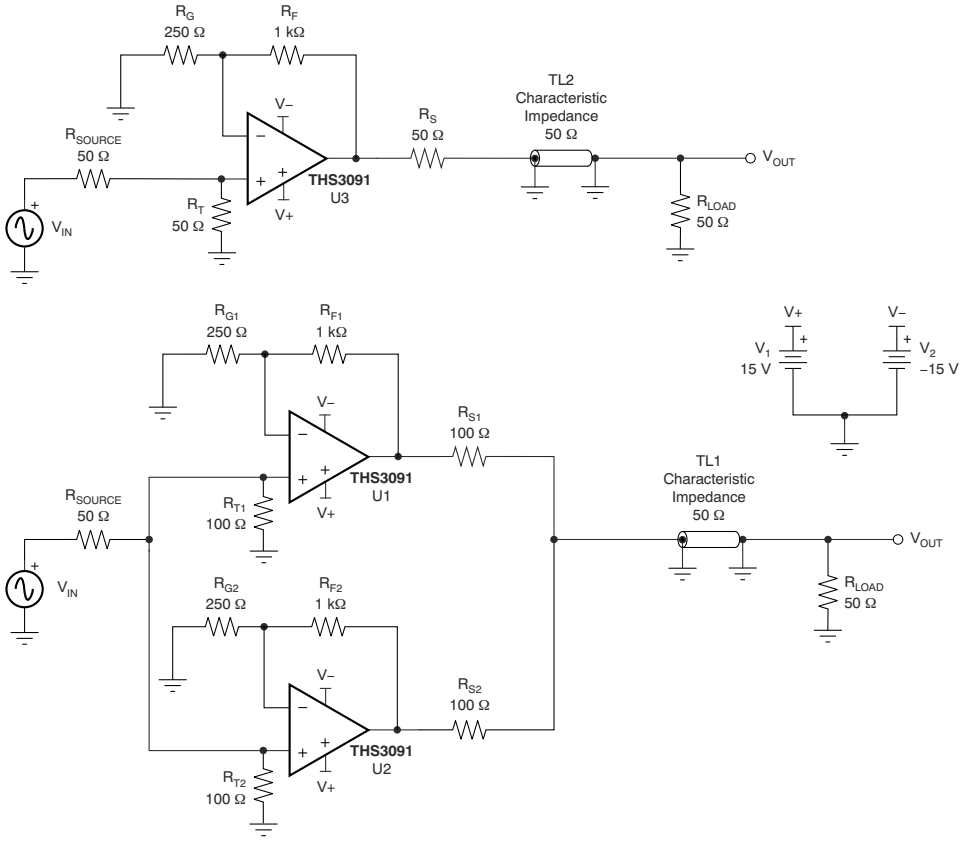


Figure 9-9. Reference THS3091 and THS3091 Load Sharing Test Configurations

9.2.1 Design Requirements

Use two THS3091 amplifiers in a parallel load-sharing circuit to improve distortion performance.

Table 9-1. Design Parameters

DESIGN PARAMETER	VALUE
V_{OPP}	20 V
R_{LOAD}	100 Ω

9.2.2 Detailed Design Procedure

In addition to providing higher output current drive to the load, the load sharing configuration can also provide improved distortion performance. In many cases, an operational amplifier shows better distortion performance as the load current decreases (that is, for higher resistive loads) until the feedback resistor starts to dominate the current load. In a load sharing configuration of N amplifiers in parallel, the equivalent current load that each amplifier drives is 1/N times the total load current.

As shown in Figure 9-9 for example, in a two-amplifier load sharing configuration with matching resistance driving a resistive load (RL), each series resistance is 2*RL and each amplifier drives 2*RL. A convenient indicator of whether an op amp will function well in a load sharing configuration is the characteristic performance graph of harmonic distortion versus load resistance. Such graphs can be found in most of TI's high-speed amplifier data sheets. These graphs can be used to obtain a general sense of whether or not an amplifier will show improved distortion performance in load sharing configurations.

Figure 9-9 shows two test circuits: one for a single THS3091 amplifier driving a double-terminated (50-Ω cable), and one with two THS3091 amplifiers in a load sharing configuration. In the load sharing configuration, the two 100-Ω series output resistors act in parallel to provide 50-Ω back-matching to the 50-Ω cable.

Figure 9-10 and Figure 9-11 show the 32-MHz, 18-VPP sine wave output amplitudes for the single THS3091 configuration and the load sharing configuration, respectively, measured using an oscilloscope. An ideal sine wave is also included as a visual reference (the dashed red line). Figure 72 shows visible distortion in the single THS3091 output. In the load sharing configuration of Figure 73, however, no obvious degradation is visible.

Figure 9-12 and Figure 9-13 show the 64-MHz sine wave outputs of the two configurations from Figure 8. While the single THS3091 output is clearly distorted in Figure 74, the output of the load sharing configuration in Figure 75 shows only minor deviations from the ideal sine wave.

The improved output waveform as a result of load sharing is quantified in the harmonic distortion versus frequency graphs shown in Figure 9-14 and Figure 9-15 for the single amplifier and load sharing configurations, respectively. While second-harmonic distortion remains largely the same between the single and load sharing cases, third-harmonic distortion is improved by approximately 8 dB in the frequency range between 20 MHz to 64 MHz.

Table 9-2. Bill of Materials

THS3091DDA and THS3095DDA EVM(1)						
ITEM	DESCRIPTION	SMD SIZE	REFERENCE DESIGNATOR	PCB QTY	MANUFACTURER'S PART NUMBER	DISTRIBUTOR'S PART NUMBER
1	Bead, Ferrite, 3 A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R-00	(Digi-Key) 240-1010-1-ND
2	Cap, 6.8 µF, Tantalum, 50 V, 10%	D	C3, C6	2	(AVX) TAJD685K050R	(Garrett) TAJD685K050R
3	Cap, 0.1 µF, ceramic, X7R, 50 V	0805	C9, C10	2(2)	(AVX) 08055C104KAT2A	(Garrett) 08055C104KAT2A
4	Cap, 0.1 µF, ceramic, X7R, 50 V	0805	C4, C7	2	(AVX) 08055C104KAT2A	(Garrett) 08055C104KAT2A
5	Resistor, 0 Ω, 1/8 W, 1%	0805	R9	1(2)	(KOA) RK73Z2ALTD	(Garrett) RK73Z2ALTD
6	Resistor, 249 Ω, 1/8 W, 1%	0805	R3	1	(KOA) RK73H2ALTD2490F	(Garrett) RK73H2ALTD2490F
7	Resistor, 1 kΩ, 1/8 W, 1%	0805	R4	1	(KOA) RK73H2ALTD1001F	(Garrett) RK73H2ALTD1001F
8	Open	1206	R8	1		
9	Resistor, 0 Ω, 1/4 W, 1%	1206	R1	1	(KOA) RK73Z2BLTD	(Garrett) RK73Z2BLTD
10	Resistor, 49.9 Ω, 1/4 W, 1%	1206	R2, R7	2	(KOA) RK73Z2BLTD49R9F	(Garrett) RK73Z2BLTD49R9F
11	Open	2512	R5, R6	2		
12	Header, 0.1-inch (2,54 mm) centers, 0.025-inch (6,35 mm) square pins		JP1, JP2	2 (2)	(Sullins) PZC36SAAN	(Digi-Key) S1011-36-ND
13	Connector, SMA PCB Jack		J1, J2, J3	3	(Amphenol) 901-144-8RFX	(Newark) 01F2208
14	Jack, banana receptacle, 0.25-inch (6,35 mm) dia. hole		J4, J5, J6	3	(SPC) 813	(Newark) 39N867
15	Test point, black		TP1, TP2	2	(Keystone) 5001	(Digi-Key) 5001K-ND
16	Standoff, 4-40 hex, 0.625-inch (15,9 mm) length			4	(Keystone) 1808	(Newark) 89F1934
17	Screw, Phillips, 4-40, 0.25-inch (6,35 mm)			4	SHR-0440-016-SN	
18	IC, THS3091(3) IC, THS3095(2)		U1	1	(TI) THS3091DDA(3) (TI) THS3095DDA(2)	
19	Board, printed-circuit			1	(TI) EDGE # 6446289 Rev. A(3) (TI) EDGE # 6446290 Rev. A(2)	

(1) All items are designated for both the THS3091DDA and THS3095 EVMs unless otherwise noted.
(2) THS3095 EVM only.
(3) THS3091 EVM only.

9.2.3 Application Curves

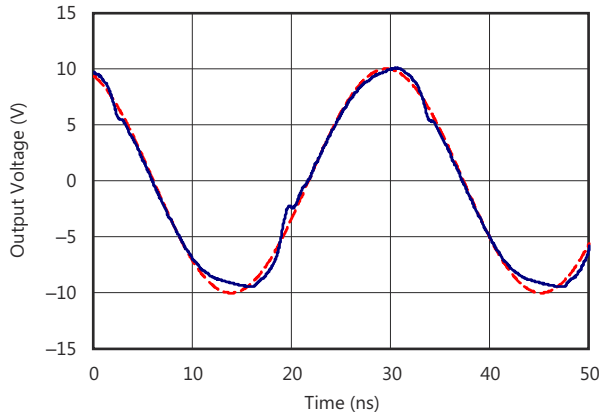


Figure 9-10. 32-MHz Sine Wave Output (Gain = 5 V/V, Signal Amplitude Referred to Amplifier Output), Single THS3091 Circuit Configuration

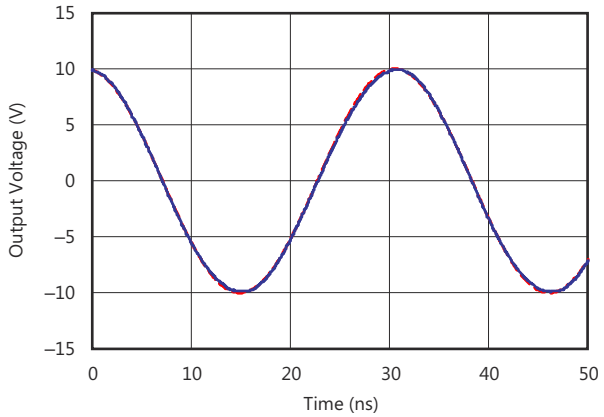


Figure 9-11. 32-MHz Sine Wave Output (Gain = 5 V/V, Signal Amplitude Referred to Amplifier Output), Two THS3091 Amplifiers in Load Sharing Configuration

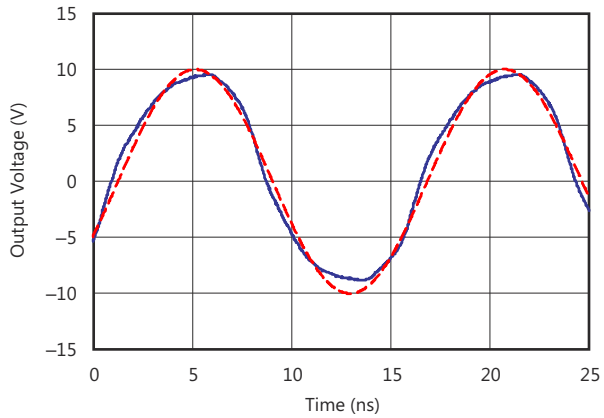


Figure 9-12. 64-MHz Sine Wave Output (Gain = 5 V/V, Signal Amplitude Referred to Amplifier Output), Single THS3091 Circuit Configuration

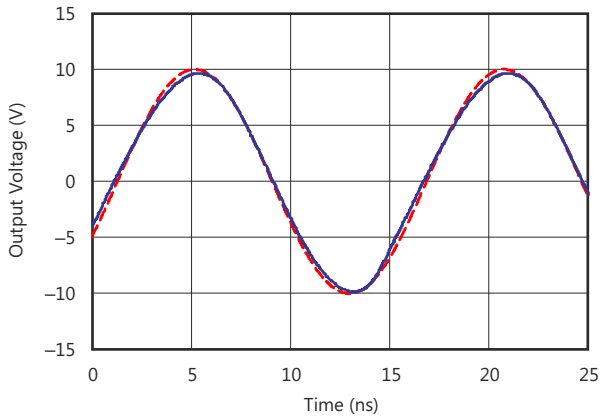


Figure 9-13. 64-MHz Sine Wave Output (Gain = 5 V/V, Signal Amplitude Referred to Amplifier Output), Two THS3091 Amplifiers in Load Sharing Configuration

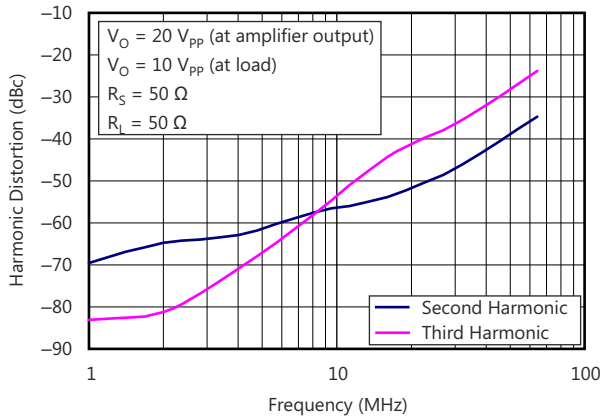


Figure 9-14. Harmonic Distortion vs Frequency, Single THS3091 Circuit Configuration

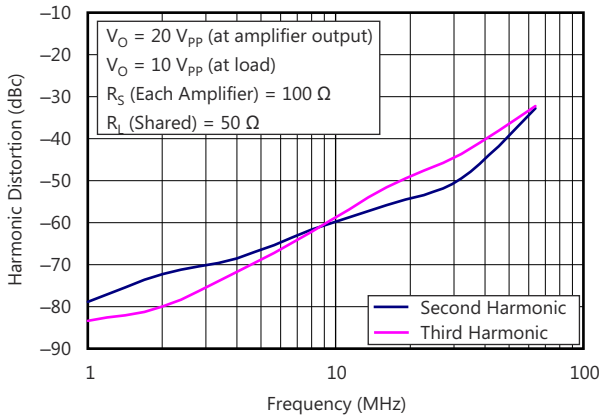


Figure 9-15. Harmonic Distortion vs Frequency, Two THS3091 Amplifiers in Load Sharing Configuration

10 Power Supply Recommendations

The THS3091 can operate off a single supply or with dual supplies as long as the input CM voltage range (CMIR) has the required headroom to either supply rail. Operating from a single supply can have numerous advantages. With the negative supply at ground, the DC errors due to the –PSRR term can be minimized. Supplies should be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. The use of ground plane is recommended, and as in most high speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs. An optional supply decoupling capacitor across the two power supplies (for split supply operation) improves second harmonic distortion performance.

11 Layout

11.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier, like the THS309x, requires careful attention to board layout parasitic and external component types.

Recommendations that optimize performance include the following:

- Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- Minimize the distance [< 0.25 inch (6.35 mm)] from the power supply pins to high-frequency 0.1-µF and 100-pF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (6.8 µF or more) tantalum decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.
- Careful selection and placement of external components preserve the high-frequency performance of the THS309x. Resistors should be a low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Again, keep their leads and PC board trace length as short as possible. Never use wire-bound type resistors in a high-frequency application. Because the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Other network components, such as input termination resistors, should be placed close to the gain-setting resistors. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 2 kΩ, this parasitic capacitance can add a pole or a zero (or both) that can effect circuit operation. Keep resistor values as low as possible, consistent with load-driving considerations.
- Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces [0.05 inch (1.3 mm) to 0.1 inch (2.54 mm)] should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low parasitic capacitive loads (< 4 pF) may not need an R_S because the THS309x are nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an RS are allowed as the signal gain increases (increasing the unloaded phase margin).

If a long trace is required, and the 6-dB signal loss intrinsic to a doubly terminated transmission line is acceptable, then implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS309x is used as well as a terminating shunt resistor at the input of the destination device. Also remember that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, then a long trace can be series- terminated at the source end only. Treat the trace as a capacitive load in this case. This does not preserve signal integrity as well as a doubly terminated line. If the input impedance of the destination device is low, then there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

- Socketing a high-speed part like the THS309x is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS309x parts directly onto the board.

11.2 Layout Example

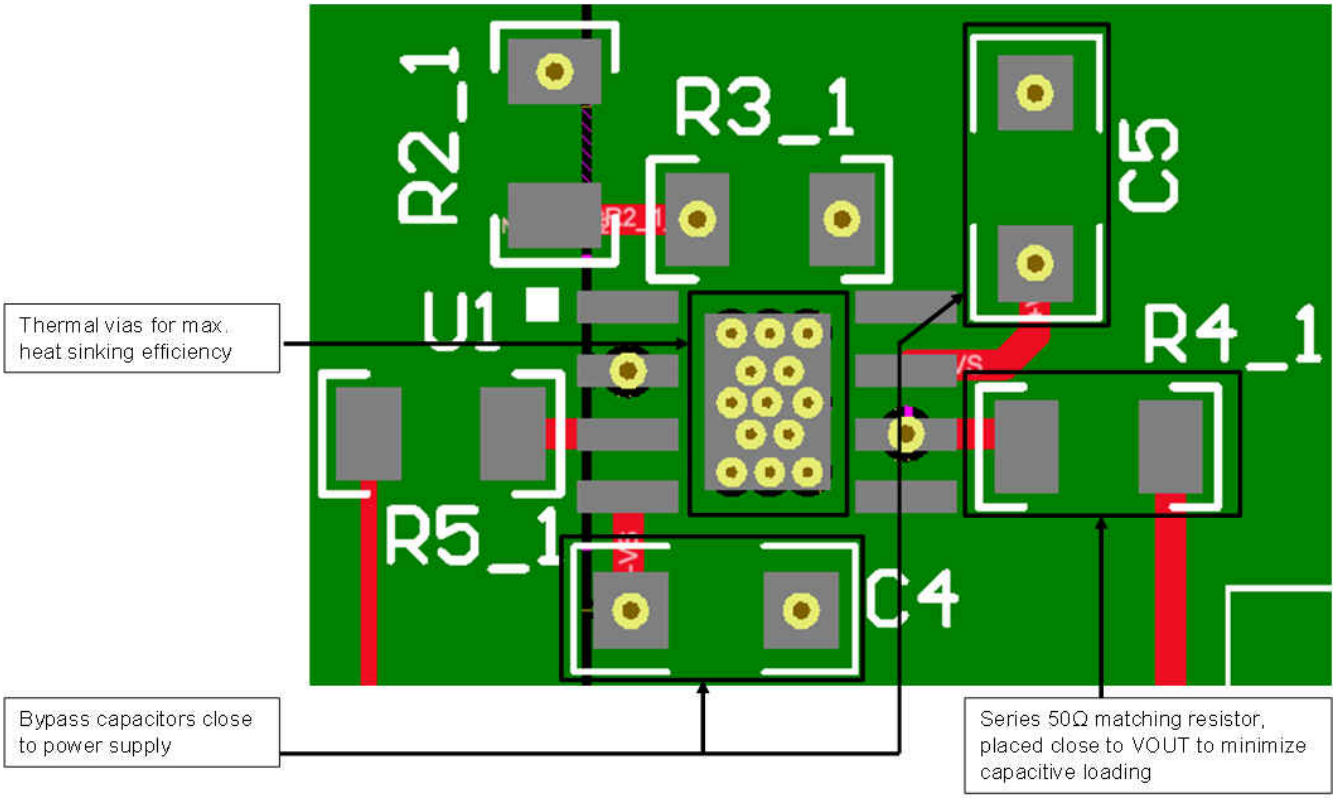


Figure 11-1. Layout Recommendation

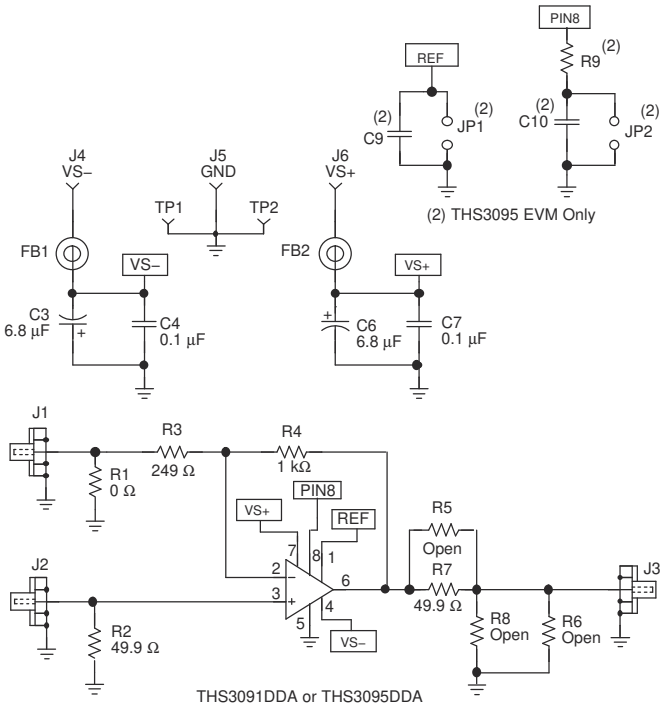


Figure 11-2. THS3091 EVM Circuit Configuration

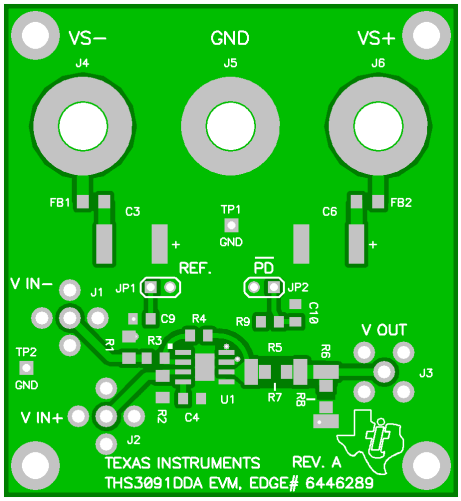


Figure 11-3. THS3091 EVM Board Layout (Top Layer)

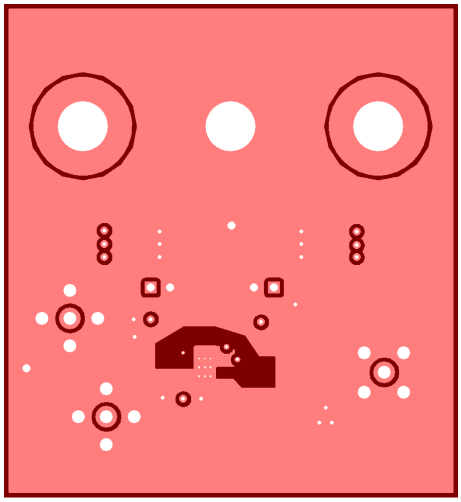


Figure 11-4. THS3091 EVM Board Layout (Second and Third Layers)

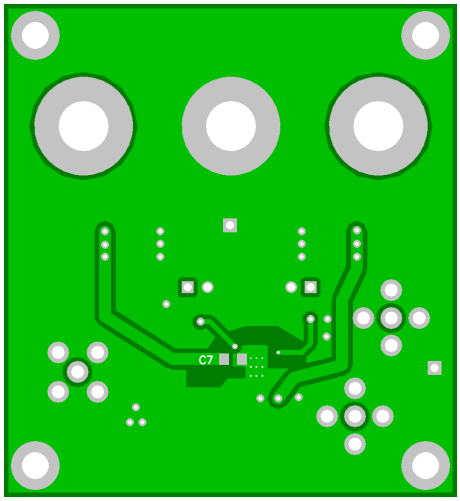


Figure 11-5. THS3091 EVM Board Layout (Bottom Layer)

11.3 PowerPAD Design Considerations

The THS309x are available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe on which the die is mounted [see Figure 11-6(a) and Figure 11-6(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 11-6(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad. Note that devices such as the THS309x have no electrical connection between the PowerPAD and the die.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the awkward mechanical methods of heatsinking.

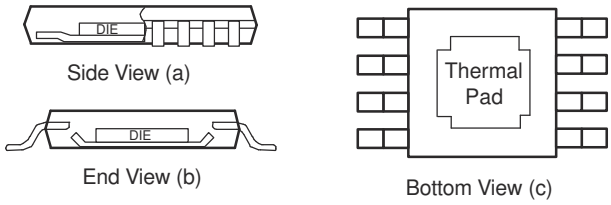


Figure 11-6. Views of Thermal Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

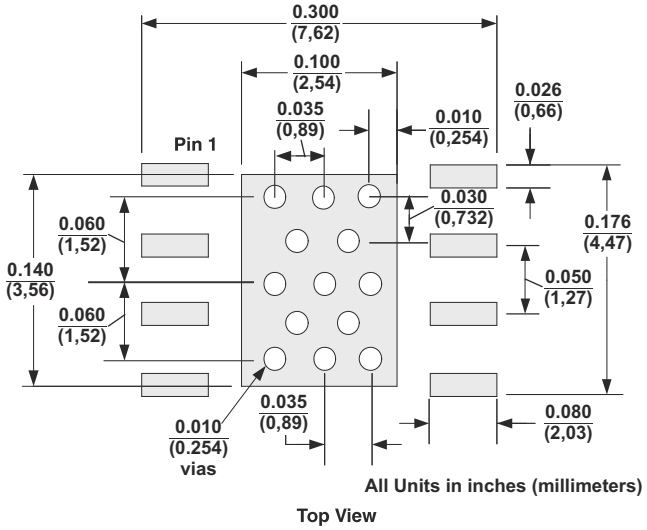


Figure 11-7. DDA PowerPAD PCB Etch and Via Pattern

11.4 PowerPAD Layout Considerations

1. PCB with a top-side etch pattern is shown in Figure 11-7. There should be etch for the leads as well as etch for the thermal pad.
2. Place 13 holes in the area of the thermal pad. These holes should be 0.01 inch (0.254 mm) in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS309x IC. These additional vias may be larger than the 0.01-inch (0.254 mm) diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane. Note that the PowerPAD is electrically isolated from the silicon and all leads. Connecting the PowerPAD to any potential voltage such as V_{S-} is acceptable as there is no electrical connection to the silicon.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS309x PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its 13 holes exposed. The bottom-side solder mask should cover the 13 holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

11.5 Power Dissipation and Thermal Considerations

The THS309x incorporates automatic thermal shutoff protection. This protection circuitry shuts down the amplifier if the junction temperature exceeds approximately 160°C. When the junction temperature reduces to approximately 140°C, the amplifier turns on again. But, for maximum performance and reliability, the designer must ensure that the design does not exceed a junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade and long-term reliability suffers. The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}} \quad (4)$$

where:

P_{Dmax} is the maximum power dissipation in the amplifier (W).

T_{max} is the absolute maximum junction temperature (°C).

T_A is the ambient temperature (°C).

$\theta_{JA} = \theta_{JC} + \theta_{CA}$

θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).

θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

For systems where heat dissipation is more critical, the THS3091 and THS3095 are offered in an 8-pin SOIC (DDA) with PowerPAD package. The thermal coefficient for the PowerPAD packages are substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in the graph for the available packages. The data for the PowerPAD packages assume a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application note (*PowerPAD™ Thermally Enhanced Package* application note). If the PowerPAD is not soldered to the PCB, then the thermal impedance will increase substantially which may cause serious heat and performance issues. Be sure to always solder the PowerPAD to the PCB for optimum performance.

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to consider not only quiescent power dissipation, but also dynamic power dissipation. Often times, this is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Evaluation Fixtures, Spice Models, and Application Support

Texas Instruments is committed to providing its customers with the highest quality of applications support. To support this goal, an evaluation board has been developed for the THS309x operational amplifier. The board is easy to use, allowing for straightforward evaluation of the device. The evaluation board can be ordered through the Texas Instruments Web site, www.ti.com, or through your local Texas Instruments sales representative.

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and RF-amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS309x is available through the Texas Instruments Web site (www.ti.com). The Product Information Center (PIC) is also available for design assistance and detailed product information. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They are not intended to model the distortion characteristics of the amplifier, nor do they attempt to distinguish between the package types in their small-signal ac performance. Detailed information about what is and is not modeled is contained in the model file itself.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *PowerPAD™ Made Easy* application brief
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* technical brief
- Texas Instruments, *Voltage Feedback vs Current Feedback Amplifiers* application note
- Texas Instruments, *Current Feedback Analysis and Compensation* application note
- Texas Instruments, *Current Feedback Amplifiers: Review, Stability, and Application* application note
- Texas Instruments, *Effect of Parasitic Capacitance in Op Amp Circuits* application note
- Texas Instruments, *Expanding the Usability of Current-Feedback Amplifiers* analog journal

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS3091D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3091	Samples
THS3091DDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	3091	Samples
THS3091DDAG3	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	3091	Samples
THS3091DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	3091	Samples
THS3091DDARG3	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	3091	Samples
THS3091DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3091	Samples
THS3095D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	3095	Samples
THS3095DDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	3095	Samples
THS3095DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	3095	Samples
XTHS3091IDGNR	ACTIVE	HVSSOP	DGN	8	2500	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

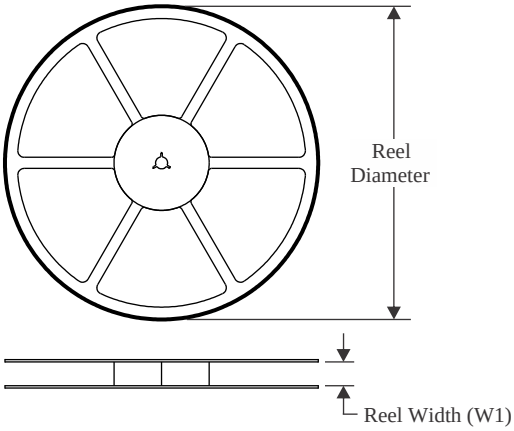
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

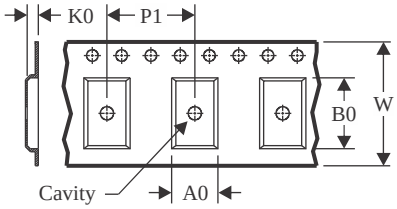
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

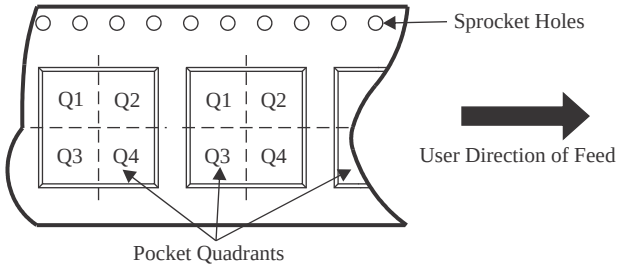


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

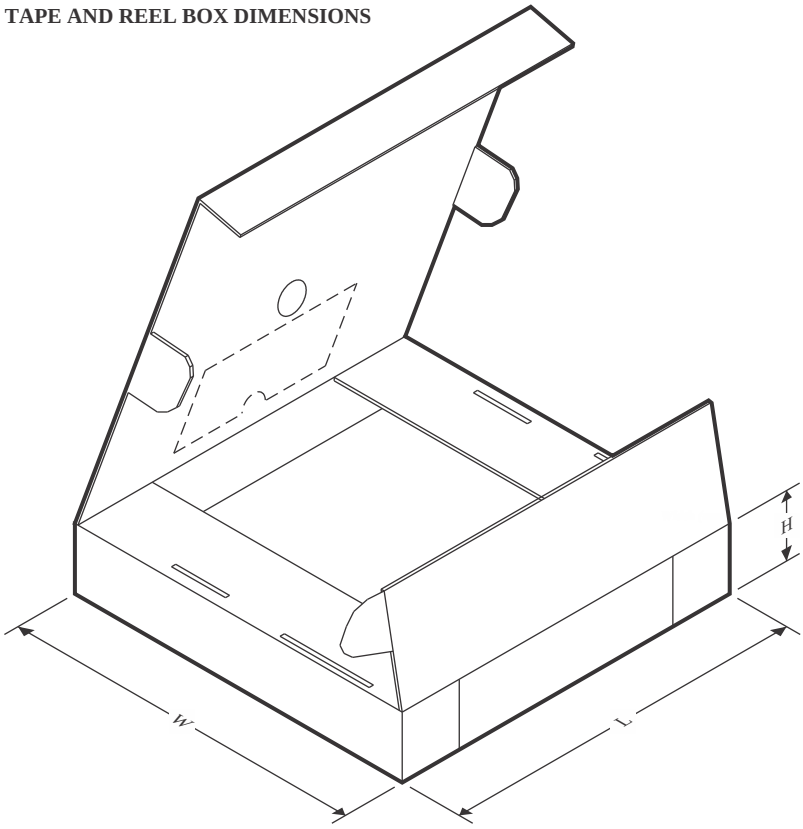
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS3091DDAR	SO PowerPAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS3091DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS3095DDAR	SO PowerPAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

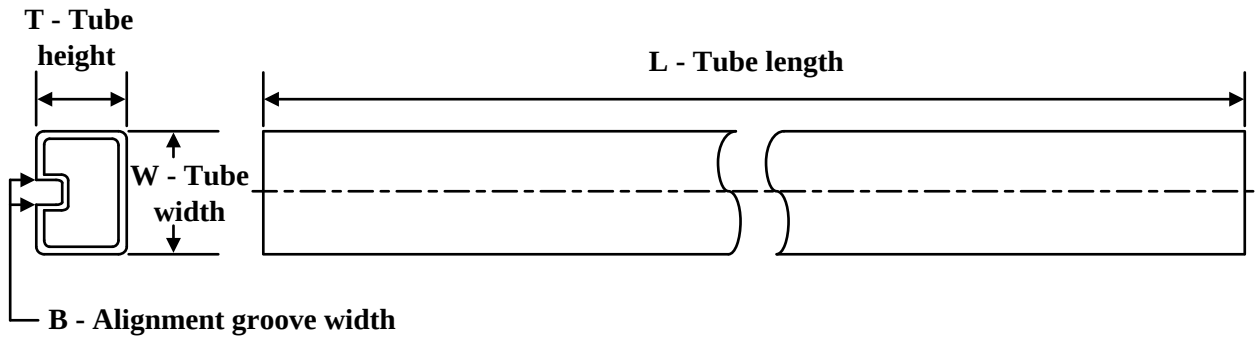
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS3091DDAR	SO PowerPAD	DDA	8	2500	350.0	350.0	43.0
THS3091DR	SOIC	D	8	2500	350.0	350.0	43.0
THS3095DDAR	SO PowerPAD	DDA	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS3091D	D	SOIC	8	75	505.46	6.76	3810	4
THS3091DDA	DDA	HSOIC	8	75	505.46	6.76	3810	4
THS3091DDAG3	DDA	HSOIC	8	75	505.46	6.76	3810	4
THS3095D	D	SOIC	8	75	505.46	6.76	3810	4
THS3095DDA	DDA	HSOIC	8	75	505.46	6.76	3810	4

GENERIC PACKAGE VIEW

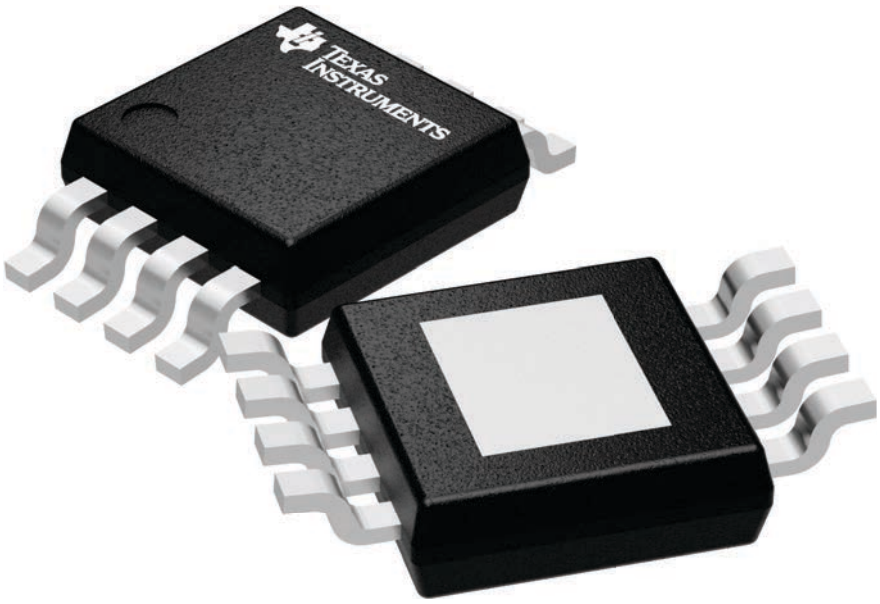
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

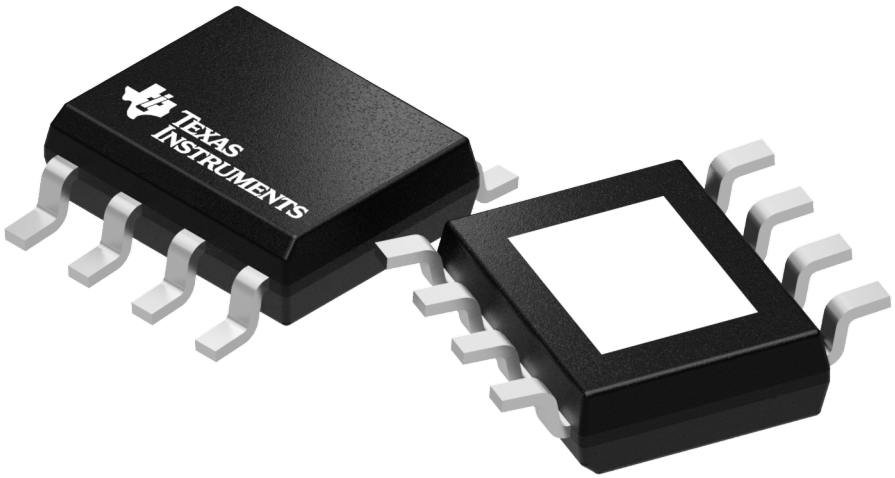
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



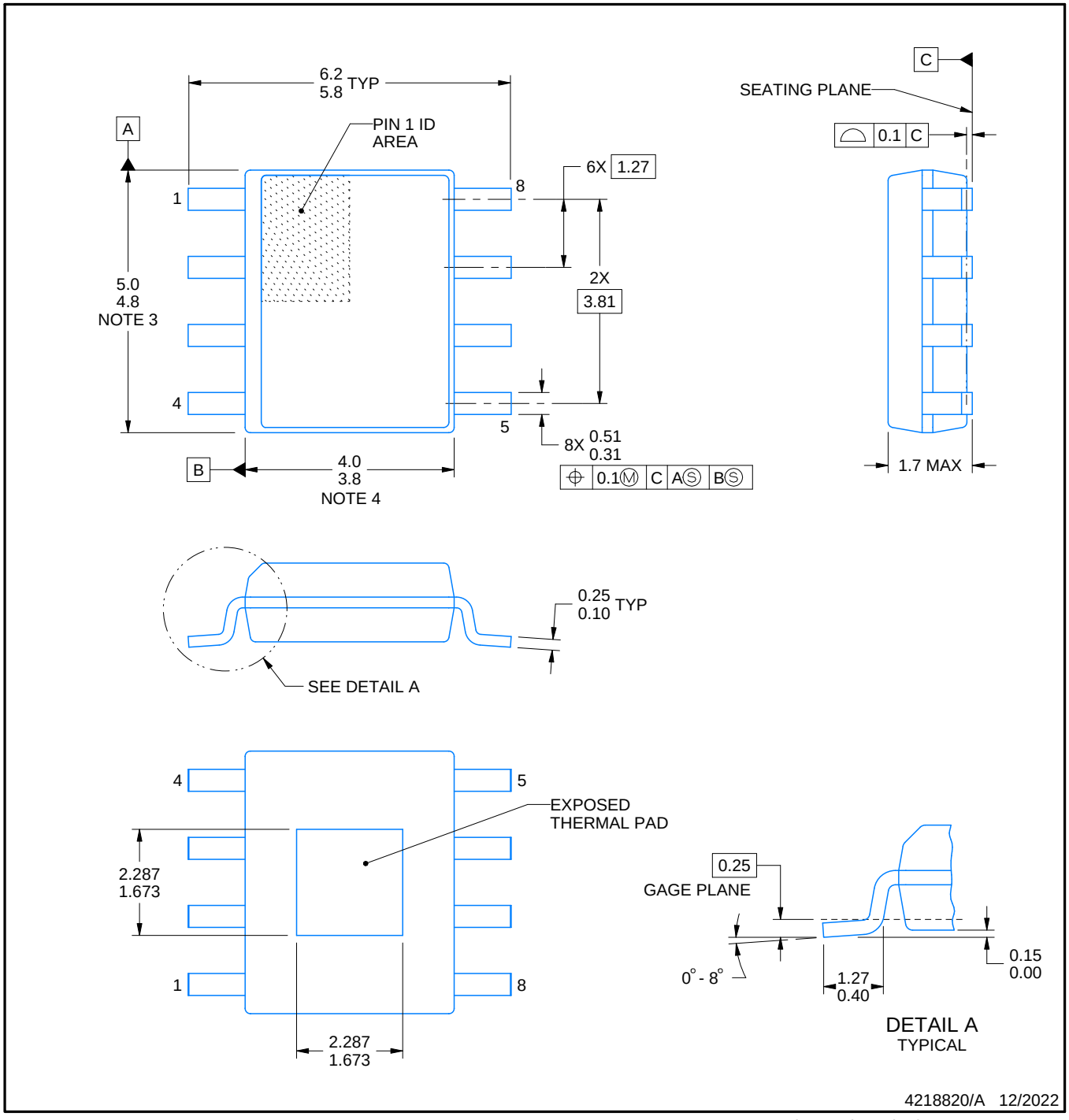
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DDA0008D

PowerPAD™ SOIC - 1.7 mm max height

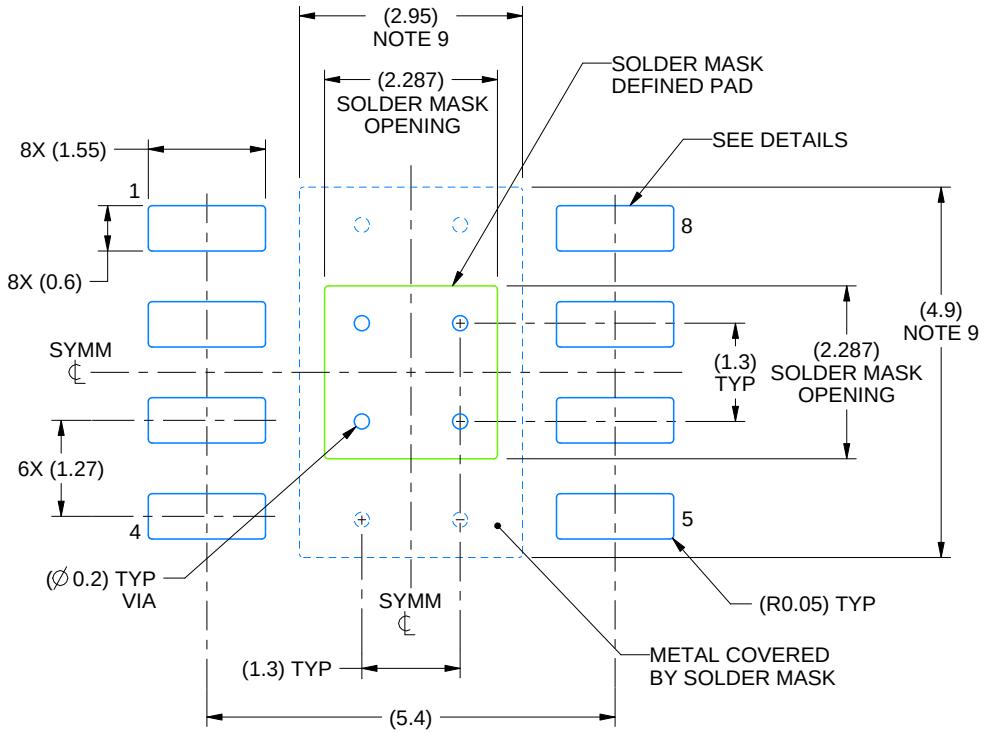
PLASTIC SMALL OUTLINE



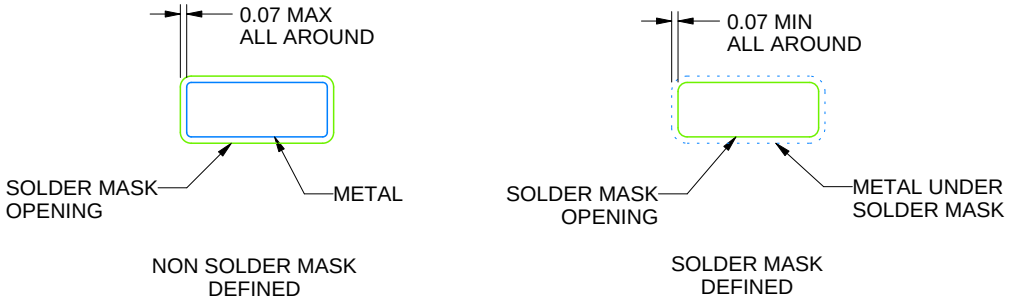
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

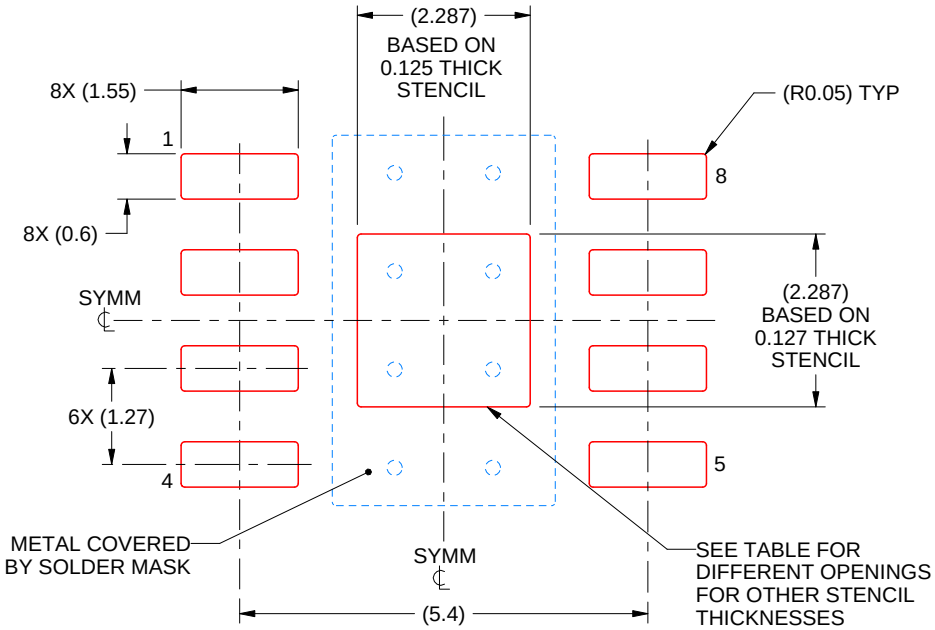


SOLDER MASK DETAILS

4218820/A 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



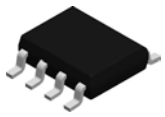
SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.557 X 2.557
0.125	2.287 X 2.287 (SHOWN)
0.150	2.088 X 2.088
0.175	1.933 X 1.933

4218820/A 12/2022

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

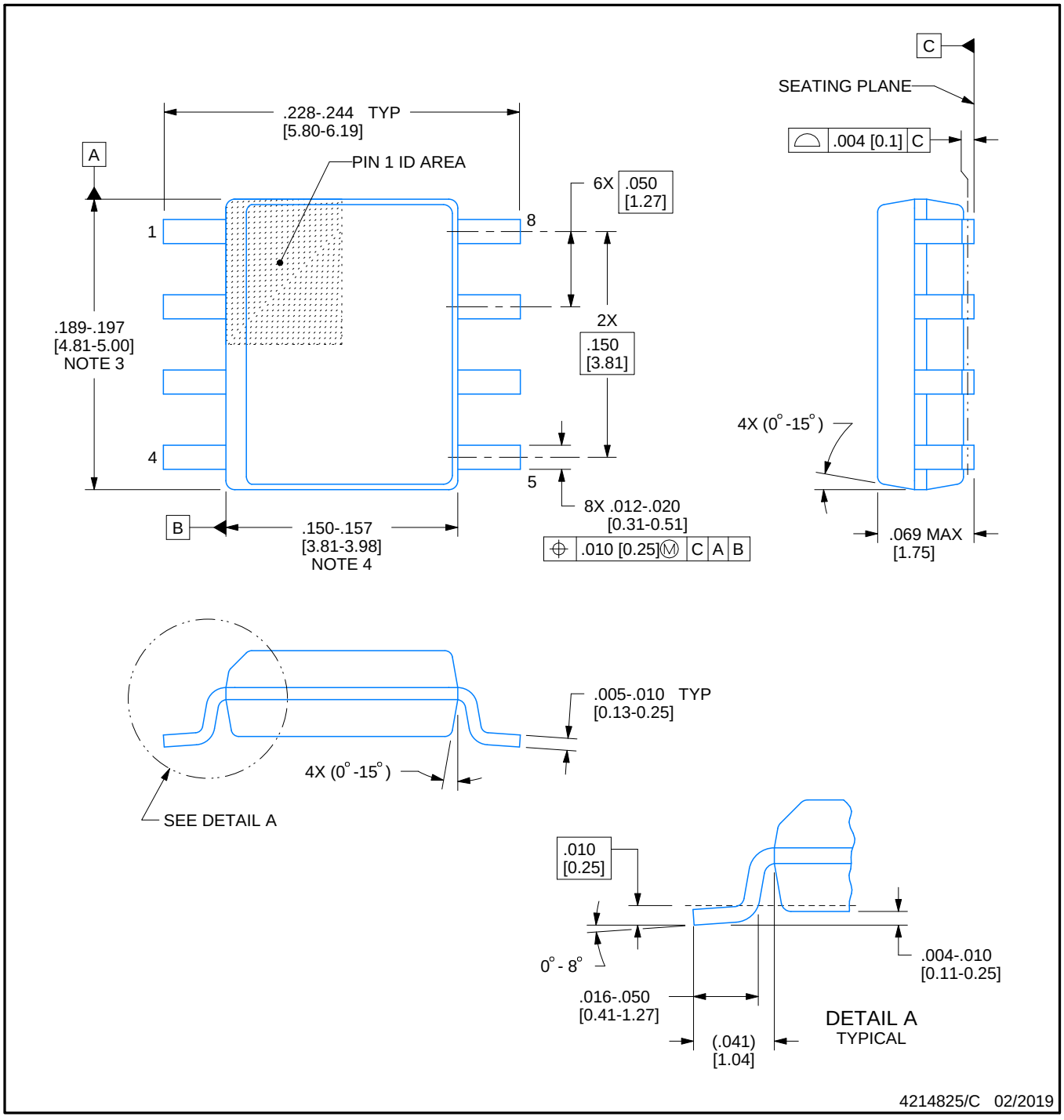


PACKAGE OUTLINE

D0008A

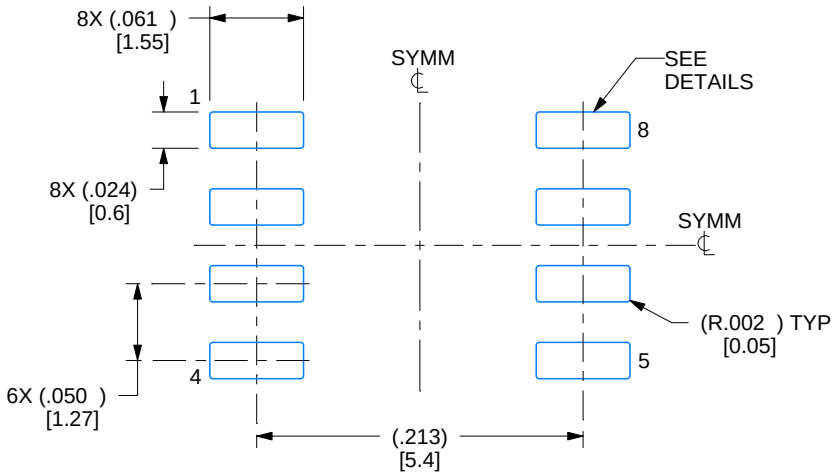
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

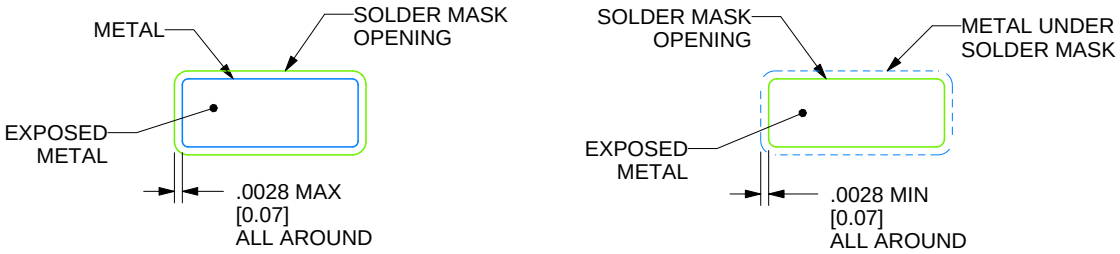


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

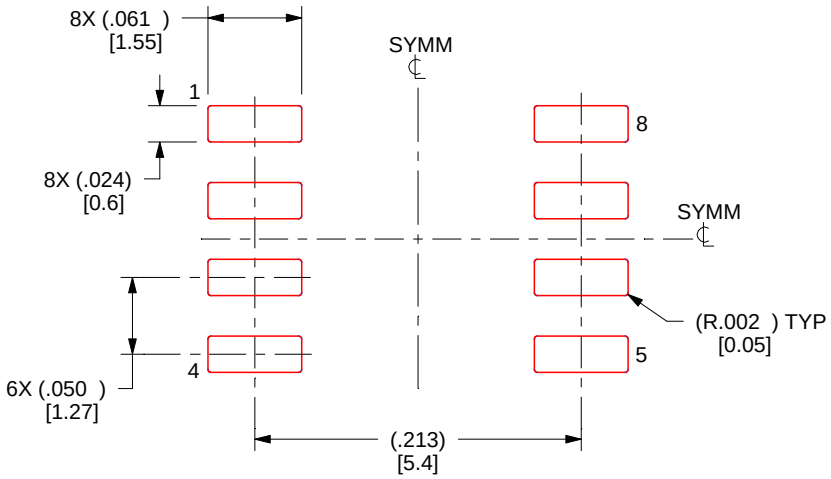
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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