

MAX14434–MAX14436

Four-Channel, Fast, Low-Power, 5kV_{RMS} Digital Isolators

General Description

The MAX14434–MAX14436 are the fastest, lowest power, 4-channel, digital galvanic isolators on the market today using Maxim's proprietary process technology. These devices transfer digital signals between circuits with different power domains while using as little as 0.58mW per channel at 1Mbps with a 1.8V supply. The MAX14434/5/6 have an isolation rating of 5kV_{RMS} for 60 seconds.

The MAX14434–MAX14436 family offers all three possible unidirectional channel configurations to accommodate any 4-channel design, including SPI, RS-232, RS-485, and digital I/O applications. Output enable for the A side of the MAX14435R/S/U/V is active-low, making them ideal for isolating a port on a shared SPI bus since the CS signal can directly enable the MISO signal on the isolator. All other devices in the family have the traditional active-high enable.

Devices are available with a maximum data rate of either 25Mbps or 200Mbps and with outputs that are either default-high or default-low. The default is the state the output assumes when the input is either not powered or is open-circuit. See the [Ordering Information](#) for suffixes associated with each option. Independent 1.71V to 5.5V supplies on each side of the isolator also make the devices suitable for use as level translators.

The MAX14434–MAX14436 are available in a 16-pin wide-body SOIC package with 8mm of creepage and clearance. The package material has a minimum comparative tracking index (CTI) of 600V, which gives it a group 1 rating in creepage tables. All devices are rated for operation at ambient temperatures of -40°C to +125°C.

Benefits and Features

- Robust Galvanic Isolation for Fast Digital Signals
 - 200Mbps Data Rate
 - Withstands 5kV_{RMS} for 60s (V_{ISO})
 - Continuously Withstands 848V_{RMS} (V_{IOWM})
 - Withstands ± 10 kV Surge between GNDA and GNDB with 1.2/50 μ s waveform
 - High CMTI (50kV/ μ s, Typical)
- Low Power Consumption
 - 1.1mW per Channel at 1Mbps with $V_{DD} = 3.3$ V
 - 3.5mW per Channel at 100Mbps with $V_{DD} = 1.8$ V
- Options to Support a Broad Range of Applications
 - 2 Data Rates (25Mbps, 200Mbps)
 - 3 Channel Direction Configurations
 - 2 Output Default States (High/Low)

Applications

- Fieldbus Communications for Industrial Automation
- Isolated RS-485/RS-422, CAN
- General Isolation Application
- Battery Management
- Medical Systems

Safety Regulatory Approvals (Pending)

- UL According to UL1577
- cUL According to CSA Bulletin 5A
- VDE 0884-10

[Ordering Information](#) appears at end of data sheet.

Absolute Maximum Ratings

| | | | |
|--|------------------------------------|--|-----------------|
| V _{DDA} to GNDA..... | -0.3V to +6V | Continuous Power Dissipation (T _A = +70°C) Wide SOIC (derate 14.1mW/°C above +70°C)..... | 1126.8mW |
| V _{DDB} to GNDB..... | -0.3V to +6V | | |
| IN ₋ , EN ₋ on Side A to GNDA..... | -0.3V to +6V | Operating Temperature Range..... | -40°C to +125°C |
| IN ₋ , EN ₋ on Side B to GNDB..... | -0.3V to +6V | Maximum Junction Temperature..... | +150°C |
| OUT ₋ on Side A to GNDA..... | -0.3V to (V _{DDA} + 0.3V) | Storage Temperature Range..... | -60°C to +150°C |
| OUT ₋ on Side B to GNDB..... | -0.3V to (V _{DDB} + 0.3V) | Soldering Temperature (reflow)..... | +260°C |
| Short-Circuit Duration | | | |
| OUT ₋ on Side A to GNDA, | | | |
| OUT ₋ on Side B to GNDB..... | Continuous | | |

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

| | |
|---|-------------------------|
| PACKAGE TYPE: 16 WIDE SOIC | |
| Package Code | W16MS+12 |
| Outline Number | 21-0042 |
| Land Pattern Number | 90-0107 |
| THERMAL RESISTANCE, FOUR-LAYER BOARD | |
| Junction to Ambient (θ _{JA}) | 71°C/W |
| Junction to Case (θ _{JC}) | 24°C/W |

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

DC Electrical Characteristics

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|------------------------|-------------------------|------|-----|------|-------|
| POWER SUPPLY | | | | | | |
| Supply Voltage | V _{DDA} | Relative to GNDA | 1.71 | | 5.5 | V |
| | V _{DDB} | Relative to GNDB | 1.71 | | 5.5 | |
| Undervoltage-Lockout Threshold | V _{UVLO-} | V _{DD-} rising | 1.5 | 1.6 | 1.66 | V |
| Undervoltage-Lockout Threshold Hysteresis | V _{UVLO_HYST} | | | 45 | | mV |

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|-------------------------------------|-------------------|---|--------------------------|-----|------|-------|-------|
| Supply Current (MAX14434_) (Note 2) | I _{DDA} | 500kHz square wave, C _L = 0pF | V _{DDA} = 5V | | 0.52 | 0.96 | mA |
| | | | V _{DDA} = 3.3V | | 0.51 | 0.93 | |
| | | | V _{DDA} = 2.5V | | 0.50 | 0.92 | |
| | | | V _{DDA} = 1.8V | | 0.49 | 0.64 | |
| | | 12.5MHz square wave, C _L = 0pF | V _{DDA} = 5V | | 1.63 | 2.42 | |
| | | | V _{DDA} = 3.3V | | 1.59 | 2.36 | |
| | | | V _{DDA} = 2.5V | | 1.58 | 2.33 | |
| | | | V _{DDA} = 1.8V | | 1.54 | 2.00 | |
| | | 50MHz square wave, C _L = 0pF | V _{DDA} = 5V | | 4.5 | 6.14 | |
| | | | V _{DDA} = 3.3V | | 4.39 | 6.00 | |
| | | | V _{DDA} = 2.5V | | 4.35 | 5.93 | |
| | | | V _{DDA} = 1.8V | | 4.21 | 5.43 | |
| Supply Current (MAX14434_) (Note 2) | I _{DDDB} | 500kHz square wave, C _L = 0pF | V _{DDDB} = 5V | | 0.87 | 1.47 | mA |
| | | | V _{DDDB} = 3.3V | | 0.82 | 1.41 | |
| | | | V _{DDDB} = 2.5V | | 0.81 | 1.39 | |
| | | | V _{DDDB} = 1.8V | | 0.79 | 1.32 | |
| | | 12.5MHz square wave, C _L = 0pF | V _{DDDB} = 5V | | 2.97 | 3.84 | |
| | | | V _{DDDB} = 3.3V | | 2.00 | 2.74 | |
| | | | V _{DDDB} = 2.5V | | 1.69 | 2.36 | |
| | | | V _{DDDB} = 1.8V | | 1.43 | 2.02 | |
| | | 50MHz square wave, C _L = 0pF | V _{DDDB} = 5V | | 9.52 | 11.17 | |
| | | | V _{DDDB} = 3.3V | | 5.68 | 6.88 | |
| | | | V _{DDDB} = 2.5V | | 4.45 | 5.38 | |
| | | | V _{DDDB} = 1.8V | | 3.46 | 4.18 | |
| Supply Current (MAX14435_) (Note 2) | I _{DDA} | 500kHz square wave, C _L = 0pF | V _{DDA} = 5V | | 0.62 | 1.10 | mA |
| | | | V _{DDA} = 3.3V | | 0.60 | 1.06 | |
| | | | V _{DDA} = 2.5V | | 0.59 | 1.05 | |
| | | | V _{DDA} = 1.8V | | 0.57 | 0.83 | |
| | | 12.5MHz square wave, C _L = 0pF | V _{DDA} = 5V | | 1.98 | 2.80 | |
| | | | V _{DDA} = 3.3V | | 1.70 | 2.47 | |
| | | | V _{DDA} = 2.5V | | 1.61 | 2.35 | |
| | | | V _{DDA} = 1.8V | | 1.52 | 2.02 | |
| | | 50MHz square wave, C _L = 0pF | V _{DDA} = 5V | | 5.77 | 7.43 | |
| | | | V _{DDA} = 3.3V | | 4.73 | 6.25 | |
| | | | V _{DDA} = 2.5V | | 4.38 | 5.81 | |
| | | | V _{DDA} = 1.8V | | 4.03 | 5.15 | |

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|-------------------------------------|------------------|---|-------------------------|------|------|-----|-------|
| Supply Current (MAX14435_) (Note 2) | I _{DDB} | 500kHz square wave, C _L = 0pF | V _{DDB} = 5V | 0.78 | 1.35 | mA | |
| | | | V _{DDB} = 3.3V | 0.75 | 1.30 | | |
| | | | V _{DDB} = 2.5V | 0.74 | 1.28 | | |
| | | | V _{DDB} = 1.8V | 0.72 | 1.16 | | |
| | | 12.5MHz square wave, C _L = 0pF | V _{DDB} = 5V | 2.64 | 3.49 | | |
| | | | V _{DDB} = 3.3V | 1.90 | 2.65 | | |
| | | | V _{DDB} = 2.5V | 1.66 | 2.36 | | |
| | | | V _{DDB} = 1.8V | 1.46 | 2.03 | | |
| | | 50MHz square wave, C _L = 0pF | V _{DDB} = 5V | 8.26 | 9.91 | | |
| | | | V _{DDB} = 3.3V | 5.36 | 6.66 | | |
| | | | V _{DDB} = 2.5V | 4.42 | 5.52 | | |
| | | | V _{DDB} = 1.8V | 3.66 | 4.51 | | |
| Supply Current (MAX14436_) (Note 2) | I _{DDA} | 500kHz square wave, C _L = 0pF | V _{DDA} = 5V | 0.70 | 1.22 | mA | |
| | | | V _{DDA} = 3.3V | 0.67 | 1.17 | | |
| | | | V _{DDA} = 2.5V | 0.66 | 1.16 | | |
| | | | V _{DDA} = 1.8V | 0.64 | 0.99 | | |
| | | 12.5MHz square wave, C _L = 0pF | V _{DDA} = 5V | 2.31 | 3.15 | | |
| | | | V _{DDA} = 3.3V | 1.81 | 2.56 | | |
| | | | V _{DDA} = 2.5V | 1.64 | 2.35 | | |
| | | | V _{DDA} = 1.8V | 1.50 | 2.02 | | |
| | | 50MHz square wave, C _L = 0pF | V _{DDA} = 5V | 7.04 | 8.70 | | |
| | | | V _{DDA} = 3.3V | 5.06 | 6.46 | | |
| | | | V _{DDA} = 2.5V | 4.40 | 5.67 | | |
| | | | V _{DDA} = 1.8V | 3.85 | 4.83 | | |
| | I _{DDB} | 500kHz square wave, C _L = 0pF | V _{DDB} = 5V | 0.70 | 1.24 | mA | |
| | | | V _{DDB} = 3.3V | 0.67 | 1.19 | | |
| | | | V _{DDB} = 2.5V | 0.66 | 1.17 | | |
| | | | V _{DDB} = 1.8V | 0.65 | 1.00 | | |
| | | 12.5MHz square wave, C _L = 0pF | V _{DDB} = 5V | 2.31 | 3.15 | | |
| | | | V _{DDB} = 3.3V | 1.80 | 2.57 | | |
| | | | V _{DDB} = 2.5V | 1.64 | 2.36 | | |
| | | | V _{DDB} = 1.8V | 1.49 | 2.03 | | |
| | | 50MHz square wave, C _L = 0pF | V _{DDB} = 5V | 7.01 | 8.66 | | |
| | | | V _{DDB} = 3.3V | 5.04 | 6.46 | | |
| | | | V _{DDB} = 2.5V | 4.40 | 5.67 | | |
| | | | V _{DDB} = 1.8V | 3.84 | 4.83 | | |

DC Electrical Characteristics (continued)

($V_{DDA} - V_{GNDA} = 1.71V$ to $5.5V$, $V_{DDB} - V_{GNDB} = 1.71V$ to $5.5V$, $C_L = 15pF$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $V_{DDA} - V_{GNDA} = 3.3V$, $V_{DDB} - V_{GNDB} = 3.3V$, $V_{GNDA} = V_{GNDB}$, $T_A = +25^{\circ}C$, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---------------------------------|--------------|--|---------------------------------|-------------------|------|---------|
| LOGIC INPUTS AND OUTPUTS | | | | | | |
| Input High Voltage | V_{IH} | EN_, IN_, relative to GND_ | $2.25V \leq V_{DD_} \leq 5.5V$ | 0.7 x $V_{DD_}$ | | V |
| | | EN_, IN_, relative to GND_ | $1.71V \leq V_{DD_} < 2.25V$ | 0.75 x $V_{DD_}$ | | |
| Input Low Voltage | V_{IL} | EN_, IN_, relative to GND_ | $2.25V \leq V_{DD_} \leq 5.5V$ | 0.8 | | V |
| | | EN_, IN_, relative to GND_ | $1.71V \leq V_{DD_} < 2.25V$ | 0.7 | | |
| Input Hysteresis | V_{HYS} | EN_, IN_, relative to GND_ | MAX1443_B/E/R/U | 410 | | mV |
| | | EN_, IN_, relative to GND_ | MAX1443_C/F/S/V | 80 | | |
| Input Pullup Current (Note 3) | I_{PU} | IN_, MAX1443_B/C/R/S | -10 | -5 | -1.5 | μA |
| Input Pulldown Current (Note 3) | I_{PD} | IN_, MAX1443_E/F/U/V | 1.5 | 5 | 10 | μA |
| EN Pullup Current (Note 3) | I_{PU_EN} | EN_ | -10 | -5 | -1.5 | μA |
| Input Capacitance | C_{IN} | IN_, $f_{SW} = 1MHz$ | 2 | | | pF |
| Output Voltage High (Note 3) | V_{OH} | $V_{OUT_}$ relative to GND_ $I_{OUT_} = 4mA$ source | $V_{DD_}$ - 0.4 | | | V |
| Output Voltage Low (Note 3) | V_{OL} | $V_{OUT_}$ relative to GND_ $I_{OUT_} = 4mA$ sink | | | 0.4 | V |

Dynamic Characteristics MAX1443_C/F/S/V

($V_{DDA} - V_{GNDA} = 1.71V$ to $5.5V$, $V_{DDB} - V_{GNDB} = 1.71V$ to $5.5V$, $C_L = 15pF$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $V_{DDA} - V_{GNDA} = 3.3V$, $V_{DDB} - V_{GNDB} = 3.3V$, $V_{GNDA} = V_{GNDB}$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|--|--------------------|---|---------------------------------|------|------|------|-------------|
| Common-Mode Transient Immunity | CMTI | IN ₋ = GND ₋ or V _{DD-} (Note 4) | | 50 | | | kV/ μ s |
| Maximum Data Rate | DR _{MAX} | $2.25V \leq V_{DD-} \leq 5.5V$ | | 200 | | | Mbps |
| | | $1.71V \leq V_{DD-} \leq 1.89V$ | | 150 | | | |
| Minimum Pulse Width | PW _{MIN} | IN ₋ to OUT ₋ | $2.25V \leq V_{DD-} \leq 5.5V$ | 5 | | | ns |
| | | | $1.71V \leq V_{DD-} \leq 1.89V$ | 6.67 | | | |
| Propagation Delay (Figure 1) | t _{PLH} | IN ₋ to OUT ₋ , C _L = 15pF | $4.5V \leq V_{DD-} \leq 5.5V$ | 4.1 | 5.4 | 9.2 | ns |
| | | | $3.0V \leq V_{DD-} \leq 3.6V$ | 4.2 | 5.9 | 10.2 | |
| | | | $2.25V \leq V_{DD-} \leq 2.75V$ | 4.9 | 7.1 | 13.4 | |
| | | | $1.71V \leq V_{DD-} \leq 1.89V$ | 7.1 | 10.9 | 20.3 | |
| | t _{PHL} | IN ₋ to OUT ₋ , C _L = 15pF | $4.5V \leq V_{DD-} \leq 5.5V$ | 4.3 | 5.6 | 9.4 | |
| | | | $3.0V \leq V_{DD-} \leq 3.6V$ | 4.4 | 6.2 | 10.5 | |
| | | | $2.25V \leq V_{DD-} \leq 2.75V$ | 5.1 | 7.3 | 14.1 | |
| | | | $1.71V \leq V_{DD-} \leq 1.89V$ | 7.2 | 10.9 | 21.7 | |
| Pulse Width Distortion | PWD | t _{PLH} - t _{PHL} | | 0.3 | 2 | ns | |
| Propagation Delay Skew Part-to-Part (Same Channel) | t _{SPLH} | $4.5V \leq V_{DD-} \leq 5.5V$ | | 3.7 | | | ns |
| | | $3.0V \leq V_{DD-} \leq 3.6V$ | | 4.3 | | | |
| | | $2.25V \leq V_{DD-} \leq 2.75V$ | | 6 | | | |
| | | $1.71V \leq V_{DD-} \leq 1.89V$ | | 10.3 | | | |
| | t _{SPHL} | $4.5V \leq V_{DD-} \leq 5.5V$ | | 3.8 | | | |
| | | $3.0V \leq V_{DD-} \leq 3.6V$ | | 4.7 | | | |
| | | $2.25V \leq V_{DD-} \leq 2.75V$ | | 6.5 | | | |
| | | $1.71V \leq V_{DD-} \leq 1.89V$ | | 11.5 | | | |
| Propagation Delay Skew Channel-to-Channel (Same Direction) | t _{SCSLH} | $1.71V \leq V_{DD-} \leq 5.5V$ | | 1.5 | | | ns |
| | t _{SCSHL} | $1.71V \leq V_{DD-} \leq 5.5V$ | | 1.5 | | | |

Dynamic Characteristics MAX1443_C/F/S/V (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------------------|---|----------------------------------|-----|------|-------|
| Propagation Delay Skew Channel-to-Channel (Opposite Direction) | t _{SCOLH} | 4.5V ≤ V _{DD_} ≤ 5.5V | | | 2.9 | ns |
| | | 3.0V ≤ V _{DD_} ≤ 3.6V | | | 3.4 | |
| | | 2.25V ≤ V _{DD_} ≤ 2.75V | | | 4.9 | |
| | | 1.71V ≤ V _{DD_} ≤ 1.89V | | | 10.2 | |
| | t _{SCOHL} | 4.5V ≤ V _{DD_} ≤ 5.5V | | | 3.2 | |
| | | 3.0V ≤ V _{DD_} ≤ 3.6V | | | 3.8 | |
| | | 2.25V ≤ V _{DD_} ≤ 2.75V | | | 5.3 | |
| | | 1.71V ≤ V _{DD_} ≤ 1.89V | | | 10.9 | |
| Peak Eye Diagram Jitter | T _{JIT(PK)} | 200Mbps | | 90 | | ps |
| Clock Jitter RMS | T _{JCLK(RMS)} | 500kHz Clock Input, Rising/Falling Edges | | 6.5 | | ps |
| Rise Time | t _R | 4.5V ≤ V _{DD_} ≤ 5.5V | | | 1.6 | ns |
| | | 3.0V ≤ V _{DD_} ≤ 3.6V | | | 2.2 | |
| | | 2.25V ≤ V _{DD_} ≤ 2.75V | | | 3 | |
| | | 1.71V ≤ V _{DD_} ≤ 1.89V | | | 4.5 | |
| Fall Time | t _F | 4.5V ≤ V _{DD_} ≤ 5.5V | | | 1.4 | ns |
| | | 3.0V ≤ V _{DD_} ≤ 3.6V | | | 2 | |
| | | 2.25V ≤ V _{DD_} ≤ 2.75V | | | 2.8 | |
| | | 1.71V ≤ V _{DD_} ≤ 1.89V | | | 5.1 | |
| Enable to Data Valid | t _{EN} | ENA to OUT_ ₊ , ENB to OUT_ ₊ , C _L = 15pF | 4.5V ≤ V _{DD_} ≤ 5.5V | | 3.5 | ns |
| | | | 3.0V ≤ V _{DD_} ≤ 3.6V | | 5.8 | |
| | | | 2.25V ≤ V _{DD_} ≤ 2.75V | | 9.3 | |
| | | | 1.71V ≤ V _{DD_} ≤ 1.89V | | 17.4 | |
| Enable to Tristate | t _{TRI} | ENA to OUT_ ₊ , ENB to OUT_ ₊ , C _L = 15pF | 4.5V ≤ V _{DD_} ≤ 5.5V | | 6.4 | ns |
| | | | 3.0V ≤ V _{DD_} ≤ 3.6V | | 9.2 | |
| | | | 2.25V ≤ V _{DD_} ≤ 2.75V | | 12.8 | |
| | | | 1.71V ≤ V _{DD_} ≤ 1.89V | | 19.4 | |

Dynamic Characteristics MAX1443_B/E/R/U

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | |
|--|--------------------|---|----------------------------------|------|------|-------|----|
| Common-Mode Transient Immunity | CMTI | IN_ = GND_ or V _{DD_} (Note 4) | | 50 | | kV/μs | |
| Maximum Data Rate | DR _{MAX} | | 25 | | | Mbps | |
| Minimum Pulse Width | PW _{MIN} | IN_ to OUT_ | | | 40 | ns | |
| Glitch Rejection | | IN_ to OUT_ | 10 | 17 | 29 | ns | |
| Propagation Delay (Figure 1) | t _{PLH} | IN_ to OUT_, C _L = 15pF | 4.5V ≤ V _{DD_} ≤ 5.5V | 17.4 | 23.9 | 32.5 | ns |
| | | | 3.0V ≤ V _{DD_} ≤ 3.6V | 17.6 | 24.4 | 33.7 | |
| | | | 2.25V ≤ V _{DD_} ≤ 2.75V | 18.3 | 25.8 | 36.7 | |
| | | | 1.71V ≤ V _{DD_} ≤ 1.89V | 20.7 | 29.6 | 43.5 | |
| | t _{PHL} | IN_ to OUT_, C _L = 15pF | 4.5V ≤ V _{DD_} ≤ 5.5V | 16.9 | 23.4 | 33.6 | |
| | | | 3.0V ≤ V _{DD_} ≤ 3.6V | 17.2 | 24.2 | 35.1 | |
| | | | 2.25V ≤ V _{DD_} ≤ 2.75V | 17.8 | 25.4 | 38.2 | |
| | | | 1.71V ≤ V _{DD_} ≤ 1.89V | 19.8 | 29.3 | 45.8 | |
| Pulse Width Distortion | PWD | t _{PLH} - t _{PHL} | | 0.4 | 4 | ns | |
| Propagation Delay Skew Part-to-Part (Same Channel) | t _{SPLH} | 4.5V ≤ V _{DD_} ≤ 5.5V | | | 15.1 | ns | |
| | | 3.0V ≤ V _{DD_} ≤ 3.6V | | | 15 | | |
| | | 2.25V ≤ V _{DD_} ≤ 2.75V | | | 15.4 | | |
| | | 1.71V ≤ V _{DD_} ≤ 1.89V | | | 20.5 | | |
| | t _{SPHL} | 4.5V ≤ V _{DD_} ≤ 5.5V | | | 13.9 | | |
| | | 3.0V ≤ V _{DD_} ≤ 3.6V | | | 14.2 | | |
| | | 2.25V ≤ V _{DD_} ≤ 2.75V | | | 16 | | |
| | | 1.71V ≤ V _{DD_} ≤ 1.89V | | | 21.8 | | |
| Propagation Delay Skew Channel-to-Channel (Same Direction) | t _{SCSLH} | 1.71V ≤ V _{DD_} ≤ 5.5V | | | 2 | ns | |
| | t _{SCSHL} | 1.71V ≤ V _{DD_} ≤ 5.5V | | | 2 | | |
| Propagation Delay Skew Channel-to-Channel (Opposite Direction) | t _{SCOLH} | 4.5V ≤ V _{DD_} ≤ 5.5V | | | 13.9 | ns | |
| | | 3.0V ≤ V _{DD_} ≤ 3.6V | | | 13.7 | | |
| | | 2.25V ≤ V _{DD_} ≤ 2.75V | | | 14.2 | | |
| | | 1.71V ≤ V _{DD_} ≤ 1.89V | | | 19.4 | | |
| | t _{SCOHL} | 4.5V ≤ V _{DD_} ≤ 5.5V | | | 13 | | |
| | | 3.0V ≤ V _{DD_} ≤ 3.6V | | | 12.9 | | |
| | | 2.25V ≤ V _{DD_} ≤ 2.75V | | | 14.4 | | |
| | | 1.71V ≤ V _{DD_} ≤ 1.89V | | | 20.1 | | |

Dynamic Characteristics MAX1443_B/E/R/U (continued)

($V_{DDA} - V_{GNDA} = 1.71V$ to $5.5V$, $V_{DDB} - V_{GNDB} = 1.71V$ to $5.5V$, $C_L = 15pF$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $V_{DDA} - V_{GNDA} = 3.3V$, $V_{DDB} - V_{GNDB} = 3.3V$, $V_{GNDA} = V_{GNDB}$, $T_A = +25^\circ C$, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------|---------------|--|----------------------------------|-----|------|-------|
| Peak Eye Diagram Jitter | $T_{JIT(PK)}$ | 25Mbps | | 250 | | ps |
| Rise Time (Figure 1) | t_R | $4.5V \leq V_{DD_} \leq 5.5V$ | | | 1.6 | ns |
| | | $3.0V \leq V_{DD_} \leq 3.6V$ | | | 2.2 | |
| | | $2.25V \leq V_{DD_} \leq 2.75V$ | | | 3 | |
| | | $1.71V \leq V_{DD_} \leq 1.89V$ | | | 4.5 | |
| Fall Time (Figure 1) | t_F | $4.5V \leq V_{DD_} \leq 5.5V$ | | | 1.4 | ns |
| | | $3.0V \leq V_{DD_} \leq 3.6V$ | | | 2 | |
| | | $2.25V \leq V_{DD_} \leq 2.75V$ | | | 2.8 | |
| | | $1.71V \leq V_{DD_} \leq 1.89V$ | | | 5.1 | |
| Enable to Data Valid | t_{EN} | ENA to OUT ₋ , ENB to OUT ₋ , $C_L = 15pF$ | $4.5V \leq V_{DD_} \leq 5.5V$ | | 3.5 | ns |
| | | | $3.0V \leq V_{DD_} \leq 3.6V$ | | 5.8 | |
| | | | $2.25V \leq V_{DD_} \leq 2.75V$ | | 9.3 | |
| | | | $1.71V \leq V_{DD_} \leq 1.89V$ | | 17.4 | |
| Enable to Tristate | t_{TRI} | ENA to OUT ₋ , ENB to OUT ₋ , $C_L = 15pF$ | $4.5V \leq V_{DD_} \leq 5.5V$ | | 6.4 | ns |
| | | | $3.0V \leq V_{DD_} \leq 3.6V$ | | 9.2 | |
| | | | $2.25V \leq V_{DD_} \leq 2.75V$ | | 12.8 | |
| | | | $1.71V \leq V_{DD_} \leq 1.89V$ | | 19.4 | |

Note 1: All devices are 100% production tested at $T_A = +25^\circ C$. Specifications over temperature are guaranteed by design.

Note 2: Not production tested. Guaranteed by design and characterization,

Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or GNDB), unless otherwise noted.

Note 4: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB ($V_{CM} = 1000V$).

ESD Protection

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------|--------|----------------------------|-----|-----|-----|-------|
| ESD | | Human Body Model, All Pins | | ±4 | | kV |

Table 1. Insulation Characteristics

| PARAMETER | SYMBOL | CONDITIONS | VALUE | UNITS |
|---|-------------------|--|-------------------|------------------|
| Partial Discharge Test Voltage | V _{PR} | Method B1 = V _{IORM} × 1.875 (t = 1s, partial discharge < 5pC) | 2250 | V _P |
| Maximum Repetitive Peak Isolation Voltage | V _{IORM} | (Note 5) | 1200 | V _P |
| Maximum Working Isolation Voltage | V _{IOWM} | Continuous RMS voltage (Note 5) | 848 | V _{RMS} |
| Maximum Transient Isolation Voltage | V _{IOTM} | t = 1s | 8400 | V _P |
| Maximum Withstand Isolation Voltage | V _{ISO} | f _{SW} = 60Hz, duration = 60s (Note 6) | 5000 | V _{RMS} |
| Maximum Surge Isolation Voltage | V _{IOSM} | Basic Insulation, 1.2/50µs pulse per IEC61000-4-5 | 10 | kV |
| Insulation Resistance | R _S | V _{IO} = 500V | >10 ¹² | Ω |
| Barrier Capacitance Side A to Side B | C _{IO} | f _{SW} = 1MHz (Note 7) | 2 | pF |
| Minimum Creepage Distance | CPG | | 8 | mm |
| Minimum Clearance Distance | CLR | | 8 | mm |
| Internal Clearance | | Distance through insulation | 0.015 | mm |
| Comparative Tracking Index | CTI | Material Group I (IEC 60112) | >600 | |
| Climate Category | | | 40/125/21 | |
| Pollution Degree (DIN VDE 0110, Table 1) | | | 2 | |

Note 5: V_{ISO}, V_{IOWM}, and V_{IORM} are defined by the IEC 60747-5-5 standard.

Note 6: Product is qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.

Note 7: Capacitance is measured with all pins on field-side and logic-side tied together.

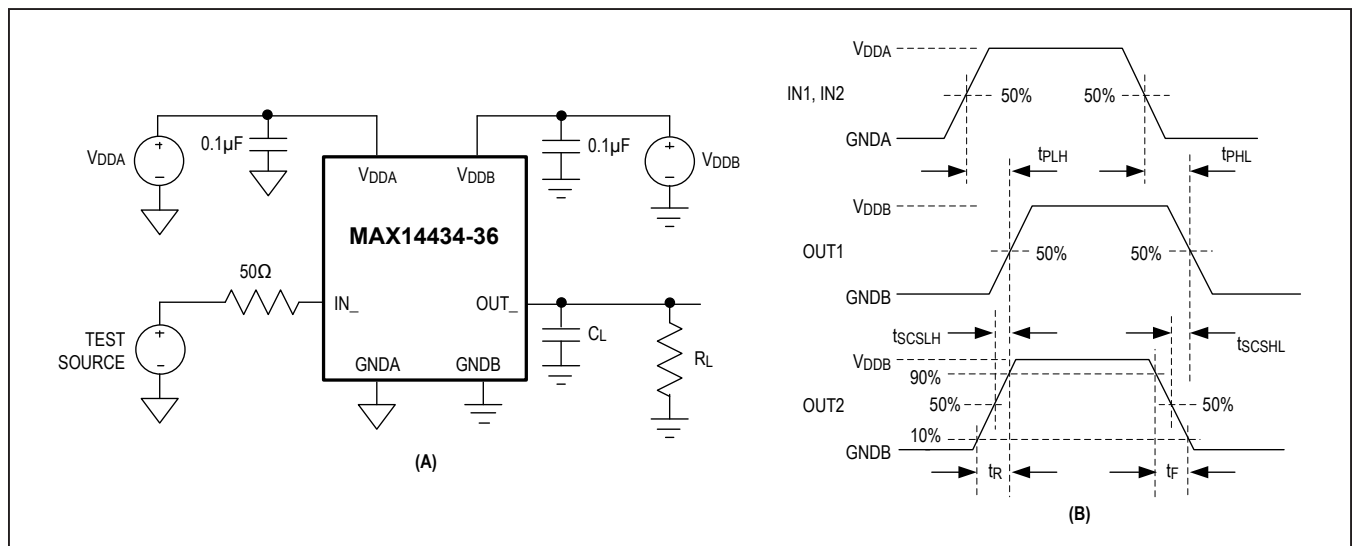
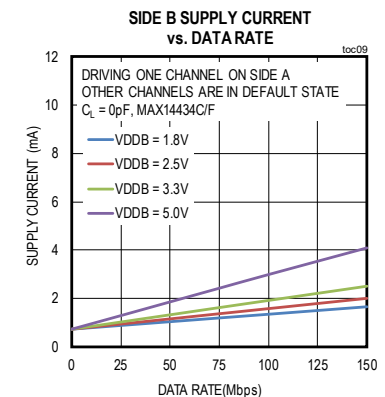
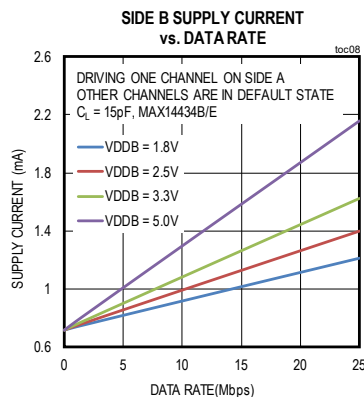
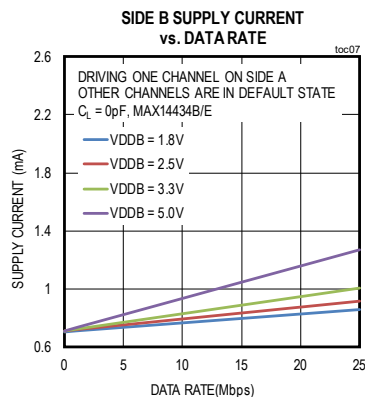
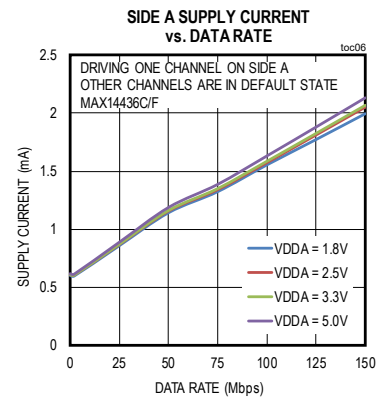
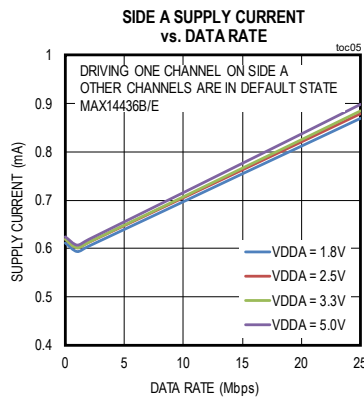
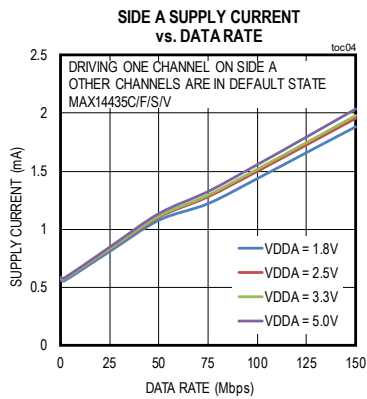
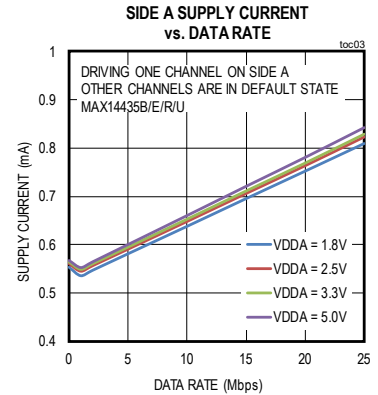
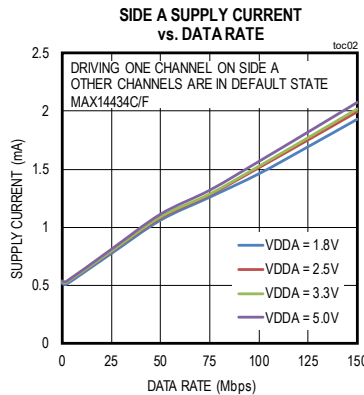
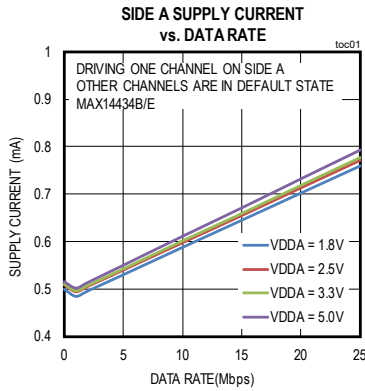


Figure 1. Test Circuit (A) and Timing Diagram (B)

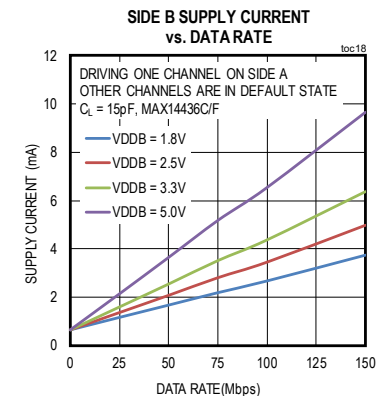
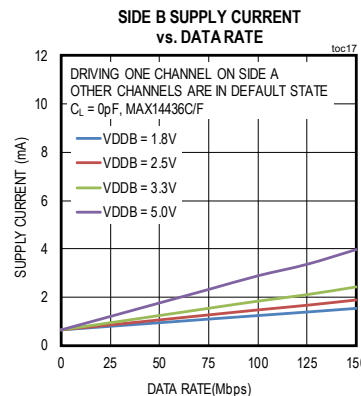
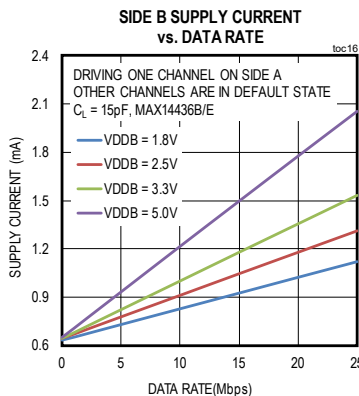
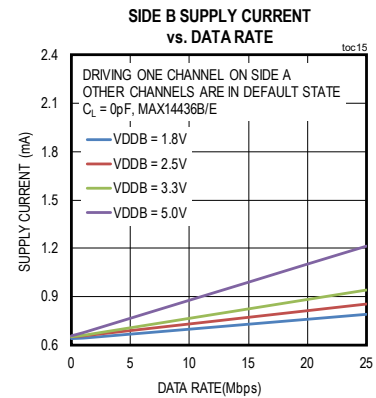
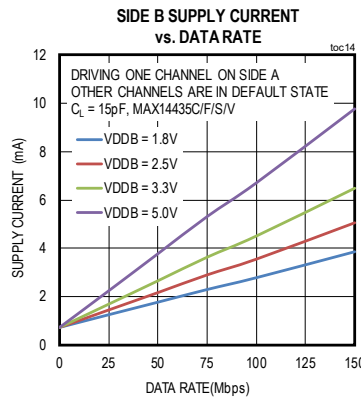
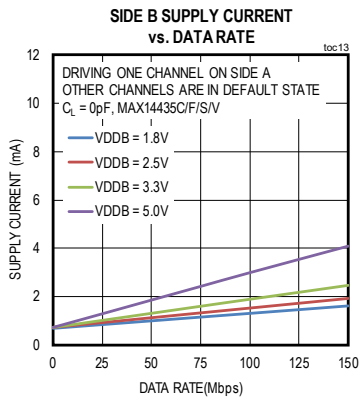
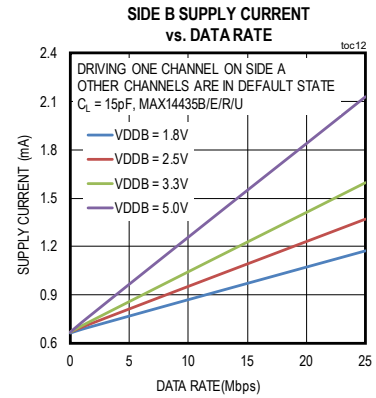
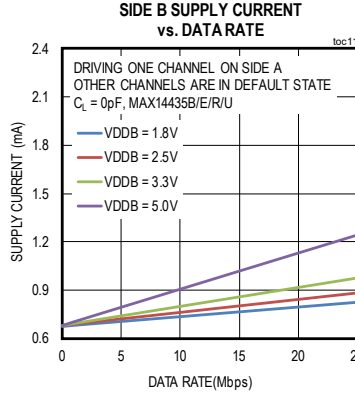
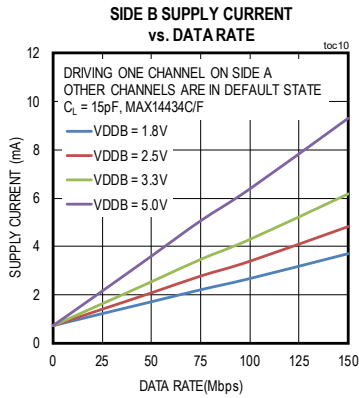
Typical Operating Characteristics

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)



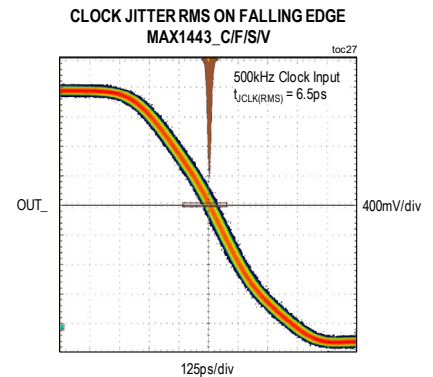
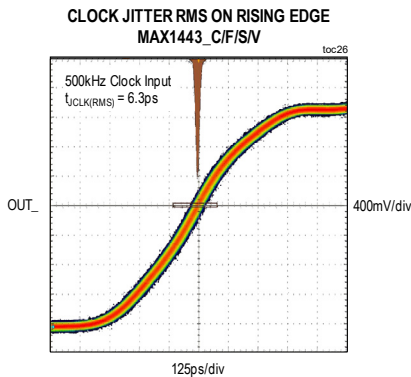
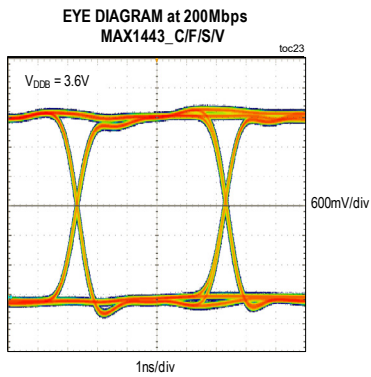
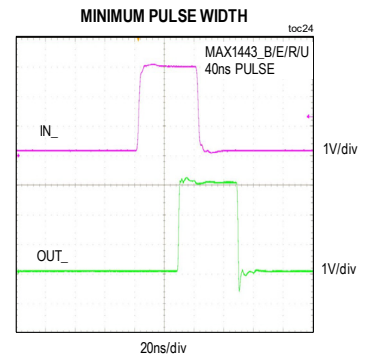
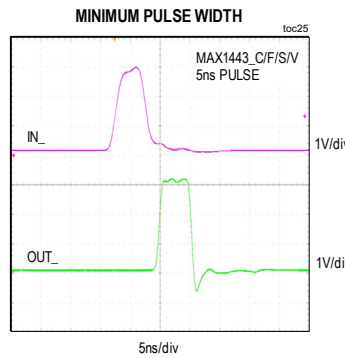
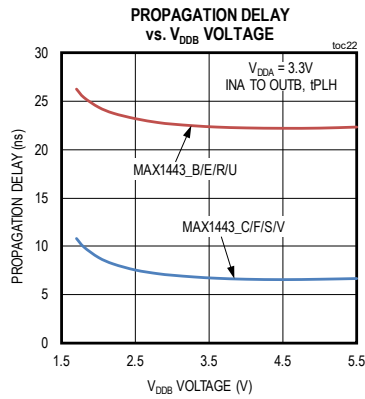
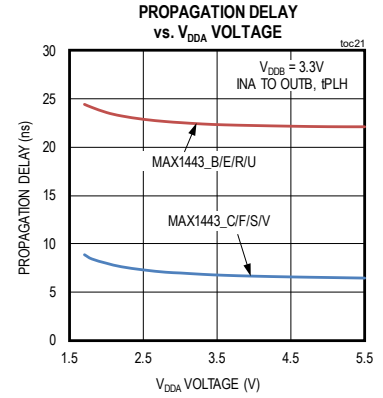
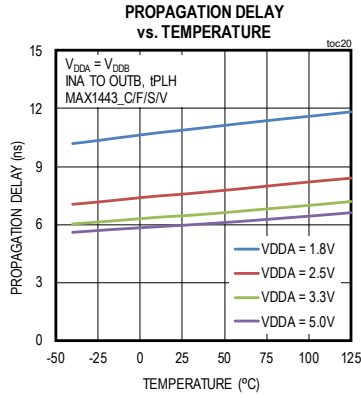
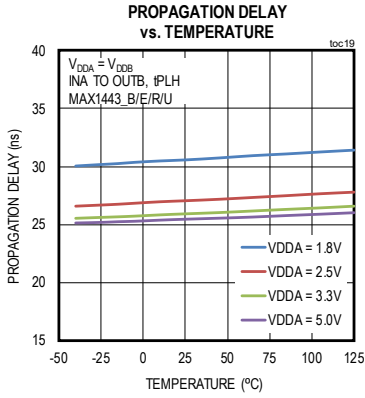
Typical Operating Characteristics (continued)

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)



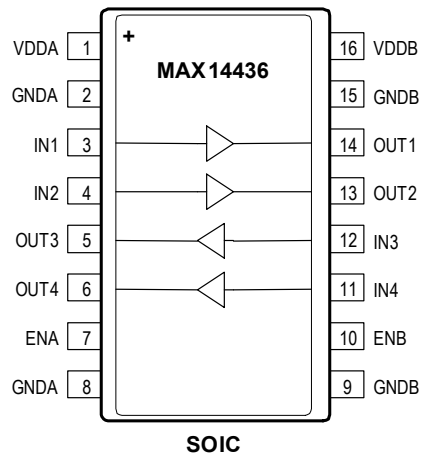
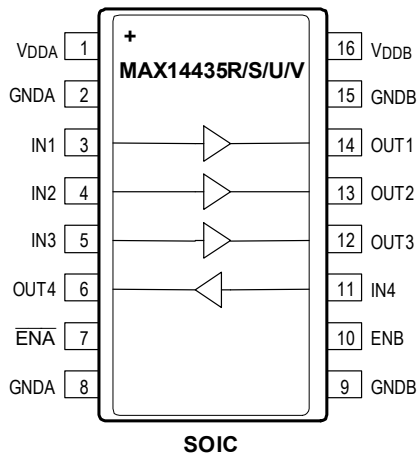
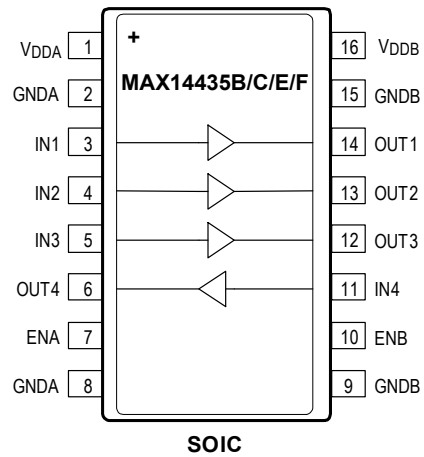
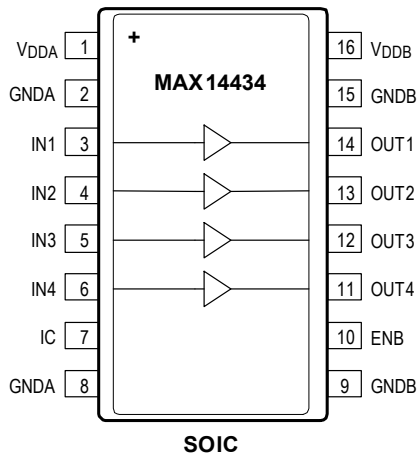
Typical Operating Characteristics (continued)

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)



Pin Configurations

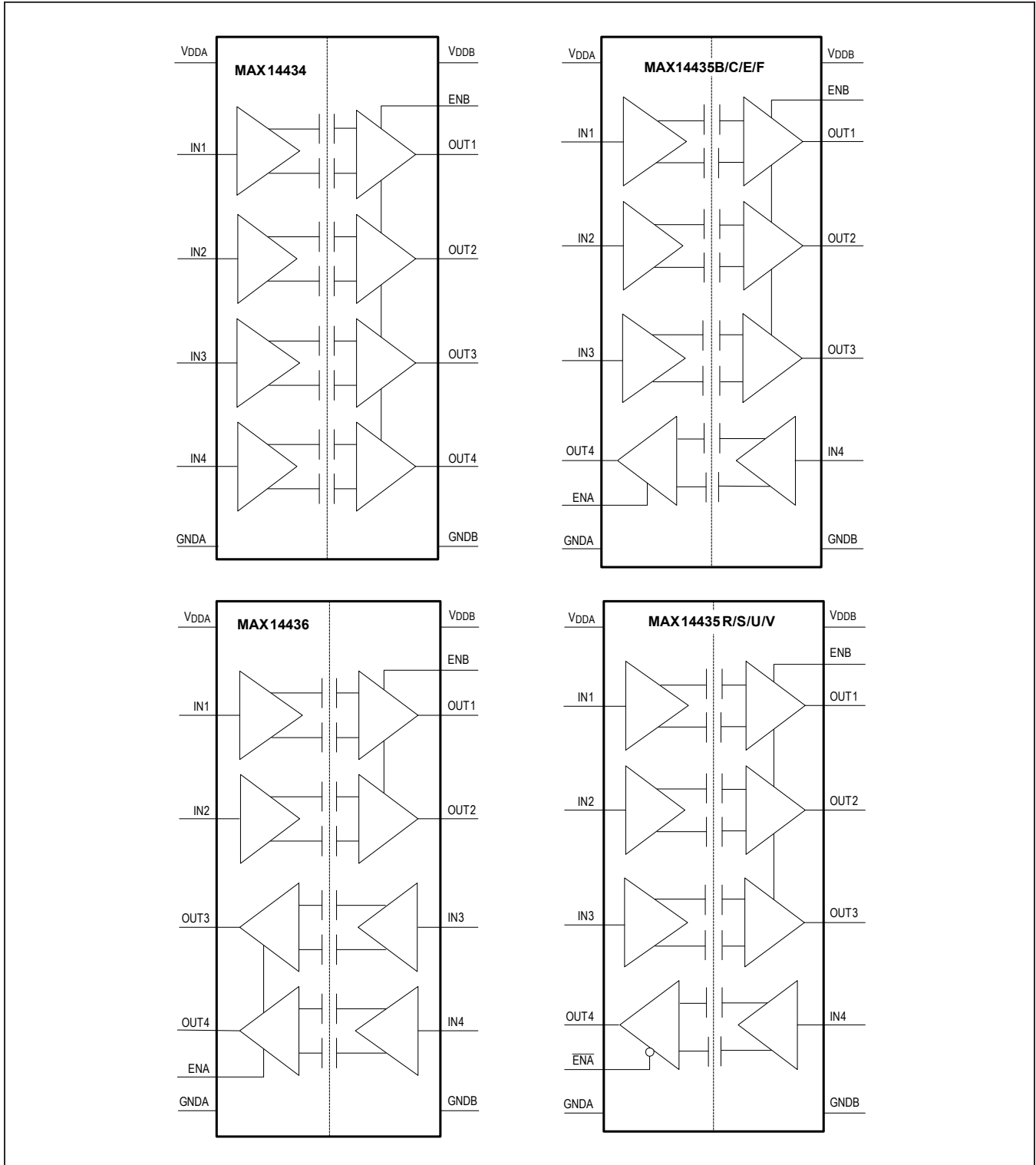
TOP VIEW



Pin Description

| NAME | PIN | | | | FUNCTION |
|-------------------------|----------|-----------------|-----------------|----------|--|
| | MAX14434 | MAX14435B/C/E/F | MAX14435R/S/U/V | MAX14436 | |
| V _{DDA} | 1 | 1 | 1 | 1 | Power Supply. Bypass V _{DDA} with a 0.1μF ceramic capacitor as close as possible to the pin. |
| GNDA | 2, 8 | 2, 8 | 2, 8 | 2, 8 | Ground Reference for Side A |
| IN1 | 3 | 3 | 3 | 3 | Logic Input 1 on Side A, corresponds to Logic Output 1 on Side B |
| IN2 | 4 | 4 | 4 | 4 | Logic Input 2 on Side A, corresponds to Logic Output 2 on Side B |
| IN3 | 5 | 5 | 5 | 12 | Logic Input 3 on Side A or B, corresponds to Logic Output 3 on Side B or A |
| IN4 | 6 | 11 | 11 | 11 | Logic Input 4 on Side A or B, corresponds to Logic Output 4 on Side B or A |
| I.C. | 7 | — | — | — | Internally Connected. Leave unconnected or connect to GNDA or V _{DDA} . |
| ENA | — | 7 | — | 7 | Active-High Enable for Side A. ENA has an internal 5μA pullup to V _{DDA} . |
| $\overline{\text{ENA}}$ | — | — | 7 | — | Active-Low Enable for Side A. $\overline{\text{ENA}}$ has an internal 5μA pullup to V _{DDA} . |
| OUT1 | 14 | 14 | 14 | 14 | Logic Output 1 on Side B |
| OUT2 | 13 | 13 | 13 | 13 | Logic Output 2 on Side B |
| OUT3 | 12 | 12 | 12 | 5 | Logic Output 3 on Side A or Side B |
| OUT4 | 11 | 6 | 6 | 6 | Logic Output 4 on Side A or Side B |
| ENB | 10 | 10 | 10 | 10 | Active-High Enable for Side B. ENB has an internal 5μA pullup to V _{DDB} . |
| GNDB | 9, 15 | 9, 15 | 9, 15 | 9, 15 | Ground Reference for Side B |
| V _{DDB} | 16 | 16 | 16 | 16 | Power Supply. Bypass V _{DDB} with a 0.1μF ceramic capacitor as close as possible to the pin. |

Functional Diagram



Detailed Description

The MAX14434–MAX14436 is a family of 4-channel digital isolators. The MAX14434–MAX14436 have an isolation rating of 5kV_{RMS}. The MAX14434–MAX14436 family offers all three possible unidirectional channel configurations to accommodate any 4-channel design, including SPI, RS-232, RS-485, and digital I/O applications. For applications requiring bidirectional channels, such as I²C, see the MAX14933 and MAX14937.

The MAX14434 features four channels transferring digital signals in one direction for applications such as isolated digital I/O. The MAX14435 has three channels transmitting data in one direction and one channel transmitting in the opposite direction, making it ideal for applications such as isolated SPI and RS-485 communication. The MAX14436 provides further design flexibility with two channels in each direction for isolated RS-232 or other applications.

Devices are available in the 16-pin wide-body SOIC package and are rated for up to 5kV_{RMS}. This family of digital isolators offers low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Maxim's proprietary process technology. The devices isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry.

Devices are available with a maximum data rate of either 25Mbps (B/E/R/U versions) or 200Mbps (C/F/S/V versions). Each device can be ordered with default-high or default-low outputs. The default is the state the output assumes when the input is not powered or if the input is open circuit. The devices have two supply inputs (V_{DDA} and V_{ddb}) that independently set the logic levels on either side of the device. V_{DDA} and V_{ddb} are referenced to GNDA and GNDB, respectively. The MAX14434–MAX14436 family also features a refresh circuit to ensure output accuracy when an input remains in the same state indefinitely.

Digital Isolation

The MAX14434–MAX14436 family provides galvanic isolation for digital signals that are transmitted between two ground domains. The devices withstand differences of up to 5kV_{RMS} for up to 60 seconds, and up to 1200V_{PEAK} of continuous isolation.

Level-Shifting

The wide supply voltage range of both V_{DDA} and V_{ddb} allows the MAX14434–MAX14436 family to be used for level translation in addition to isolation. V_{DDA} and V_{ddb} can be independently set to any voltage from 1.71V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

Unidirectional Channels

Each channel of the MAX14434–MAX14436 is unidirectional; it only passes data in one direction, as indicated in the functional diagram. Each device features four unidirectional channels that operate independently with guaranteed data rates from DC up to 25Mbps (B/E/R/U versions), or from DC to 200Mbps (C/F/S/V versions). The output driver of each channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Startup and Undervoltage-Lockout

The V_{DDA} and V_{ddb} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage condition is detected on either supply while the outputs are enabled, all outputs go to their default states regardless of the state of the inputs ([Table 2](#)). [Figure 2](#) through [Figure 5](#) show the behavior of the outputs during power-up and power-down.

Table 2. Output Behavior During Undervoltage Conditions

| V _{IN_} | V _{DDA} | V _{DDB} | ENA | ENB | V _{OUTA} | V _{OUTB} |
|------------------|------------------|------------------|-----|-----|-------------------|-------------------|
| 1 | Powered | Powered | 1 | 1 | 1 | 1 |
| | | | 0 | 0 | Hi-Z | Hi-Z |
| 0 | Powered | Powered | 1 | 1 | 0 | 0 |
| | | | 0 | 0 | Hi-Z | Hi-Z |
| X | Undervoltage | Powered | 1 | 1 | Default | Default |
| | | | 0 | 0 | Hi-Z | Hi-Z |
| X | Powered | Undervoltage | 1 | 1 | Default | Default |
| | | | 0 | 0 | Hi-Z | Hi-Z |

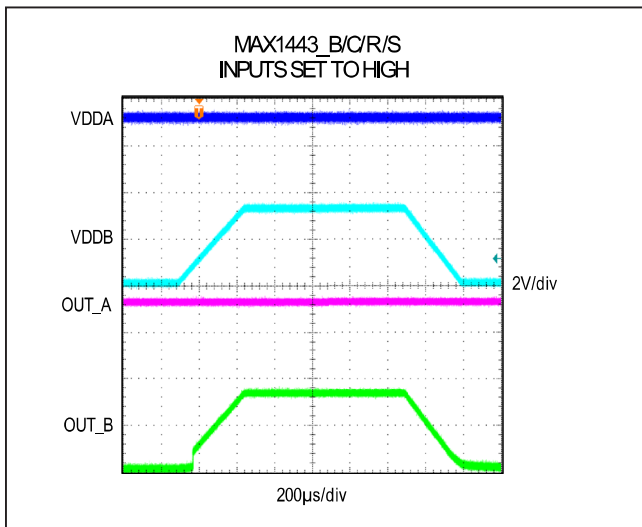


Figure 2. Undervoltage Lockout Behavior (MAX1443_B/C/R/S High)

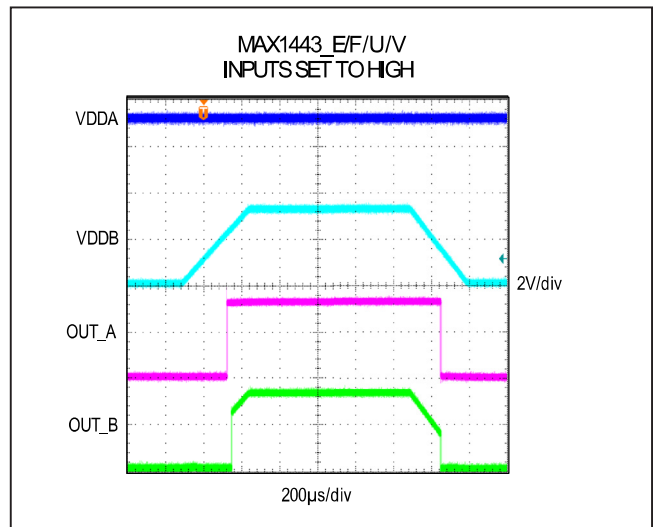


Figure 3. Undervoltage Lockout Behavior (MAX1443_E/F/U/V High)

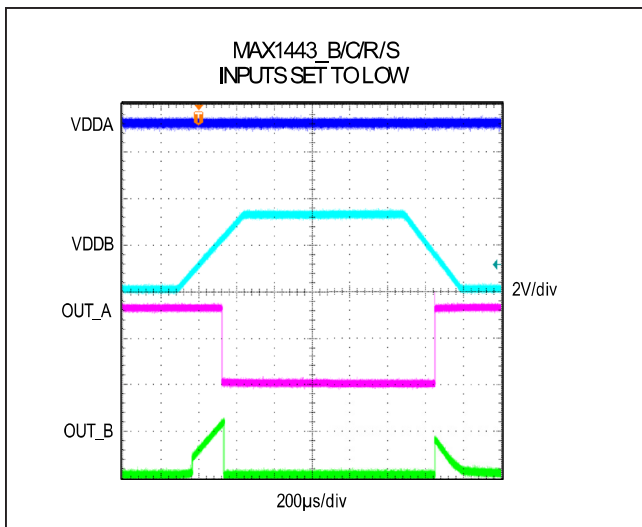


Figure 4. Undervoltage Lockout Behavior (MAX1443_B/C/R/S Low)

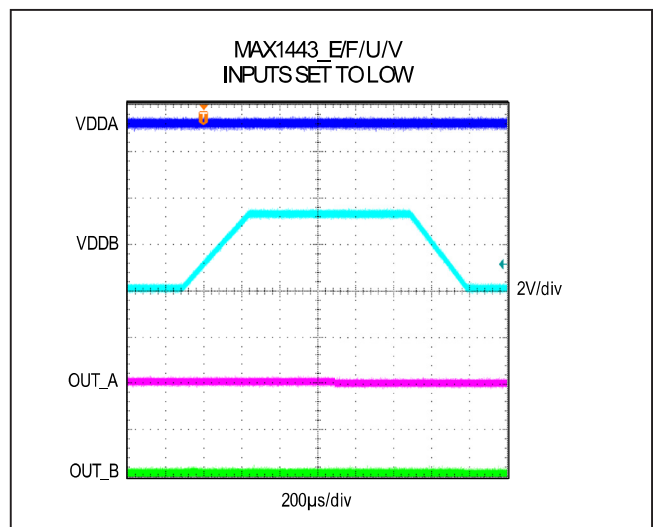


Figure 5. Undervoltage Lockout Behavior (MAX1443_E/F/U/V Low)

Applications Information

Power-Supply Sequencing

The MAX14434–MAX14436 do not require special power supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB}. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 0.1µF low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power supply input pins as possible.

Layout Considerations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. Avoid using vias to make low-inductance paths for the signals.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the MAX14434–MAX14436 free from ground and signal planes. Any galvanic or metallic connection between the field-side and logic-side defeats the isolation.

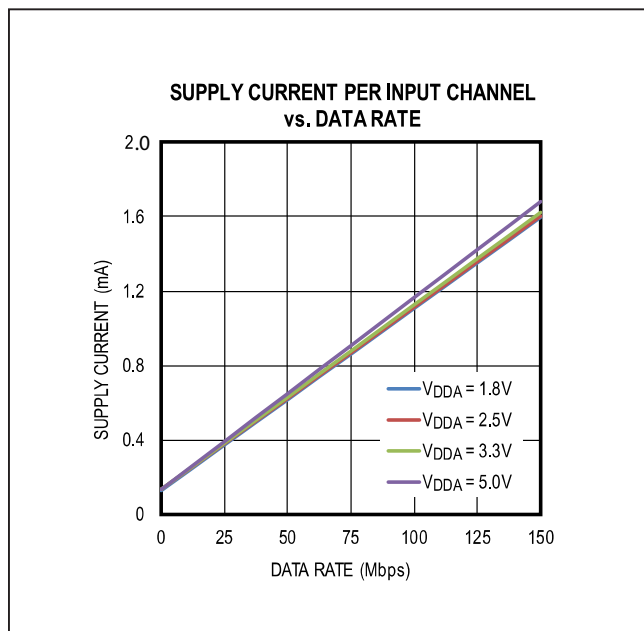


Figure 6. Supply Current Per Input Channel (Estimated)

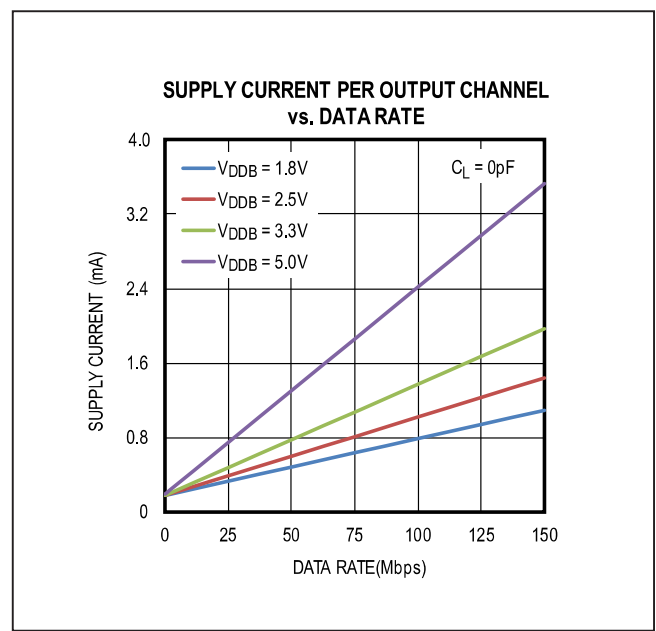


Figure 7. Supply Current Per Output Channel (Estimated)

Calculating Power Dissipation

The required current for a given supply (V_{DDA} or V_{DDB}) can be estimated by summing the current required for each channel. The supply current for a channel depends on whether the channel is an input or an output, the channel’s data rate, and the capacitive or resistive load if it is an output. The typical current for an input or output at any data rate can be estimated from the graphs in [Figure 6](#) and [Figure 7](#). Please note the data in [Figure 6](#) and [Figure 7](#) are extrapolated from the supply current measurements in a typical operating condition.

The total current for a single channel is the sum of the “no load” current (shown in [Figure 6](#) and [Figure 7](#)) which is a function of Voltage and Data Rate, and the “load current,” which depends on the type of load. Current into a capacitive load is a function of the load capacitance, the switching frequency, and the supply voltage.

$$I_{CL} = C_L \times f_{SW} \times V_{DD}$$

where

I_{CL} is the current required to drive the capacitive load.

C_L is the load capacitance on the isolator’s output pin.

f_{SW} is the switching frequency (bits per second / 2).

V_{DD} is the supply voltage on the output side of the isolator.

Current into a resistive load depends on the load resistance, the supply voltage and the average duty cycle of the data waveform. The DC load current can be conservatively estimated by assuming the output is always high.

$$I_{RL} = V_{DD} \div R_L$$

where

I_{RL} is the current required to drive the resistive load.

V_{DD} is the supply voltage on the output side of the isolator.

R_L is the load resistance on the isolator’s output pin.

Example (shown in [Figure 8](#)): A MAX14435F is operating with V_{DDA} = 2.5V, V_{DDB} = 3.3V, channel 1 operating at 20Mbps with a 10pF capacitive load, channel 2 held high with a 10kΩ resistive load, and channel 4 operating at 100Mbps with a 15pF capacitive load. Channel 3 is not in use and the resistive load is negligible since the isolator is driving a CMOS input. Refer to [Table 3](#) and [Table 4](#) for V_{DDA} and V_{DDB} supply current calculation worksheets.

V_{DDA} must supply:

- Channel 1 is an input channel operating at 2.5V and 20Mbps, consuming 0.33mA, estimated from [Figure 6](#).
- Channel 2 and 3 are input channels operating at 2.5V with DC signal, consuming 0.13mA, estimated from [Figure 6](#).
- Channel 4 is an output channel operating at 2.5V and 100Mbps, consuming 1.02mA, estimated from [Figure 7](#).
- I_{CL} on channel 4 for 15pF capacitor at 2.5V and 100Mbps is 1.875mA.

Total current for side A = 0.33 + 0.13 × 2 + 1.02 + 1.875 = 3.485mA, typical

V_{DDB} must supply:

- Channel 1 is an output channel operating at 3.3V and 20Mbps, consuming 0.42mA, estimated from [Figure 7](#).
- Channel 2 and 3 are output channels operating at 3.3V with DC signal, consuming 0.18mA, estimated from [Figure 7](#).
- Channel 4 is an input channel operating at 3.3V and 100Mbps, consuming 1.13mA, estimated from [Figure 6](#).
- I_{CL} on channel 1 for 10pF capacitor at 3.3V and 20Mbps is 0.33mA.
- I_{RL} on channel 2 for 10kΩ resistor held at 3.3V is 0.33mA.

Total current for side B = 0.42 + 0.18 × 2 + 1.13 + 0.33 + 0.33 = 2.57mA, typical

Table 3. Side A Supply Current Calculation Worksheet

| SIDE A | | V _{DDA} = 2.5V | | | | |
|----------------|--------|-------------------------|------------|------|------------------------|-------------------------------|
| Channel | IN/OUT | Data Rate (Mbps) | Load Type | Load | “No Load” Current (mA) | Load Current (mA) |
| 1 | IN | 20 | | | 0.33 | |
| 2 | IN | 0 | | | 0.13 | |
| 3 | IN | 0 | | | 0.13 | |
| 4 | OUT | 100 | Capacitive | 15pF | 1.02 | 2.5V x 50MHz x 15pF = 1.875mA |
| Total: 3.485mA | | | | | | |

Table 4. Side B Supply Current Calculation Worksheet

| SIDE B | | V _{DDB} = 3.3V | | | | |
|---------------|--------|-------------------------|------------|------|------------------------|--|
| Channel | IN/OUT | Data Rate (Mbps) | Load Type | Load | “No Load” Current (mA) | Load Current (mA) |
| 1 | OUT | 20 | Capacitive | 10pF | 0.42 | $3.3V \times 10MHz \times 10pF = 0.33mA$ |
| 2 | OUT | 0 | Resistive | 10kΩ | 0.18 | $3.3V / 10k\Omega = 0.33mA$ |
| 3 | OUT | 0 | | | 0.18 | |
| 4 | IN | 100 | | | 1.13 | |
| Total: 2.57mA | | | | | | |

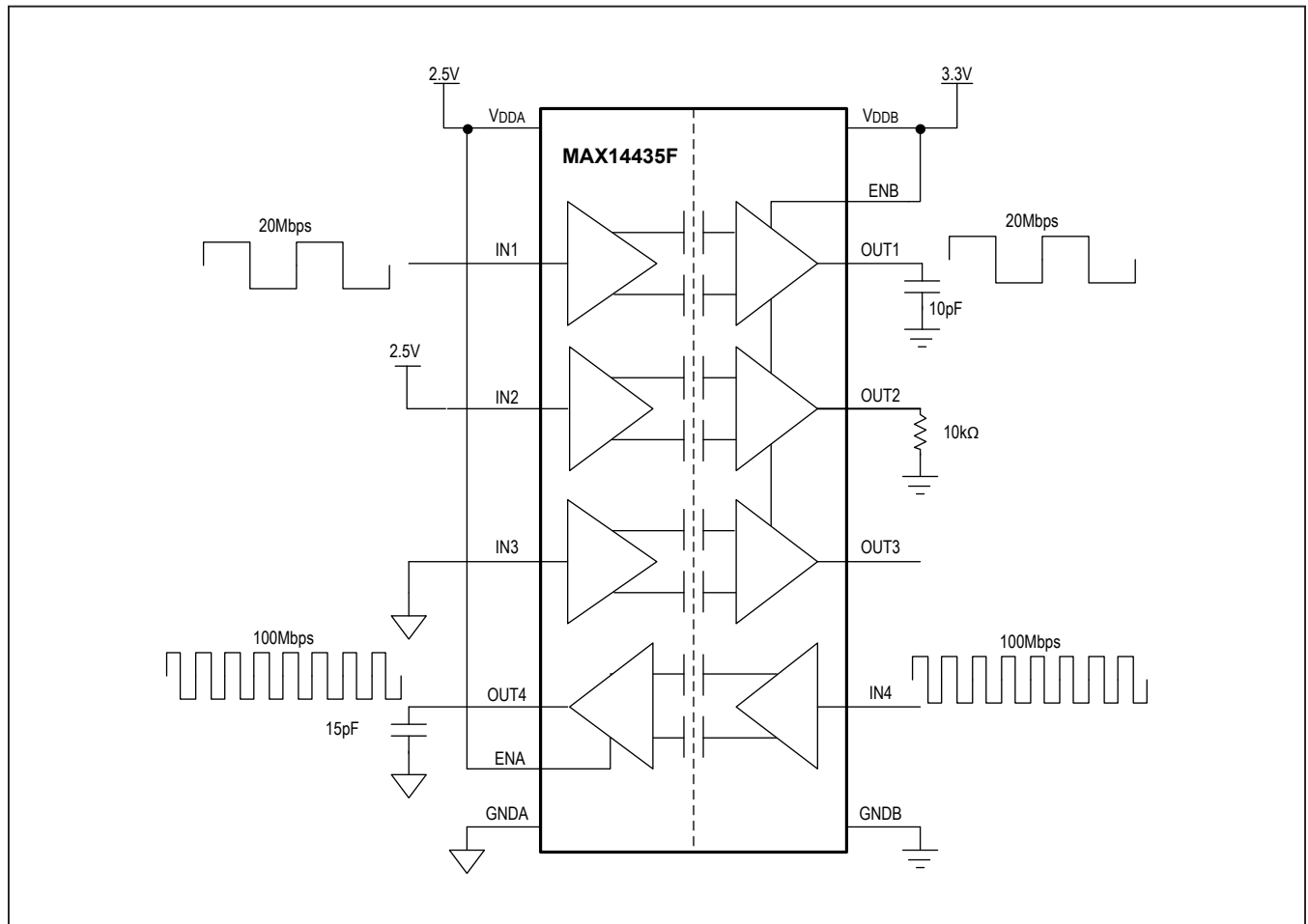
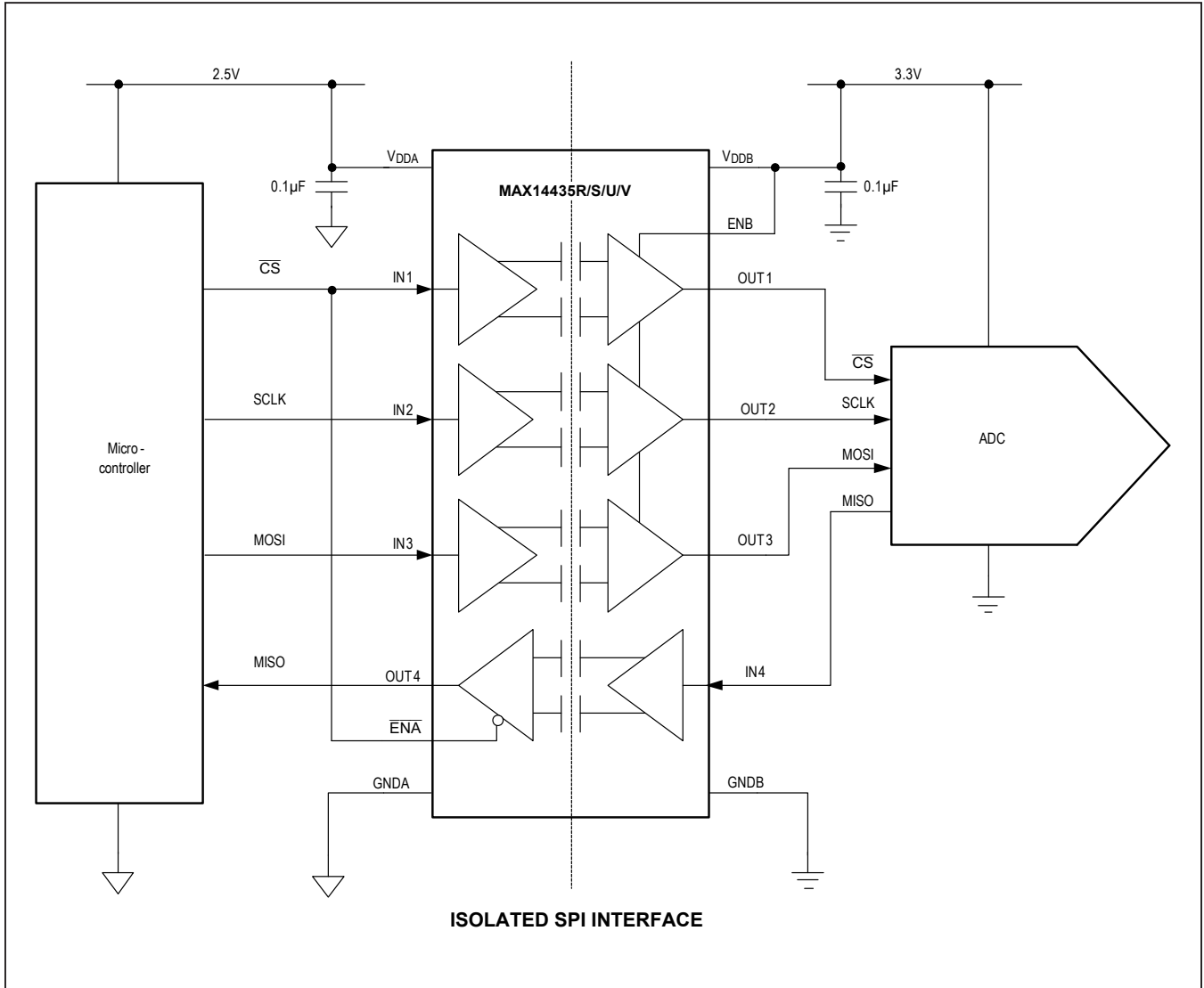
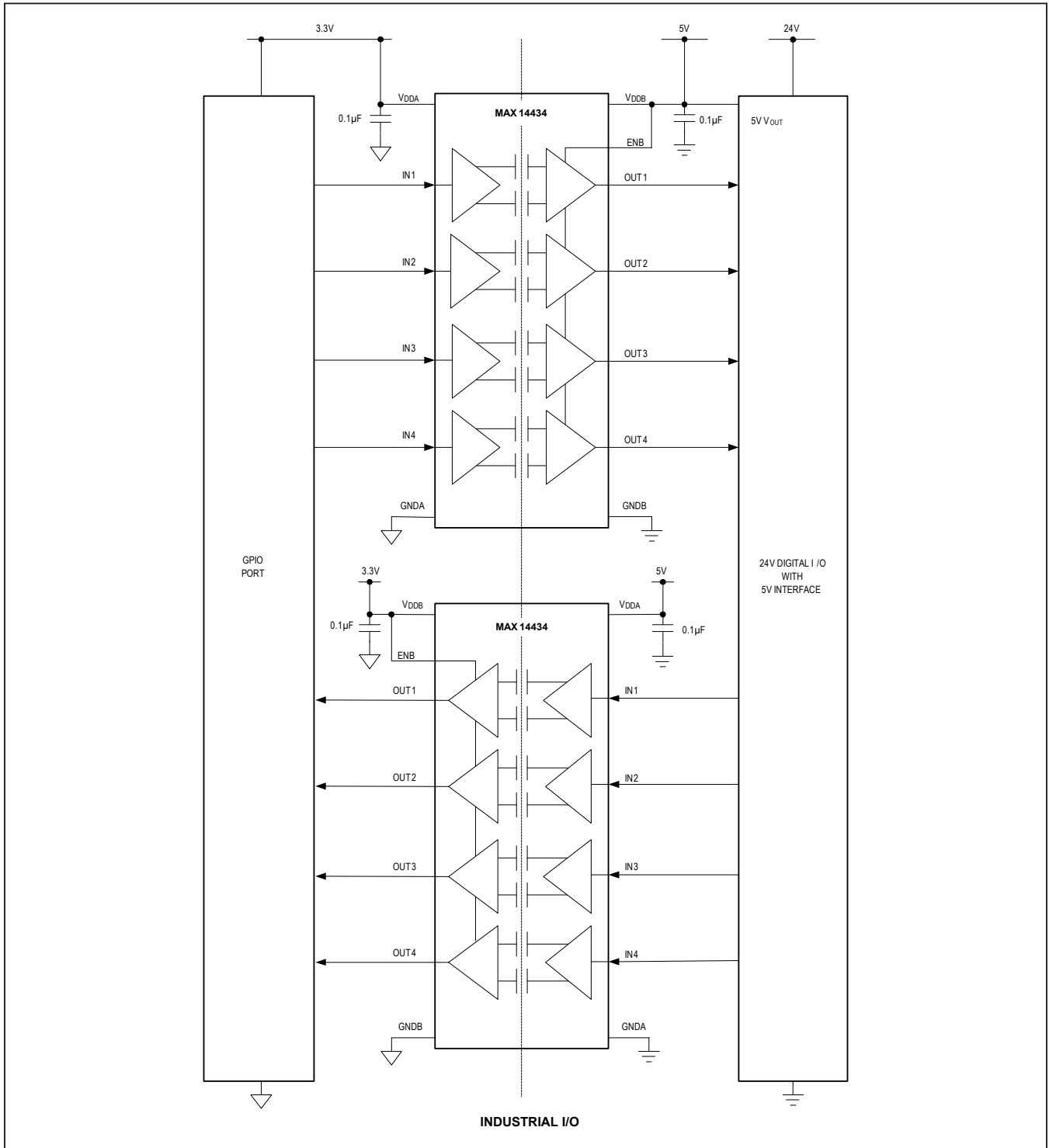


Figure 8. Example Circuit for Supply Current Calculation

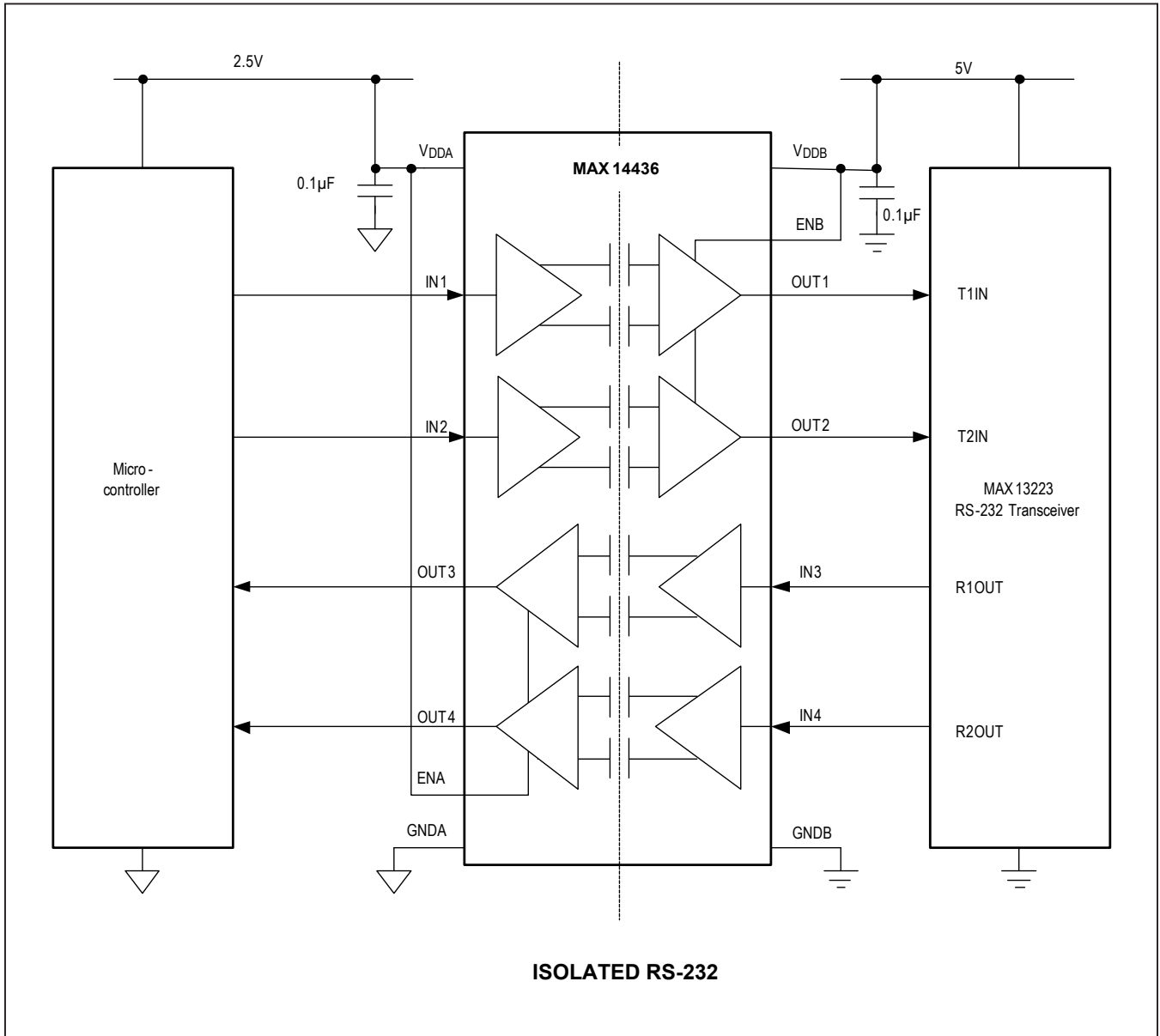
Typical Operating Circuit



Typical Operating Circuit (continued)



Typical Operating Circuit (continued)



Ordering Information

| PART | CHANNEL CONFIGURATION | DATA RATE (Mbps) | DEFAULT OUTPUT | ENA Polarity | ISOLATION VOLTAGE (kV _{RMS}) | TEMP RANGE (°C) | PIN-PACKAGE |
|------------------------|-----------------------|------------------|----------------|--------------|--|-----------------|--------------|
| MAX14434 BAWE+* | 4/0 | 25 | Default High | Active-High | 5.0 | -40 to +125 | 16 Wide SOIC |
| MAX14434CAWE+* | 4/0 | 200 | Default High | Active-High | 5.0 | -40 to +125 | 16 Wide SOIC |
| MAX14434EAWWE+* | 4/0 | 25 | Default Low | Active-High | 5.0 | -40 to +125 | 16 Wide SOIC |
| MAX14434FAWE+ | 4/0 | 200 | Default Low | Active-High | 5.0 | -40 to +125 | 16 Wide SOIC |
| MAX14435 BAWE+* | 3/1 | 25 | Default High | Active-High | 5.0 | -40 to +125 | 16 Wide SOIC |
| MAX14435CAWE+* | 3/1 | 200 | Default High | Active-High | 5.0 | -40 to +125 | 16 Wide SOIC |
| MAX14435EAWWE+* | 3/1 | 25 | Default Low | Active-High | 5.0 | -40 to +125 | 16 Wide SOIC |
| MAX14435FAWE+ | 3/1 | 200 | Default Low | Active-High | 5.0 | -40 to +125 | 16 Wide SOIC |
| MAX14435RAWWE+* | 3/1 | 25 | Default High | Active-Low | 5.0 | -40 to +125 | 16 Wide SOIC |
| MAX14435SAWE+* | 3/1 | 200 | Default High | Active-Low | 5.0 | -40 to +125 | 16 Wide SOIC |
| MAX14435UAWWE+* | 3/1 | 25 | Default Low | Active-Low | 5.0 | -40 to +125 | 16 Wide SOIC |
| MAX14435VAWE+* | 3/1 | 200 | Default Low | Active-Low | 5.0 | -40 to +125 | 16 Wide SOIC |
| MAX14436 BAWE+* | 2/2 | 25 | Default High | Active-High | 5.0 | -40 to +125 | 16 Wide SOIC |
| MAX14436CAWE+* | 2/2 | 200 | Default High | Active-High | 5.0 | -40 to +125 | 16 Wide SOIC |
| MAX14436EAWWE+* | 2/2 | 25 | Default Low | Active-High | 5.0 | -40 to +125 | 16 Wide SOIC |
| MAX14436FAWE+ | 2/2 | 200 | Default Low | Active-High | 5.0 | -40 to +125 | 16 Wide SOIC |

*Future Product—Contact Maxim for availability.

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|--|---------------|
| 0 | 6/17 | Initial release | — |
| 1 | 8/17 | Updated <i>Insulation Characteristics</i> table | 10 |
| 2 | 1/18 | Updated <i>Ordering Information</i> table | 25 |
| 3 | 1/19 | Removed future product designation from MAX14434FAWE+ in the <i>Ordering Information</i> table | 24 |

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