

247/15

54/74126
54LS/74LS126
QUAD BUS BUFFER GATE
 (With 3-State Outputs)

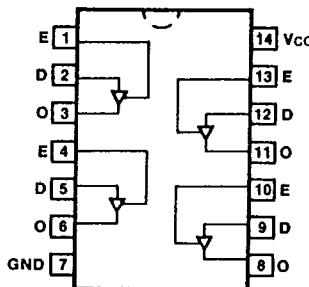
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V _{CC} = +5.0 V ±5%, T _A = 0°C to +70°C	V _{CC} = +5.0 V ±10%, T _A = -55°C to +125°C	
Plastic DIP (P)	A	74126PC, 74LS126PC		9A
Ceramic DIP (D)	A	74126DC, 74LS126DC	54126DM, 54LS126DM	6A
Flatpak (F)	A	74126FC, 74LS126FC	54126FM, 54LS126FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	0.5/0.25
Outputs	130/10 (50)	65/15 (25)/(7.5)

CONNECTION DIAGRAM
PINOUT A



TRUTH TABLE

INPUTS		OUTPUT
E	D	
H	L	L
H	H	H
L	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74		54/74LS		UNITS	CONDITIONS	
		Min	Max	Min	Max			
V _{OH}	Output HIGH Voltage	XM	2.4		2.4	V	V _{CC} = Min, V _{IN} = V _{IH} or V _{IL}	
			XC	2.4				
			XM					2.4
			XC					2.4
I _{OS}	Output Short Circuit Current	XM	-30 -70	-30 -130	mA	V _{CC} = Max		
XC	-28 -70	-30 -130						
I _{CC}	Power Supply Current		62	24	mA	Outputs LOW, V _E = 4.5 V	V _{CC} = Max V _{IN} = Gnd	
				20		Outputs OFF, V _E = 0 V		
t _{PLH}	Propagation Delay		13	15	ns	Figs. 3-3, 3-5		
t _{PHL}	Data to Output		18	18				
t _{pZH}	Output Enable Time		18	20	ns	Figs. 3-3, 3-11, 3-12		
t _{pZL}			25	30				
t _{PLZ}	Output Disable Time		16	30	ns	Figs. 3-3, 3-11, 3-12		
t _{PHZ}			18	30				

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.