FAIRCHILD SEMICONDUCTOR®

December 2010

NC7SP04 — TinyLogic® ULP Inverter

Features

- 0.9V to 3.6V V_{CC} Supply Operation
- 3.6V Over-Voltage Tolerant I/Os at V_{CC} from 0.9V to 3.6V
- Propagation Delay (t_{PD}):
  - 4.0ns Typical for 3.0V to 3.6V V_{CC}
  - 5.0ns Typical for 2.3V to 2.7V V_{CC}
  - 6.0ns Typical for 1.65V to 1.95V V_{CC}
  - 7.0ns Typical for 1.40V to 1.60V V_{CC}
  - 11.0ns Typical for 1.10V to 1.30V V_{CC}
  - 27.0ns Typical for 0.90V V_{CC}
- Power-Off High-Impedance Inputs and Outputs
- Static Drive (I_{OH}/I_{OL}):
  - ± 2.6mA at 3.00V V_{CC}
  - ± 2.1mA at 2.30V V_{CC}
  - ± 1.5mA at 1.65V V_{CC}
  - ± 1.0mA at 1.40V V_{CC}
  - ± 0.5mA at 1.10V V_{CC}
  - ± 20μA at 0.9V V_{CC}
- Quiet Series™ Noise / EMI Reduction Circuitry
- Ultra Small MicroPak™ Packages
- Ultra Low Dynamic Power

Description

The NC7SP04 is a single inverter from Fairchild's Ultra Low Power (ULP) series of TinyLogic®. Ideal for applications where battery life is critical, this product is designed for ultra low power consumption within the V_{CC} operating range of 0.9V to 3.6V.

The internal circuit is composed of a minimum of inverter stages, including the output buffer, to enable ultra low static and dynamic power.

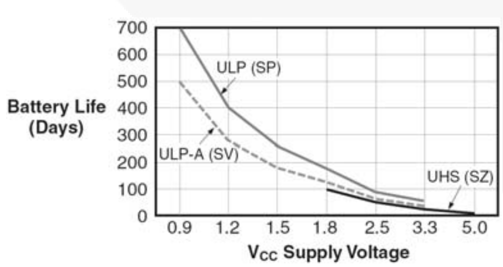
The NC7SP04, for lower drive requirements, is uniquely designed for optimized power and speed and is fabricated with an advanced CMOS technology to achieve best-in-class speed of operation, while maintaining extremely low CMOS power dissipation.

Related Resources

- AN-5055 — Portability and Ultra Low Power TinyLogic®

Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7SP04P5X	P04	5-Lead SC70, EIAJ SC-88a, 1.25mm Wide	3000 Units on Tape & Reel
NC7SP04L6X	J6	6-Lead MicroPak™, 1.00mm Wide	5000 Units on Tape & Reel
NC7SP04FHX	J6	6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch	5000 Units on Tape & Reel



Notes:
1. TinyLogic ULP and ULP-A with up to 50% less power consumption can extend battery life significantly.
2. Battery Life=($V_{battery}$ x $I_{battery}$ x 0.9) / (P_{device}) / 24hrs/day; where, P_{device}=(I_{CC} x V_{CC}) + (C_{PD} + C_L) x V_{CC}^2 x f.
3. Assumes ideal 3.6V Lithium Ion battery with current rating of 900mAH and derated 90% and device frequency at 10MHz, with C_L=15pF load.

Figure 1. Battery Life vs. V_{CC} Supply Voltage

Connection Diagrams

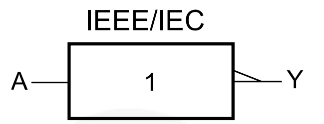


Figure 2. Logic Symbol

Pin Configurations

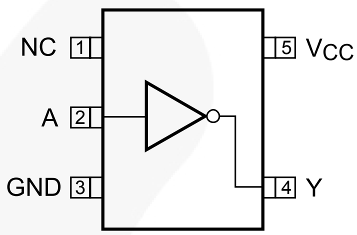


Figure 3. SC70 (Top View)

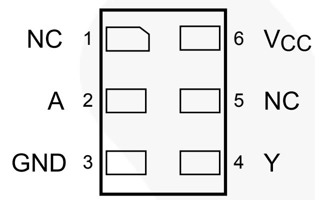


Figure 4. MicroPak™ (Top Through View)

Function Table

Inputs	Output
A	**Y**
L	H
H	L

L = Low Logic Level
H = High Logic Level

Pin Definitions

Pin # SC70	Pin # MicroPak™	Name	Description
1	1, 5	NC	No Connect
2	2	A	Input
3	3	GND	Ground
4	4	Y	Output
5	6	V_{CC}	Supply Voltage

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	4.6	V
V_{IN}	DC Input Voltage		-0.5	4.6	V
V_{OUT}	DC Output Voltage	HIGH or LOW State(4)	-0.5	V_{CC} to +0.5	V
		V_{CC}=0V	-0.5	4.6	V
I_{IK}	DC Input Diode Current at V_{IN} < 0V			-50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0V		-50	mA
		V_{OUT} > V_{CC}		+50	
I_{OH} / I_{OL}	DC Output Source/Sink Current			±50	mA
I_{CC} or Ground	DC V_{CC} or Ground Current per Supply Pin			±50	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature Under Bias			+150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)			+260	°C
P_D	Power Dissipation at +85°C	SC70-5		150	mW
		MicroPak™-6		130	
		MicroPak2™-6		120	
ESD	Human Body Model	JEDEC: JESD22-A114		4000	V
	Charged Device Model	JEDEC: JESD22-C101		2000	

Note:
4. The I_O maximum rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage		0.9	3.6	V
V_{IN}	Input Voltage(5)		0	3.6	V
V_{OUT}	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		V_{CC}=0V	0	3.6	
I_{OH} / I_{OL}	Output Current in I_{OH} / I_{OL}	V_{CC}=3.0V to 3.6V		±2.6	mA
		V_{CC}=2.3V to 2.7V		±2.1	
		V_{CC}=1.65V to 1.95V		±1.5	
		V_{CC}=1.40V to 1.60V		±1.0	
		V_{CC}=1.10V to 1.30V		±0.5	
		V_{CC}=0.9V		20.0	µA
T_A	Free Air Operating Temperature		-40	+85	°C
$\Delta t / \Delta V$	Minimum Input Edge Rate	V_{IN}=0.8V to 2.0V, V_{CC}=3.0V		10	ns/V
θ_{JA}	Thermal Resistance	SC70-5		425	°C/W
		MicroPak™-6		500	
		MicroPak2™-6		560	

Note:
5. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=25°C		T_A=-40 to 85°C		Units
				Min.	Max.	Min.	Max.	
V_{IH}	HIGH Level Input Voltage	0.90		0.65 x V_{CC}		0.65 x V_{CC}		V
		1.10 ≤ V_{CC} ≤ 1.30		0.65 x V_{CC}		0.65 x V_{CC}		
		1.40 ≤ V_{CC} ≤ 1.60		0.65 x V_{CC}		0.65 x V_{CC}		
		1.65 ≤ V_{CC} ≤ 1.95		0.65 x V_{CC}		0.65 x V_{CC}		
		2.30 ≤ V_{CC} ≤ 2.70		1.6		1.6		
		3.00 ≤ V_{CC} ≤ 3.60		2.1		2.1		
V_{IL}	LOW Level Input Voltage	0.90			0.35 x V_{CC}		0.35 x V_{CC}	V
		1.10 ≤ V_{CC} ≤ 1.30			0.35 x V_{CC}		0.35 x V_{CC}	
		1.40 ≤ V_{CC} ≤ 1.60			0.35 x V_{CC}		0.35 x V_{CC}	
		1.65 ≤ V_{CC} ≤ 1.95			0.35 x V_{CC}		0.35 x V_{CC}	
		2.30 ≤ V_{CC} ≤ 2.70			0.7		0.7	
		3.00 ≤ V_{CC} ≤ 3.60			0.9		0.9	
V_{OH}	HIGH Level Output Voltage	0.90	I_{OH}=-20µA	V_{CC} - 0.1		V_{CC} - 0.1		V
		1.10 ≤ V_{CC} ≤ 1.30		V_{CC} - 0.1		V_{CC} - 0.1		
		1.40 ≤ V_{CC} ≤ 1.60		V_{CC} - 0.1		V_{CC} - 0.1		
		1.65 ≤ V_{CC} ≤ 1.95		V_{CC} - 0.1		V_{CC} - 0.1		
		2.30 ≤ V_{CC} ≤ 2.70		V_{CC} - 0.1		V_{CC} - 0.1		
		3.00 ≤ V_{CC} ≤ 3.60		V_{CC} - 0.1		V_{CC} - 0.1		
		1.10 ≤ V_{CC} ≤ 1.30	I_{OH}=-0.5mA	0.75 x V_{CC}		0.75 x V_{CC}		
		1.40 ≤ V_{CC} ≤ 1.60	I_{OH}=-1mA	1.07		0.99		
		1.65 ≤ V_{CC} ≤ 1.95	I_{OH}=-1.5mA	1.24		1.22		
		2.30 ≤ V_{CC} ≤ 2.70	I_{OH}=-2.1mA	1.95		1.87		
		3.00 ≤ V_{CC} ≤ 3.60	I_{OH}=-2.6mA	2.61		2.55		
V_{OL}	LOW Level Output Voltage	0.90	I_{OL}=20µA		0.1		0.1	V
		1.10 ≤ V_{CC} ≤ 1.30			0.1		0.1	
		1.40 ≤ V_{CC} ≤ 1.60			0.1		0.1	
		1.65 ≤ V_{CC} ≤ 1.95			0.1		0.1	
		2.30 ≤ V_{CC} ≤ 2.70			0.1		0.1	
		3.00 ≤ V_{CC} ≤ 3.60			0.1		0.1	
		1.10 ≤ V_{CC} ≤ 1.30	I_{OL}=0.5mA		0.30 x V_{CC}		0.30 x V_{CC}	
		1.40 ≤ V_{CC} ≤ 1.60	I_{OL}=1mA		0.31		0.37	
		1.65 ≤ V_{CC} ≤ 1.95	I_{OL}=1.5mA		0.31		0.35	
		2.30 ≤ V_{CC} ≤ 2.70	I_{OL}=2.1mA		0.31		0.33	
		3.00 ≤ V_{CC} ≤ 3.60	I_{OL}=2.6mA		0.31		0.33	
I_{IN}	Input Leakage Current	0.90 to 3.60	0 ≤ V_I ≤ 3.6V		±0.1		±0.5	µA
I_{OFF}	Power Off	0	0 ≤ (V_O, V_I) ≤ 3.6V		0.5		0.5	µA
I_{CC}	Quiescent Supply Current	0.90 to 3.60	V_{IN}=V_{CC} or GND		0.9		0.9	µA

AC Electrical Characteristics

Symbol	Parameter	V_{CC}	Conditions	T_A=25°C			T_A=-40 to 85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{PHL}, t_{PLH}	Propagation Delay	0.90	C_L=10pF, R_L=1MΩ		27.0				ns	Figure 1, Figure 2
		$1.10 \le V_{CC} \le 1.30$		3.5	11.0	21.8	3.0	34.3		
		$1.40 \le V_{CC} \le 1.60$		2.5	7.0	14.8	2.0	15.0		
		$1.65 \le V_{CC} \le 1.95$		2.0	6.0	12.0	1.5	12.2		
		$2.30 \le V_{CC} \le 2.70$		1.5	5.0	9.4	1.0	9.9		
		$3.00 \le V_{CC} \le 3.60$		1.0	4.0	8.3	1.0	9.0		
		0.90	C_L=15pF, R_L=1MΩ		30.0					
		$1.10 \le V_{CC} \le 1.30$		4.0	11.0	22.8	3.5	37.3		
		$1.40 \le V_{CC} \le 1.60$		3.0	8.0	15.5	2.5	16.5		
		$1.65 \le V_{CC} \le 1.95$		2.5	6.0	12.6	2.0	13.6		
		$2.30 \le V_{CC} \le 2.70$		2.0	5.0	9.9	1.5	10.8		
		$3.00 \le V_{CC} \le 3.60$		1.5	4.0	8.7	1.0	9.5		
		0.90	C_L=30pF, R_L=1MΩ		32.0					
		$1.10 \le V_{CC} \le 1.30$		5.0	13.0	25.9	4.0	46.3		
		$1.40 \le V_{CC} \le 1.60$		4.0	9.0	17.8	3.5	18.2		
		$1.65 \le V_{CC} \le 1.95$		3.0	7.0	14.4	2.0	15.9		
		$2.30 \le V_{CC} \le 2.70$		2.0	6.0	11.3	1.5	12.8		
		$3.00 \le V_{CC} \le 3.60$		1.5	5.0	9.2	1.0	10.7		
C_{IN}	Input Capacitance	0			2				pF	
C_{PD}	Power Dissipation Capacitance	0.90 to 3.60	V_{IN}=0V or V_{CC}, f=10MHz		8				pF	

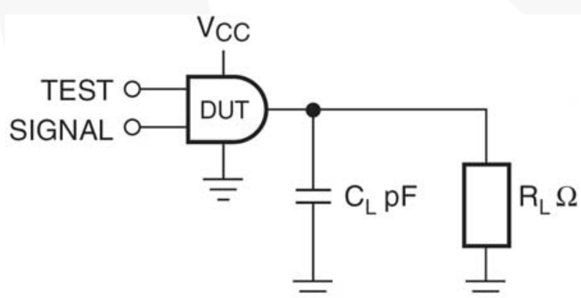


Figure 5. AC Test Circuit

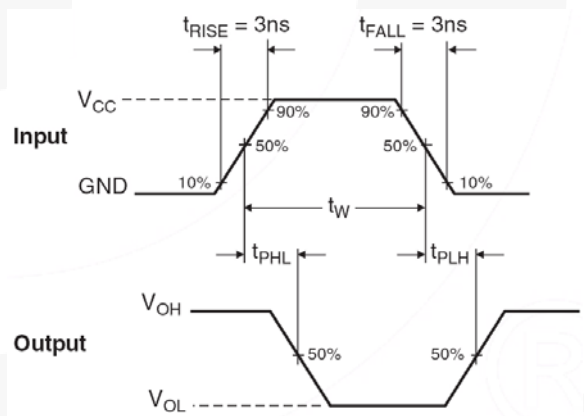


Figure 6. AC Waveforms

Symbol	V_{CC}					
	3.3V ± 0.3V	2.5V ± 0.2V	1.8V ± 0.15V	1.5V ± 0.1V	1.2V ± 0.1V	0.9V
V_{mi}	1.5V	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2
V_{mo}	1.5V	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2	V_{CC} / 2

Physical Dimensions

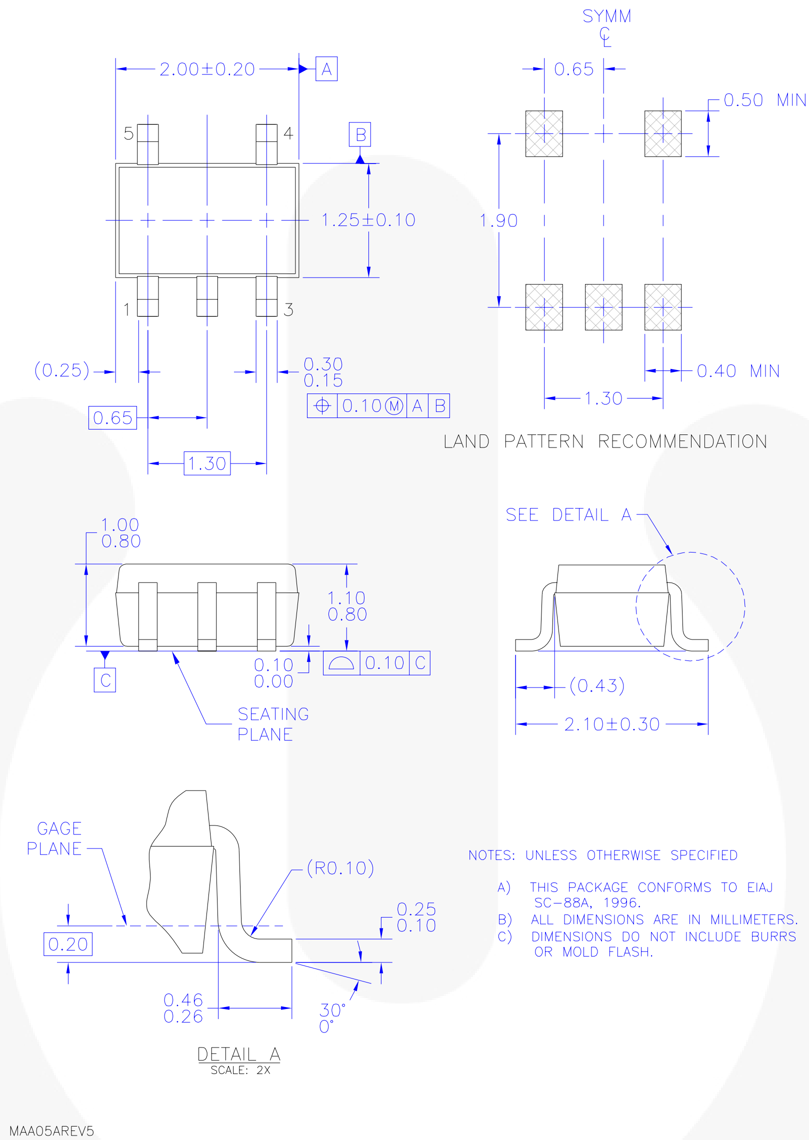


Figure 7. 5-Lead, SC70, EIAJ SC-88a, 1.25mm Wide

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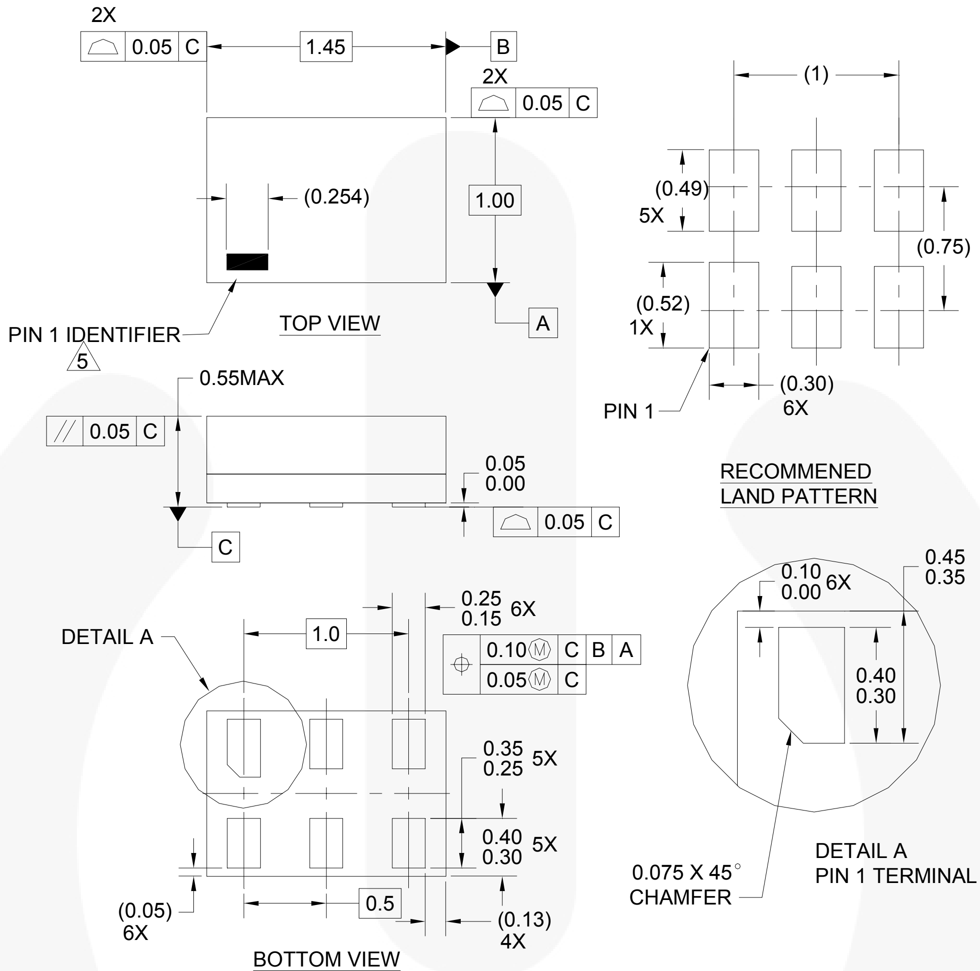
Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/analog/pdf/sc70-5_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
P5X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994
4. FILENAME AND REVISION: MAC06AREV4
5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

Figure 8. 6-Lead, MicroPak™, 1.0mm Wide

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Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions

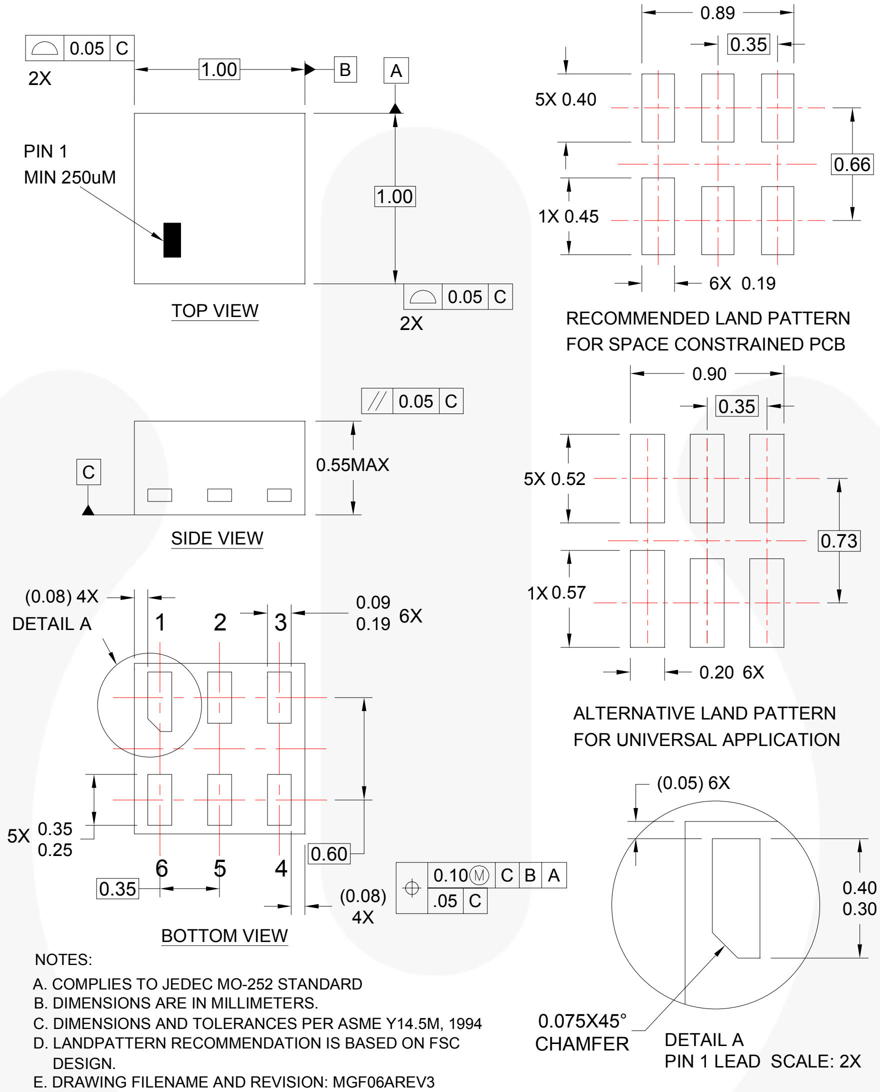

Figure 9. 6-Lead, MicroPak2™, 1x1mm Body, .35mm Pitch

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Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/packaging/MicroPAK2_6L_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

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SuperSOT™-8
SupreMOS®
SyncFET™
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The Right Technology for Your Success™
the power franchise®
TinyBoost™
TinyBuck™
TinyCalc™
TinyLogic®
TINYOPTO™
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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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