



1M (128K x 8) Static RAM

Features

- High speed: 55 ns and 70 ns
- Wide voltage range: 2.7V–3.6V
- Low active power and standby power
- Easy memory expansion with \overline{CE}_1 , CE_2 and \overline{OE} features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Package is available in a standard 450-mil-wide 32-lead SOIC, 32-lead TSOP-I, 32-lead reverse TSOP-1, and 32-lead STSOP-1 package

Functional Description^[1]

The CY62128V is composed of high-performance CMOS static RAMs organized as 128K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}_1), an active HIGH Chip Enable (CE_2), an active LOW Output

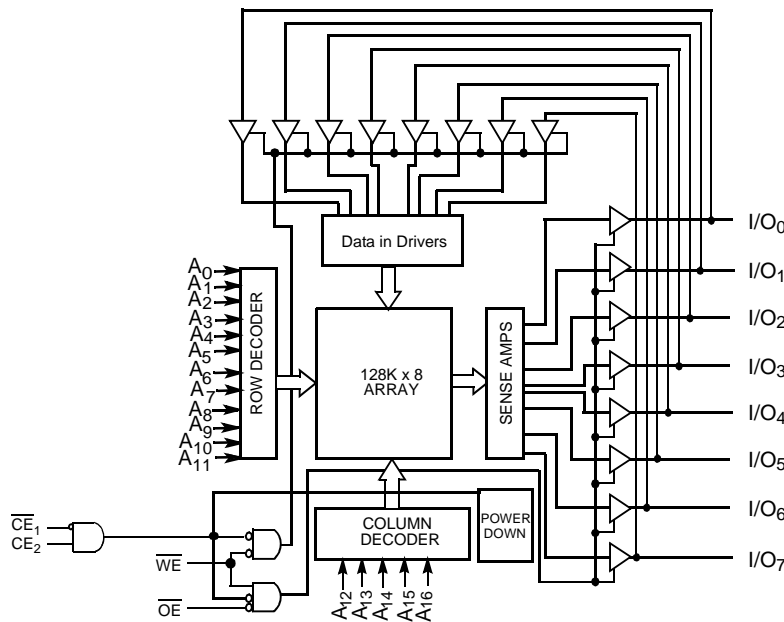
Enable (\overline{OE}) and three-state drivers. These devices have an automatic power-down feature, reducing the power consumption by over 99% when deselected.

Writing to the device is accomplished by taking Chip Enable one (\overline{CE}_1) and Write Enable (\overline{WE}) inputs LOW and the Chip Enable two (CE_2) input HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{16}).

Reading from the device is accomplished by taking Chip Enable one (\overline{CE}_1) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) and Chip Enable two (CE_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

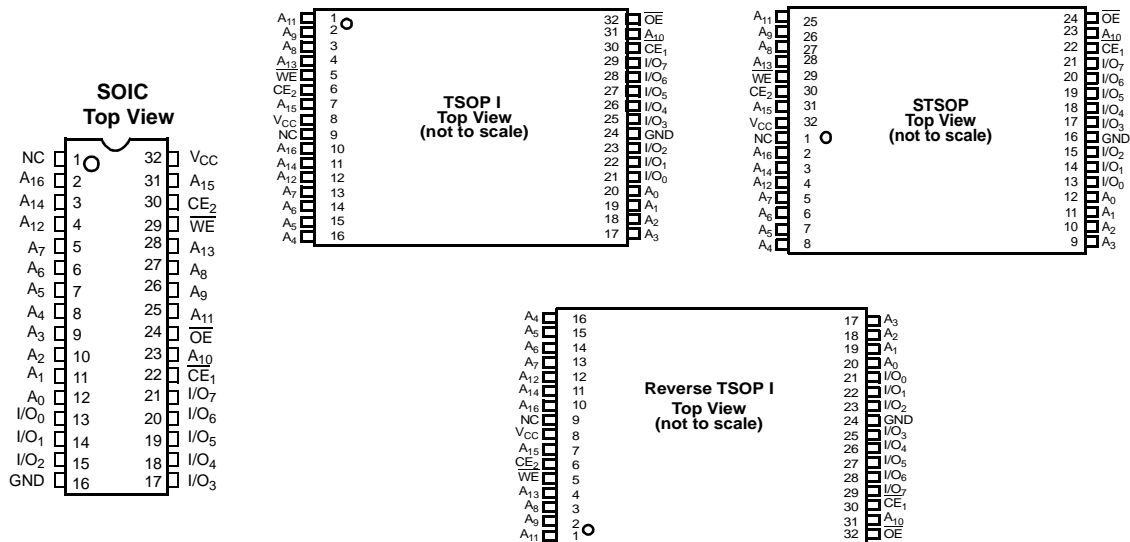
The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected (\overline{CE}_1 HIGH or CE_2 LOW), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW).

Logic Block Diagram



Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Pin Configurations

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) -0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State^[2] -0.5V to V_{CC} + 0.5V

DC Input Voltage^[2] -0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	2.7V to 3.6V
Industrial	-40°C to +85°C	2.7V to 3.6V

Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation (Commercial)			
	Min.	Typ. ^[3]	Max.		Operating I _{CC} (mA)		Standby I _{SB2} (µA)	
					Typ. ^[3]	Maximum	Typ. ^[3]	Maximum
CY62128VLL	2.7	3.0	3.6	70	20	40	0.4	100
				55				

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62128V-55/70			Unit
			Min.	Typ. ^[3]	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -1.0 mA	2.4			V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA			0.4	V
V _{IH}	Input HIGH Voltage		2		V _{CC} + 0.5V	V
V _{IL}	Input LOW Voltage		-0.5		0.8	V

Notes:

2. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.

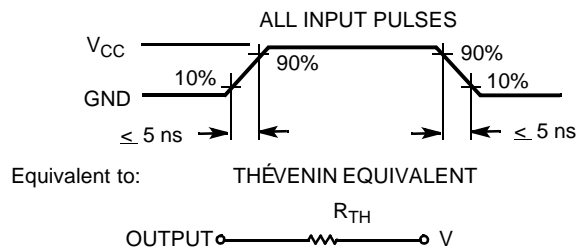
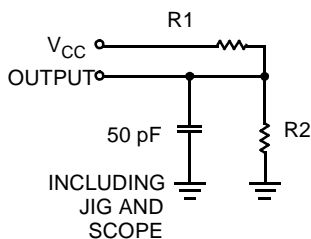
3. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ., T_A = 25°C.

Electrical Characteristics Over the Operating Range (continued)

Parameter	Description	Test Conditions	CY62128V-55/70			Unit
			Min.	Typ. ^[3]	Max.	
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1		1	μA
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled	-1		1	μA
I_{CC}	V_{CC} Operating Supply Current	$V_{CC} = \text{Max.}$, $I_{OUT} = 0 \text{ mA}$, $f = f_{MAX} = 1/t_{RC}$	Com'l, 70 ns	20	40	mA
			Ind'l, 55 ns	23	50	
			Ind'l, 70 ns	20	40	
I_{SB1}	Automatic CE Power-down Current—TTL Inputs	Max. V_{CC} , $\overline{CE}_1 \geq V_{IH}$, $CE_2 < V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	Com'l, 70 ns	15	300	μA
			Com'l, 55 ns	17	350	
			Ind'l, 70ns	15	300	
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	Max. V_{CC} , $\overline{CE}_1 \geq V_{CC} - 0.3V$, $CE_2 < V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$, $f = 0$	Com'l	0.4	15	μA
			Ind'l		30	

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ C$, $f = 1 \text{ MHz}$, $V_{CC} = 3.0V$	6	pF
C_{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms


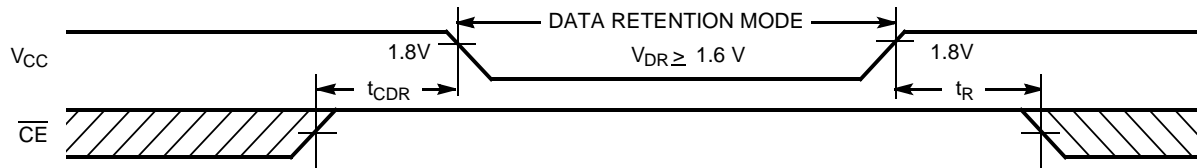
Parameters	3.3V	Unit
R1	1213	Ohms
R2	1378	Ohms
R_{TH}	645	Ohms
V_{TH}	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions ^[5]	Min.	Typ. ^[3]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.6			V
I_{CCDR}	Data Retention Current	Com'l	$V_{CC} = 2V$, $\overline{CE}_1 \geq V_{CC} - 0.3V$ or $CE_2 < V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$; no input may exceed $V_{CC} + 0.3V$	0.4	10	μA
		Ind'l			20	
$t_{CDR}^{[4]}$	Chip Deselect to Data Retention Time		0			ns
t_R	Operation Recovery Time		t_{RC}			ns

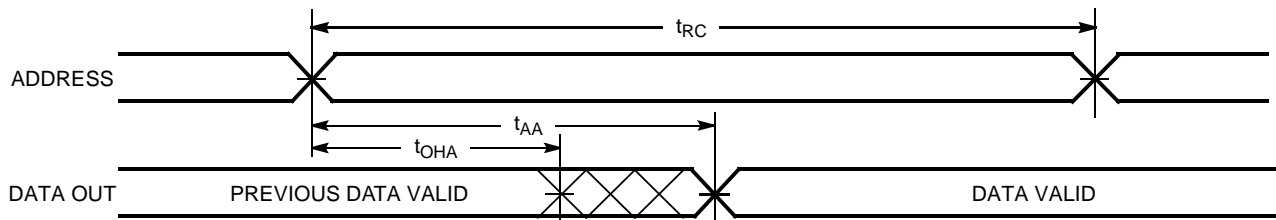
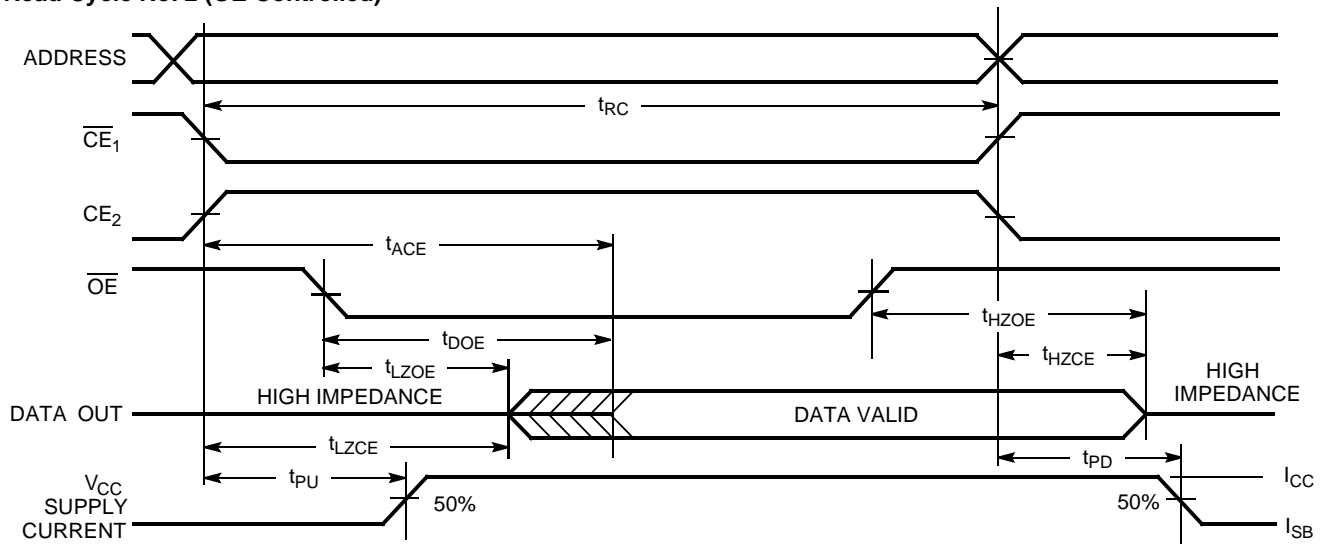
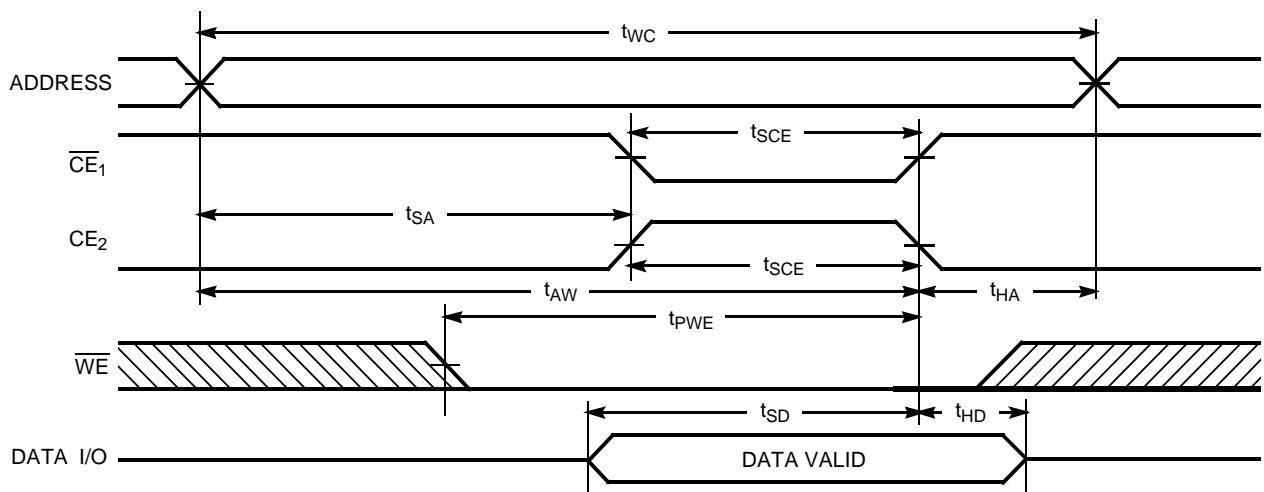
Notes:

- Tested initially and after any design or process changes that may affect these parameters.
- No input may exceed $V_{CC} + 0.3V$.

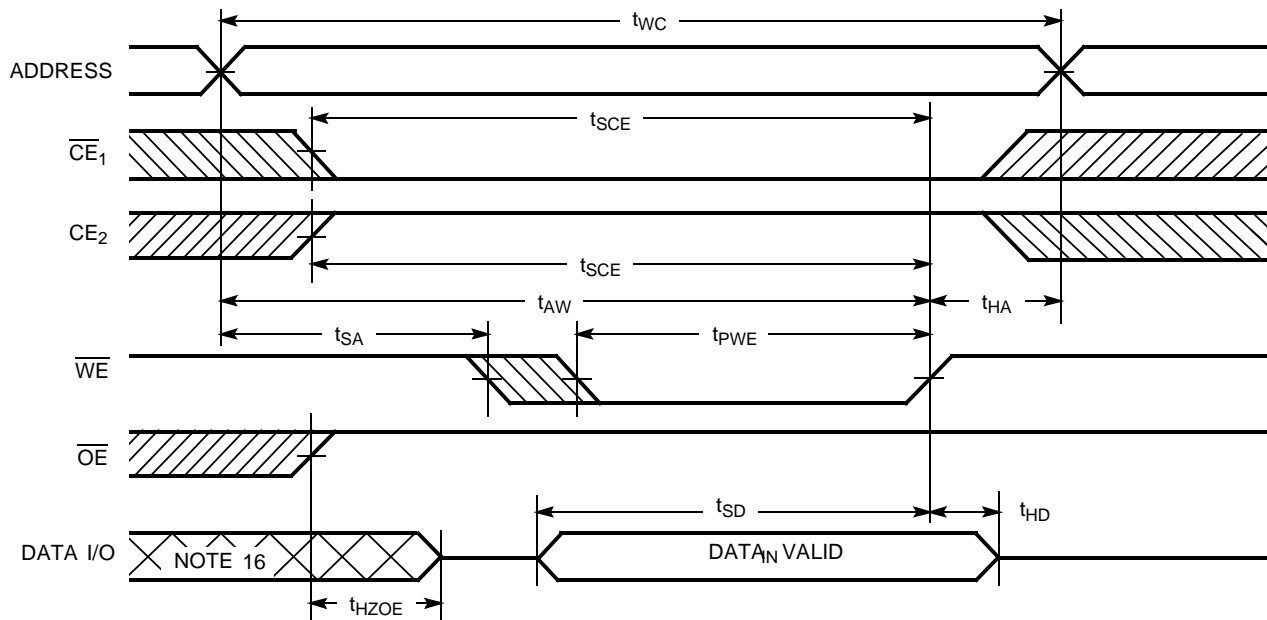
Data Retention Waveform

Switching Characteristics Over the Operating Range^[6]

Parameter	Description	CY62128V-55		CY62128V-70		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t _{RC}	Read Cycle Time	55		70		ns
t _{AA}	Address to Data Valid		55		70	ns
t _{OHA}	Data Hold from Address Change	5		10		ns
t _{ACE}	\overline{CE}_1 LOW and CE ₂ HIGH to Data Valid		55		70	ns
t _{DOE}	OE LOW to Data Valid		20		35	ns
t _{LZOE}	OE LOW to Low-Z ^[7]	10		10		ns
t _{HZOE}	OE HIGH to High-Z ^[7, 8]		20		25	ns
t _{LZCE}	\overline{CE}_1 LOW and CE ₂ HIGH to Low-Z ^[7]	10		10		ns
t _{HZCE}	CE ₁ HIGH or CE ₂ LOW to High-Z ^[7, 8]		20		25	ns
t _{PU}	\overline{CE}_1 LOW and CE ₂ HIGH to Power-up	0		0		ns
t _{PD}	CE ₁ HIGH or CE ₂ LOW to Power-down		55		70	ns
Write Cycle^[9, 10]						
t _{WC}	Write Cycle Time	55		70		ns
t _{SCE}	\overline{CE}_1 LOW and CE ₂ HIGH to Write End	45		60		ns
t _{AW}	Address Set-up to Write End	45		60		ns
t _{HA}	Address Hold from Write End	0		0		ns
t _{SA}	Address Set-up to Write Start	0		0		ns
t _{PWE}	WE Pulse Width	45		55		ns
t _{SD}	Data Set-up to Write End	25		30		ns
t _{HD}	Data Hold from Write End	0		0		ns
t _{HZWE}	WE LOW to High-Z ^[7, 8]		20		25	ns
t _{LZWE}	WE HIGH to Low-Z ^[7]	5		5		ns

6. Test conditions assume signal transition time of 5 ns or less timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±200 mV from steady-state voltage.
9. The internal write time of the memory is defined by the overlap of CE₁ LOW, CE₂ HIGH, and WE LOW. CE₁ and WE signals must be LOW and CE₂ HIGH to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
10. The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms
Read Cycle No. 1^[11, 12]

Read Cycle No. 2 (\overline{OE} Controlled)^[12, 13]

Write Cycle No. 1 ($\overline{CE_1}$ or CE_2 Controlled)^[13,14]

Notes:

11. Device is continuously selected. \overline{OE} , $\overline{CE_1} = V_{IL}$, $CE_2 = V_{IH}$.
12. \overline{WE} is HIGH for read cycle.
13. Address valid prior to or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)
Write Cycle No. 2 (WE Controlled, OE HIGH During Write)^[13, 14]

Truth Table

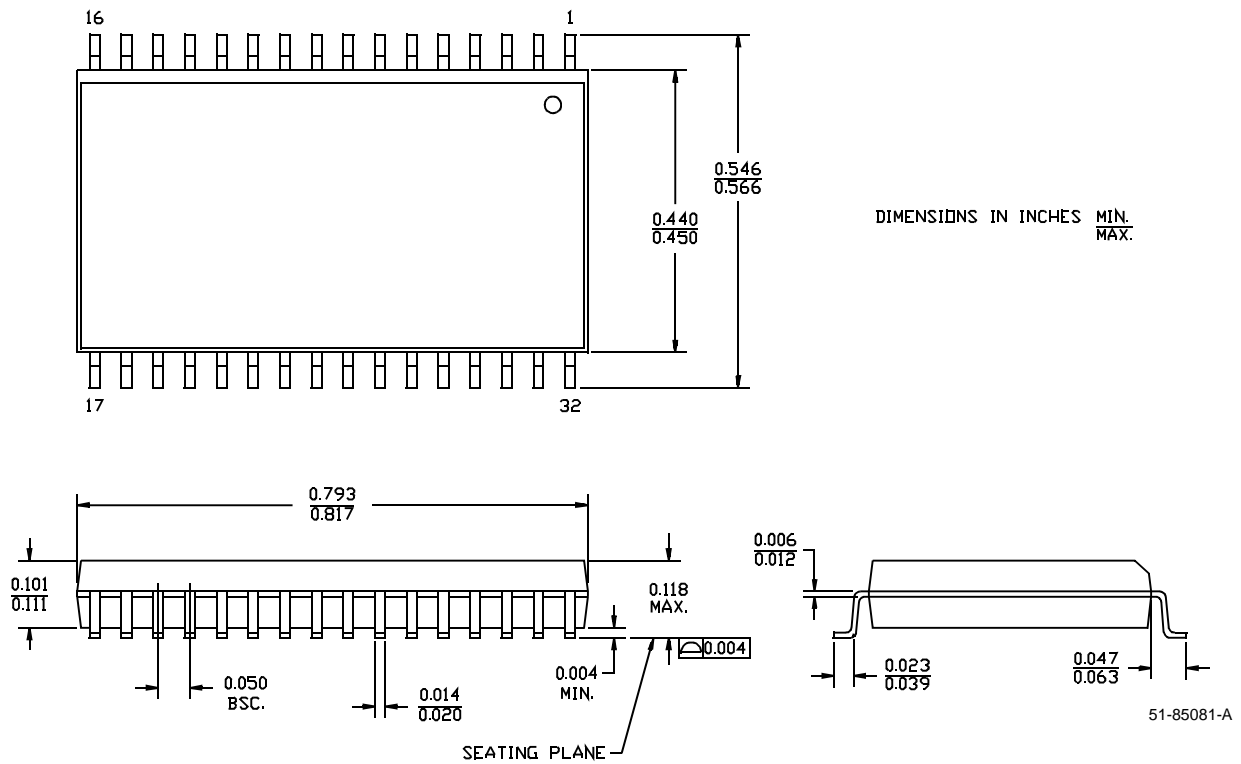
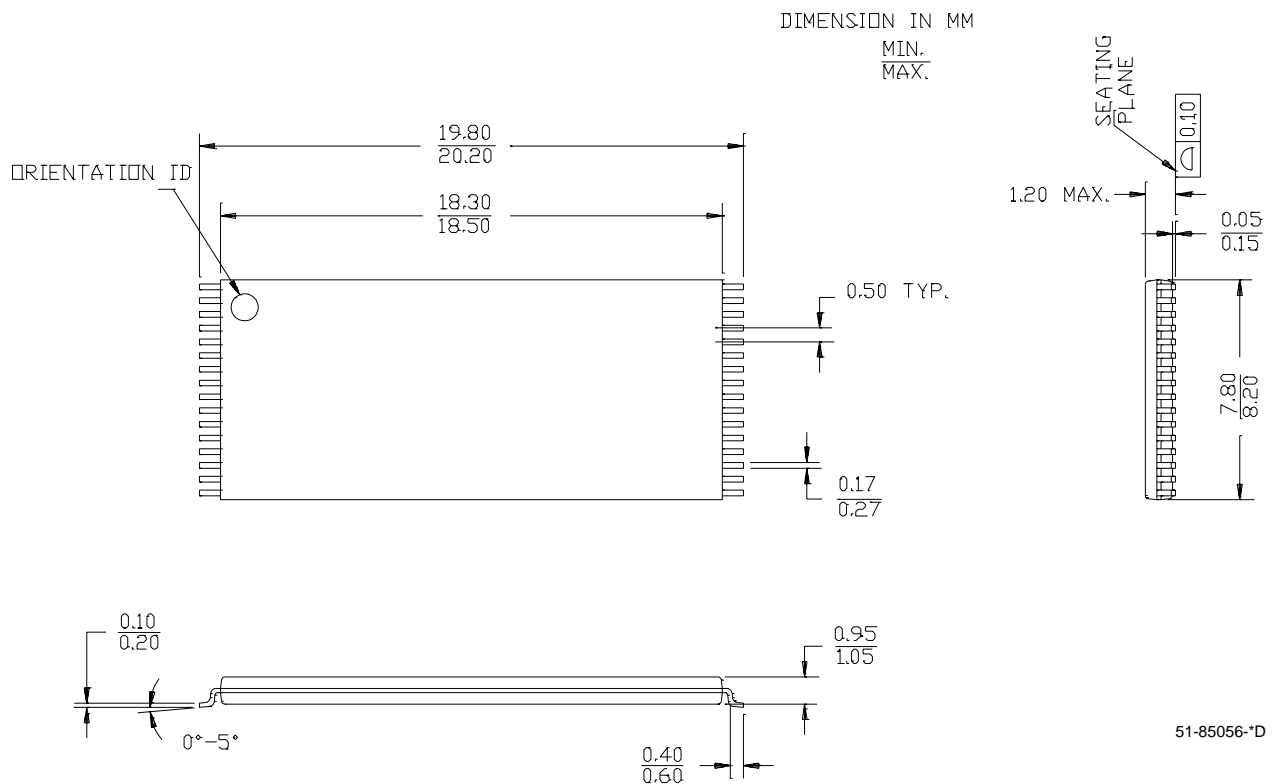
\overline{CE}_1	\overline{CE}_2	\overline{OE}	\overline{WE}	I/O ₀ -I/O ₇	Mode	Power
H	X	X	X	High-Z	Power-down	Standby (I_{SB})
X	L	X	X	High-Z	Power-down	Standby (I_{SB})
L	H	L	H	Data Out	Read	Active (I_{CC})
L	H	X	L	Data In	Write	Active (I_{CC})
L	H	H	H	High-Z	Selected, Outputs Disabled	Active (I_{CC})

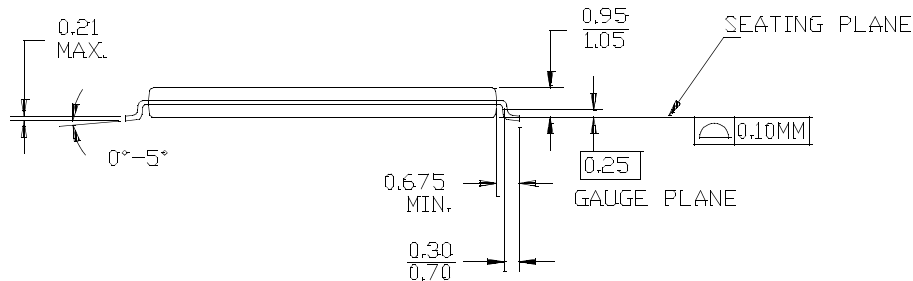
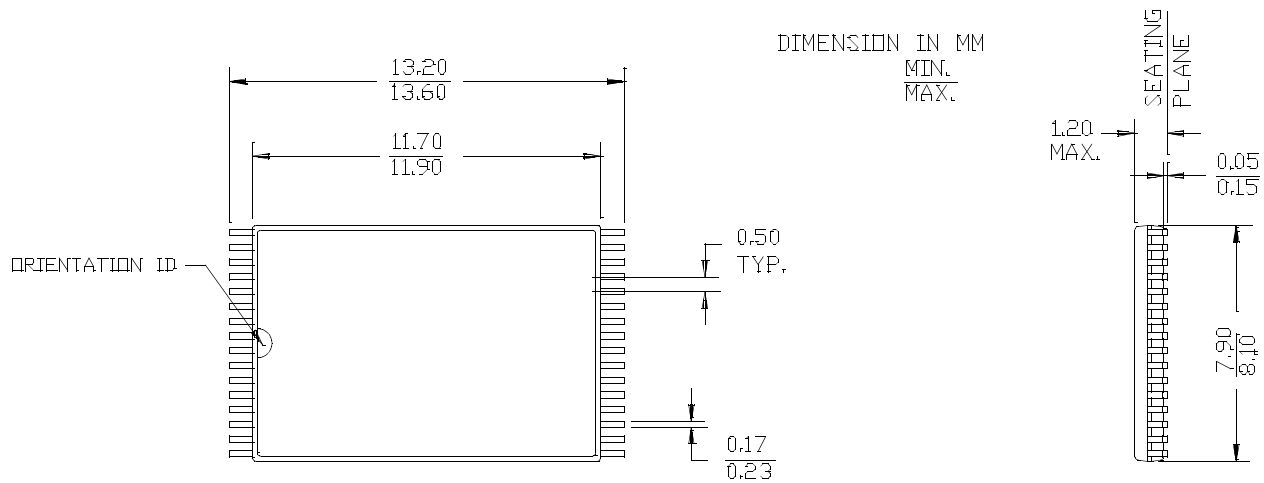
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62128VLL-55SC	S34	32-lead 450-Mil SOIC	Commercial
	CY62128VLL-55ZAI	ZA32	32-lead STSOP Type 1	Industrial
	CY62128VLL-55ZI	Z32	32-lead TSOP Type 1	
70	CY62128VLL-70SC	S34	32-lead 450-Mil SOIC	Commercial
	CY62128VLL-70ZC	Z32	32-lead TSOP Type 1	
	CY62128VLL-70ZAC	ZA32	32-lead STSOP Type 1	
	CY62128VLL-70ZRC	ZR32	32-lead Reverse TSOP Type 1	
	CY62128VLL-70SI	S34	32-lead 450-Mil SOIC	Industrial
	CY62128VLL-70ZI	Z32	32-lead TSOP Type 1	
	CY62128VLL-70ZAI	ZA32	32-lead STSOP Type 1	
	CY62128VLL-70ZRI	ZR32	32-lead Reverse TSOP Type 1	

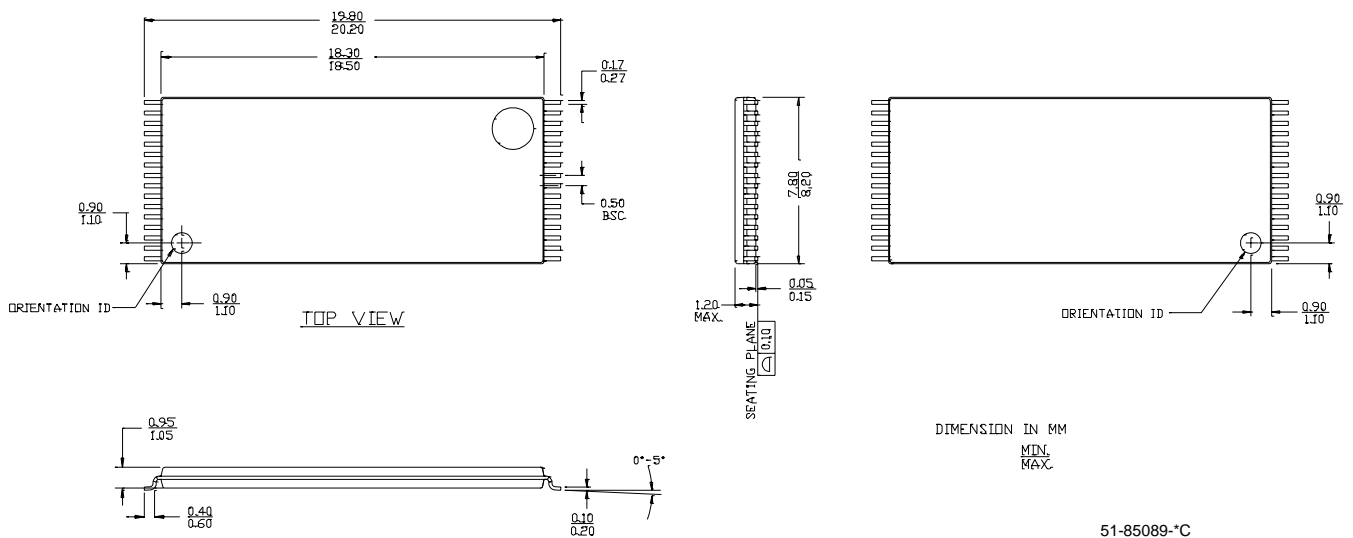
Notes:

14. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
15. If \overline{CE}_1 goes HIGH or \overline{CE}_2 goes LOW simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
16. During this period, the I/Os are in output state and input signals should not be applied.

Package Diagrams
32-Lead (450 MIL) Molded SOIC S34

32-lead Thin Small Outline Package Type I (8x20 mm) Z32


Package Diagrams (continued)
32-lead Shrunken Thin Small Outline Package (8x13.4 mm) ZA32


51-85094-*D

32-lead Reverse Thin Small Outline Package ZR32


51-85089-*C

All product and company names mentioned in this document are the trademarks of their respective holders.

Document Title: CY62128V (128K x 8) Static RAM				
Document Number: 38-05061				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	107252	09/10/01	SZV	Changed spec. number from 38-00547 to 38-05061
*A	111446	03/01/02	MGN	Removed obsolete parts. Changed to standardized format.
*B	116510	09/05/02	GBI	Added footnote 1. Clarified Control Pin (\overline{CE}_1 and CE_2) description