3-Dimensional Stack (3DS) DDR4 SDRAM

MT40A4G4, MT40A8G4, MT40A2G8, MT40A4G8

Description

The 16Gb, 2-high (2H) and 32Gb, 4-high (4H) 3-dimensional stack (3DS) DDR4 SDRAM use Micron's special 3DS 8Gb DDR4 SDRAM organized as two or four logical ranks. Refer to Micron's 8Gb DDR4 SDRAM data sheet for the specifications not included in this document. Specifications for base part number MT40A2G4 correspond to 2H 3DS manufacturing part number MT40A4G4 and to 4H 3DS manufacturing part number MT40A8G4; specifications for base part number MT40A1G8 correspond to 2H 3DS manufacturing part number MT40A2G8 and to 4H 3DS manufacturing part number MT40A4G8.

Features

- Uses Micron 3DS 8Gb die
- Single electrical signal load for each command, address and data pin
- Two or four logical ranks (includes one or two 2C pins)
- Each rank has 4 groups of 4 internal banks for concurrent operation
- $V_{DD} = V_{DDQ} = 1.2V$ (1.14–1.26V)
- 1.2V V_{DDQ}-terminated I/O
- JEDEC-standard ball-out
- Low-profile package
- T_C of 0°C to 95°C
  - 0°C to 85°C: 8192 refresh cycles in 64ms
  - 85°C to 95°C: 8192 refresh cycles in 32ms

Options	Marking
• 2H configurations	
– 128 Meg x 4 x 16 banks x 2 ranks	4G4
– 64 Meg x 8 x 16 banks x 2 ranks	2G8
• 4H configurations	
– 128 Meg x 4 x 16 banks x 4ranks	8G4
– 64 Meg x 8 x 16 banks x 4 ranks	4G8
• FBGA package (Pb-free)	
– 2H 78-ball FBGA (8.0mm x 12mm x 1.2mm) Die Rev :G	HPR
– 2H 78-ball FBGA (7.5mm x 11mm x 1.2mm) Die Rev :E	DVN
– 4H 78-ball FBGA (8.0mm x 12mm x 1.2mm) Die Rev :G	KVA
– 4H 78-ball FBGA (7.5mm x 11mm x 1.2mm) Die Rev :E	CLU
• Timing – cycle time[1]	
– 0.625ns @ CL = 26 (DDR4-3200)	-062H
– 0.682ns @ CL = 24 (DDR4-2933)	-068H
– 0.750ns @ CL = 22 (DDR4-2666)	-075H
– 0.833ns @ CL = 19 (DDR4-2400)	-083J
– 0.833ns @ CL = 20 (DDR4-2400)	-083H
– 0.937ns @ CL = 18 (DDR4-2133)	-093H
• Self refresh	
– Standard	None
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ 95°C)	None
• Revision	:G, :E

Notes: 1. CL = CAS (READ) latency.
2. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

Table 1: Key Timing Parameters

Speed Grade[1]	Data Rate (MT/s)	Target CL-*n*RCD-*n*RP	^{t}AA (ns)	^{t}RCD (ns)	^{t}RP (ns)
-062H	3200	26-22-22	16.25	13.75	13.75
-068H	2933	24-21-21	16.37	14.32 (14.06)	14.32 (14.06)
-075H	2666	22-19-19	16.50	14.25 (14.06)	14.25 (14.06)
-083J	2400	19-17-17	15.83	14.16 (14.06)	14.16 (13.75)
-083H	2400	20-17-17	16.67	14.16 (14.06)	14.16 (14.06)
-093H	2133	18-15-15	16.88	14.06	14.06

Note: 1. Refer to the Speed Bin Tables for additional details.

Table 2: 2H Addressing

Parameter	4096 Meg x 4	2048 Meg x 8
Configuration	128 Meg x 4 x 16 banks x 2 ranks	64 Meg x 8 x 16 banks x 2 ranks
Logical rank address	C[0]	C[0]
Bank group address	BG[1:0]	BG[1:0]
Bank count per group	4	4
Bank address in bank group	BA[1:0]	BA[1:0]
Row address	128K A[16:0]	64K A[15:0]
Column address	1K A[9:0]	1K A[9:0]

Table 3: 4H Addressing

Parameter	8192 Meg x 4	4096 Meg x 8
Configuration	128 Meg x 4 x 16 banks x 4 ranks	64 Meg x 8 x 16 banks x 4 ranks
Logical rank address	C[1:0]	C[1:0]
Bank group address	BG[1:0]	BG[1:0]
Bank count per group	4	4
Bank address in bank group	BA[1:0]	BA[1:0]
Row address	128K A[16:0]	64K A[15:0]
Column address	1K A[9:0]	1K A[9:0]

Contents

List of Figures

List of Tables

Important Notes and Warnings

Micron Technology, Inc. ("Micron") reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions. This document supersedes and replaces all information supplied prior to the publication hereof. You may not rely on any information set forth in this document if you obtain the product described herein from any unauthorized distributor or other source not authorized by Micron.

Automotive Applications. Products are not designed or intended for use in automotive applications unless specifically designated by Micron as automotive-grade by their respective data sheets. Distributor and customer/distributor shall assume the sole risk and liability for and shall indemnify and hold Micron harmless against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, death, or property damage resulting directly or indirectly from any use of non-automotive-grade products in automotive applications. Customer/distributor shall ensure that the terms and conditions of sale between customer/distributor and any customer of distributor/customer (1) state that Micron products are not designed or intended for use in automotive applications unless specifically designated by Micron as automotive-grade by their respective data sheets and (2) require such customer of distributor/customer to indemnify and hold Micron harmless against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, death, or property damage resulting from any use of non-automotive-grade products in automotive applications.

Critical Applications. Products are not authorized for use in applications in which failure of the Micron component could result, directly or indirectly in death, personal injury, or severe property or environmental damage ("Critical Applications"). Customer must protect against death, personal injury, and severe property and environmental damage by incorporating safety design measures into customer's applications to ensure that failure of the Micron component will not result in such harms. Should customer or distributor purchase, use, or sell any Micron component for any critical application, customer and distributor shall indemnify and hold harmless Micron and its subsidiaries, subcontractors, and affiliates and the directors, officers, and employees of each against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, or death arising in any way out of such critical application, whether or not Micron or its subsidiaries, subcontractors, or affiliates were negligent in the design, manufacture, or warning of the Micron product.

Customer Responsibility. Customers are responsible for the design, manufacture, and operation of their systems, applications, and products using Micron products. ALL SEMICONDUCTOR PRODUCTS HAVE INHERENT FAILURE RATES AND LIMITED USEFUL LIVES. IT IS THE CUSTOMER'S SOLE RESPONSIBILITY TO DETERMINE WHETHER THE MICRON PRODUCT IS SUITABLE AND FIT FOR THE CUSTOMER'S SYSTEM, APPLICATION, OR PRODUCT. Customers must ensure that adequate design, manufacturing, and operating safeguards are included in customer's applications and products to eliminate the risk that personal injury, death, or severe property or environmental damages will result from failure of any semiconductor component.

Limited Warranty. In no event shall Micron be liable for any indirect, incidental, punitive, special or consequential damages (including without limitation lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort, warranty, breach of contract or other legal theory, unless explicitly stated in a written agreement executed by Micron's duly authorized representative.

3DS (Master/Slave) Overview

The 3DS DDR4 SDRAM provides enhanced functionality and performance when compared to a traditional stacked DDR4 SDRAM device. This data sheet details the product's unique features; providing package dimensions, functional block diagrams, and electrical and timing specifications as applicable. Topics not addressed in this data sheet are covered in the standard Micron DDR4 SDRAM data sheet.

The 3DS device provides a stack of DRAM die with one die configured as the master and the remaining die in the stack configured as slave device(s). Each die functions as a different logical rank. Because the master die provides isolation (or buffering) to the slave die, the electrical signal loading of the external interface is that of a single DDR4 SDRAM, which can improve timing, bus speeds, and signal integrity while lowering power consumption—a significant benefit over a traditional stacked device.

Functionality

The 3DS DDR4 SDRAM is a high-speed, CMOS dynamic random access memory built as a 2-high or 4-high 3DS component. The 2-high device consists of one master die and one slave die. The 4-high device consists of one master die and three slave die. The bottom die will always be the master and any stacked die will be a slave.

Figure 1: 2-High 3DS Functional Block Diagram

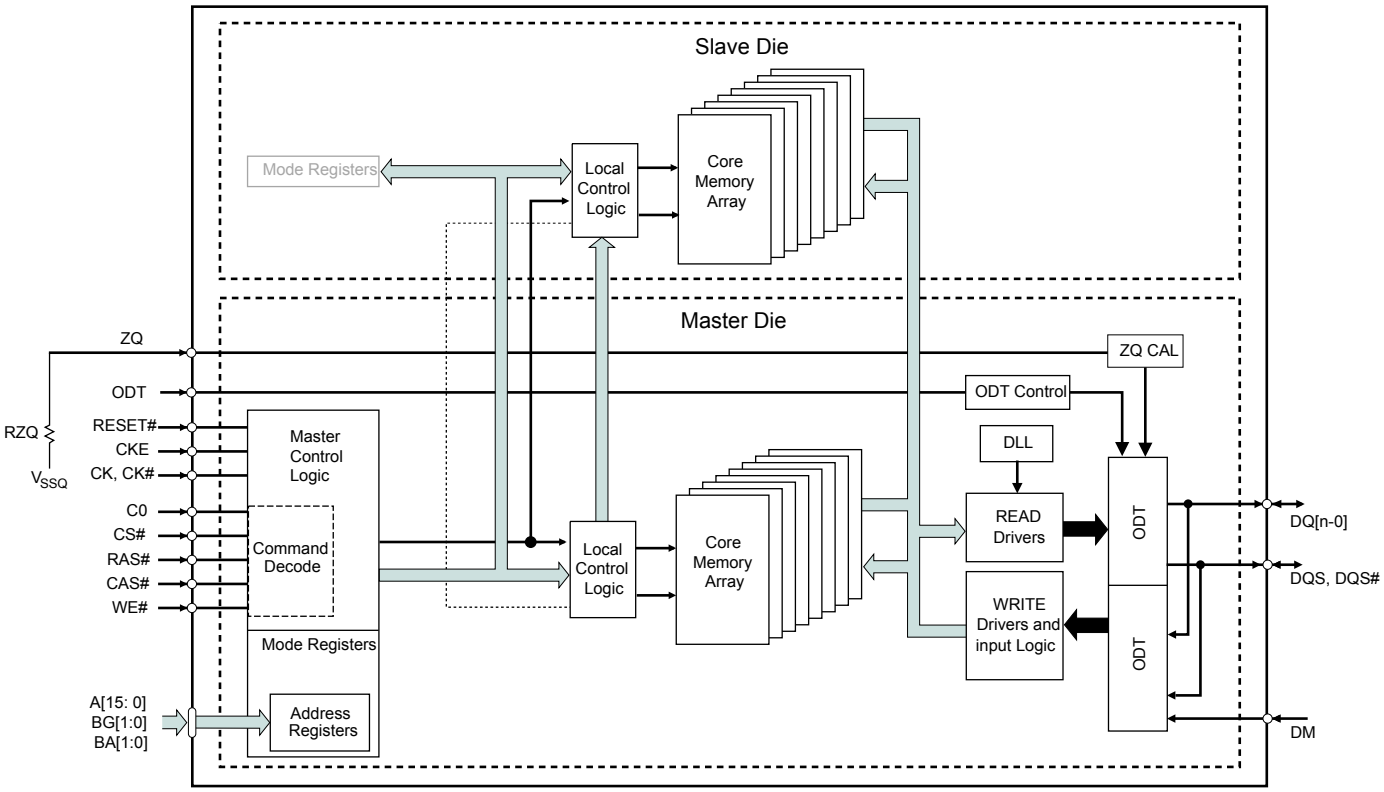
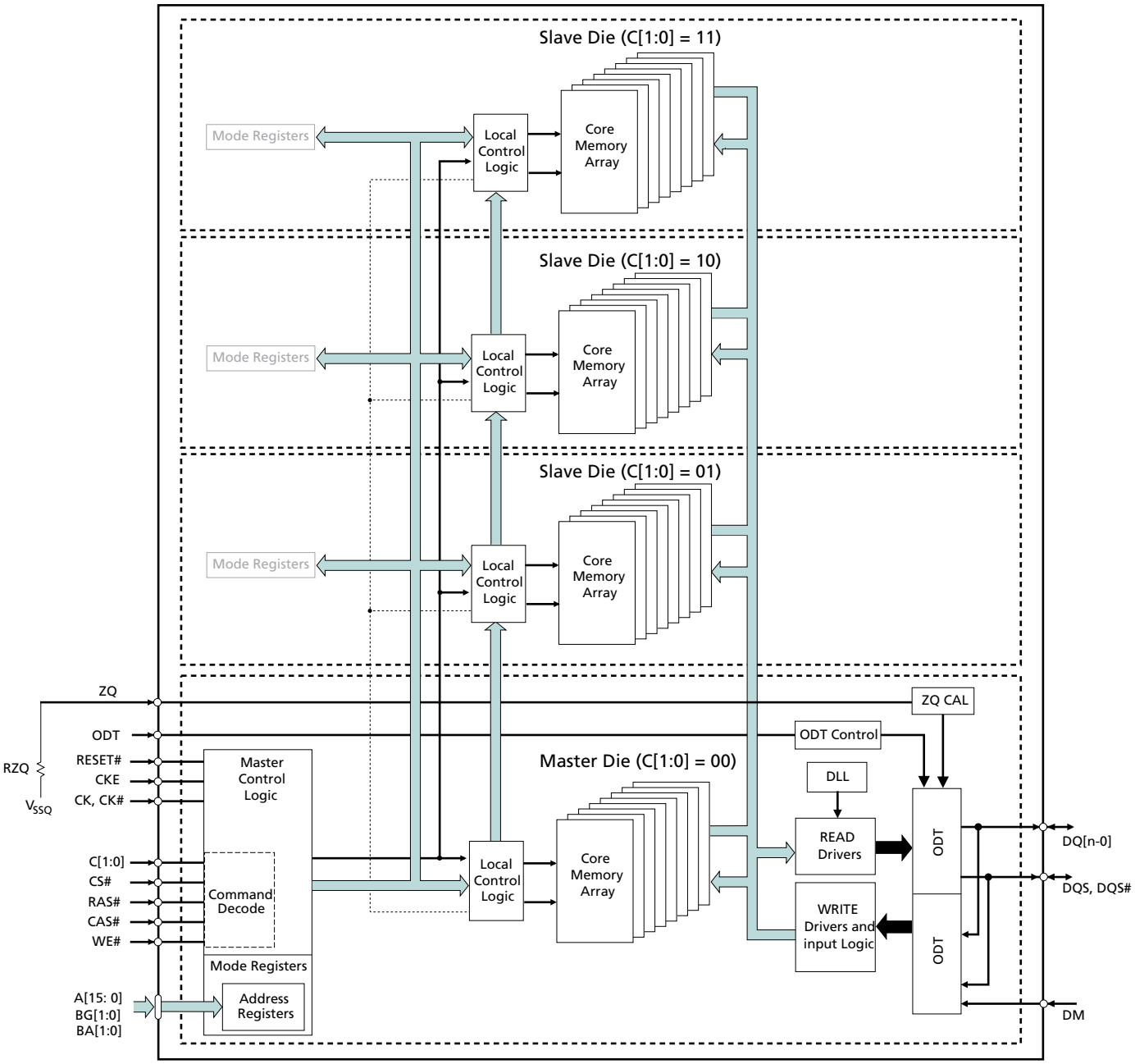


Figure 2: 4-High 3DS Functional Block Diagram



Addressing

Each die within the 3DS stack uses the same addressing as its like-density monolithic device. A 2-high stack has two independent selectable logical ranks; a 4-high stack has four independent selectable logical ranks. In contrast to conventionally stacked DDR4 (TwinDie), 3DS stacks only have one CS_n pin regardless of the number of die; die (logical rank) selection is accomplished by the state of the Chip ID (Cx) pin(s), which behave as rank address(es). Because logic is shared between master and slave(s) on the 3DS device, some commands and operations affect all ranks while others only impact a single rank.

Table 4: 3DS Signals

Configuration	Number of Die (Logical Ranks)	Relevant Signals
16Gb (2-high) 3DS addressing – 8Gb die	2	CS_n, C0
32Gb (4-high) 3DS addressing – 8Gb die	4	CS_n, C0, C1

Table 5: 2H Stack Addressing

Logical Rank Selected	CS_n	C0
0	L	L
1	L	H

Table 6: 4H Stack Addressing

Logical Rank Selected	CS_n	C1	C0
0	L	L	L
1	L	L	H
2	L	H	L
3	L	H	H

All-Die Commands vs. Single-Die Commands

Some commands issued to the 3DS stack device only impact the function of a single rank (providing the host controller with the best functionality), while others affect all of the ranks (because of the shared nature of the logic).

Table 7: Commands/Operations vs. Ranks Impacted

Command/Operation	Ranks Impacted	Notes
Mode register	All	One mode register sets condition for all die/ranks
Gear-down mode sync	All	Single electrical interface
Write leveling	All	Single electrical interface
ZQ CAL	All	Single electrical interface
ODT	All	Single electrical interface
Power-down (including SELF REFRESH)	All	Single CKE

Table 7: Commands/Operations vs. Ranks Impacted (Continued)

Command/Operation	Ranks Impacted	Notes
ACTIVE	By rank	New tRRD/tFAW timings
WRITE	By rank	New tCCD timings
READ	By rank	New tCCD timings
PRECHARGE	By rank	Precharge all restrictions
REFRESH	By rank	New tRFC timing to stagger refresh

Initialization and Reset

The 3DS device requires a complete power-up and initialization sequence, which follows the standard DDR4 SDRAM requirement. Mode register commands affect the operation of all die, so there is no need to send mode register commands to each die individually. The 3DS device has special mode register set (MRS) requirements described in the following section; all other power-up and reset timings and conditions follow the normal operations listed in the DDR4 SDRAM specification.

Mode Register Set

Standard mode register locations and definitions apply to the 3DS device as described in the DDR4 SDRAM specification, except as outlined in this section. Any valid MRS command sets the operating mode for all logical ranks. As such, prior to an MRS command, all logical ranks must be precharged and tRP must be met. In addition, tMRD and tMOD apply to MRS commands for the 3DS component.

Table 8: Truth Table for MRS Commands

DRAM Command[1]	CS#	C2	C1	C0	Status
MODE REGISTER SET	L	V	V	V	MRS affects all logical ranks
MODE REGISTER SET	H	V	V	V	All Ranks see DESELECT
Any other command	H	V	V	V	All Ranks see DESELECT

Note: 1. H = High logic level, L = Low logic level, V = H or L (but a defined logic level).

Unique 3DS MRS Values for Mode Register 1

The additional latency settings of the 3DS device requires support for additive latency of 3 (AL = CL - 3). This setting is required if tAA > tRCD. See Speed Bin tables for more information.

Table 9: MR1 Register Definition

Mode Register	Description
4, 3	**Additive latency (AL) – Command additive latency setting** 00 = 0 (AL disabled) 01 = CL - 1[1] 10 = CL - 2 11 = CL - 3

Note: 1. The additive latency settings for the 3DS device are some different than for monolithic device. The setting AL = CL - 3 may be useful where *n*CL > *n*RCD + 2.

Multipurpose Register

When CA parity or Write CRC are enabled and an error is detected, the 3DS DDR4 device reports the latched states of C[2:0] for the error cycle in multipurpose register(MPR) Page 1 MPR3[2:0]. This is shown in the MPR Page and MPRx Definitions table in the standard DDR4 data sheet. In the case of 2H and 4H stacks, where not all C[2:0] pins are used, the unused bits report zero.

Post Package Repair

Post package repair (PPR) is supported on 3DS components and functions largely the same as on monolithic components. For 3DS devices, the host also provides the die (logical rank) address on the C[2:0] pins for the ACT command associated with the repair row address, and REFRESH is the only operation allowed by the host on any die while in PPR mode.

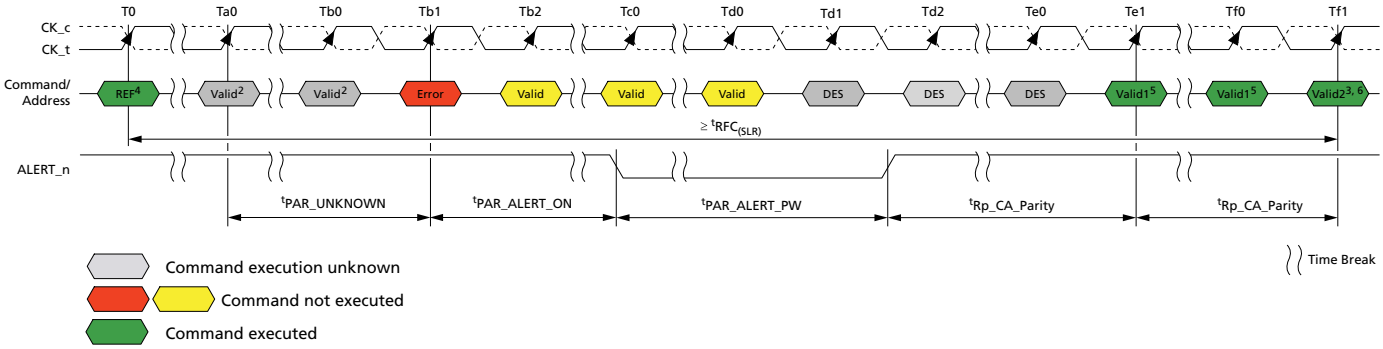
Command/Address Parity

Because command/address (CA) parity provides protection against errors on the command/address bus and the 3DS device has only one electrical interface, parity errors may impact operations on all die (logical ranks). Otherwise, with the exception of REFRESH operations discussed below, CA parity on the 3DS device functions largely the same as on the monolithic component.

After a REF command has been issued, a monolithic DDR4 component allows only DESELECT commands until ^{t}RFC is satisfied, alleviating the device from having to validate commands for correct parity during this time. A 3DS device allows commands to be latched to one rank while another has a refresh in progress; as a result, the 3DS device has the following behaviors with respect to CA parity:

- A 3DS device continues to calculate CA parity even while refreshes are ongoing
- The CA parity error recovery process shouldn't interrupt refresh(es) that may be in progress
- The CA parity error recovery process returns to a precharge-all state except for any rank(s) already refreshing
- MRS commands must wait until ^{t}RFC$_{(SLR)}$ is complete for all refreshes in progress (this is also true for accessing MPR mode)

Figure 3: CA Parity Error During Refresh



Notes:
1. DRAM is emptying queues. Precharge all and parity checking are off until parity error status bit is cleared.
2. Command execution is unknown; the corresponding DRAM internal state change may or may not occur. The DRAM controller should consider both cases and make sure that the command sequence meets the specifications.
3. Normal operation with parity latency (CA parity persistent error mode disabled). Parity checking is off until parity error status bit is cleared.
4. When a REF command is issued in ^{t}PART_UNKNOWN range, REF may not be executed; the host should wait $^{t}RFC_{(SLR)}$ to issue valid commands to the same logical rank.
5. Valid commands to the rank with no on-going REF commands are available.
6. Valid commands to the rank with on-going REF commands, including MRS, are available.

Calibration

All configurations of the 3DS device use only a single ZQ pin, which has the same functionality as that of a standard DDR4 SDRAM device. The 3DS device should be considered a single device from the standpoint of calibration. ZQCL commands are required during the normal initialization and/or reset sequences. ZQCS commands are also required for the 3DS device. When a ZQ command is issued, all ranks must be idle (all banks precharged with only NOP/DES commands) until the calibration sequence is complete. All DDR4 SDRAM core ZQ timing parameters and conditions apply simultaneously to all die within the 3DS stack; after a ZQ command has been issued, the appropriate timing must be met before issuing another ZQ command, regardless of the status of the C[2:0] pins.

ACTIVE Operation

Restrictions for ACT commands to banks of the same logical rank (SLR) follow the standard DDR4 SDRAM specification, that is, ^{t}RRD and ^{t}FAW apply to 3DS devices as $^{t}RRD_{(SLR)}$ and $^{t}FAW_{(SLR)}$. ACT commands to different logical ranks (DLR) must be separated by $^{t}RRD_{(DLR)}$ as shown in the figure and table below. The rate at which groups of four ACT commands can be issued to different die is given by $^{t}FAW_{(DLR)}$, which is always 16 clocks for every speed, configuration and density.

Figure 4: ^{t}RRD and ^{t}FAW Timing Example

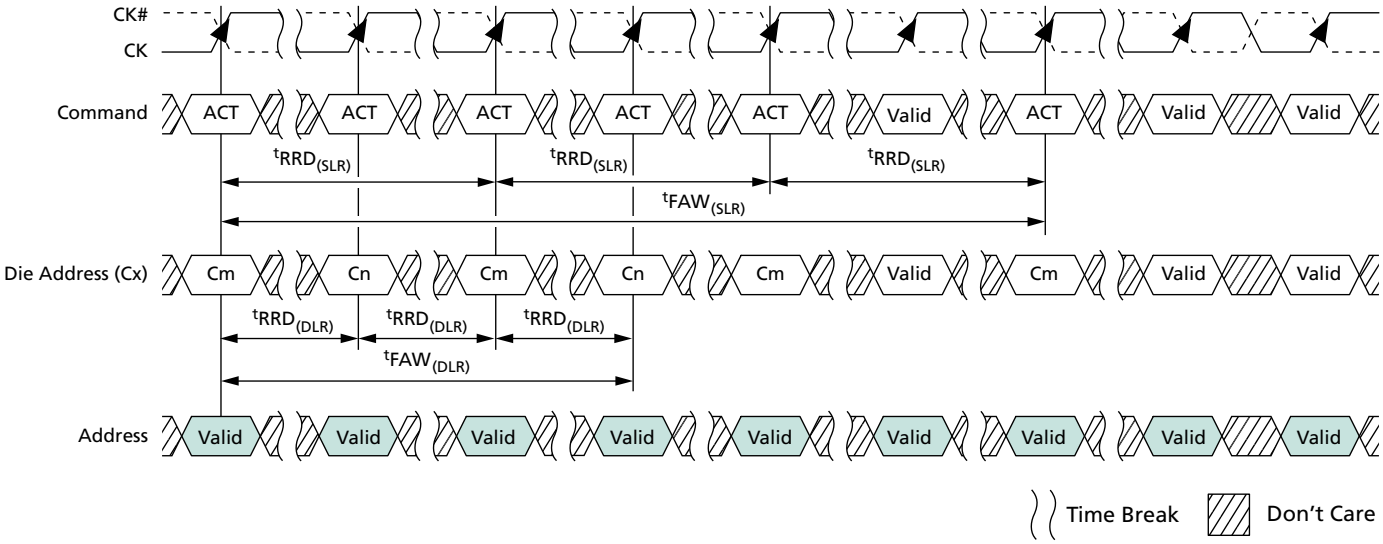


Table 10: 3DS Device ^{t}RRD and ^{t}FAW Timing at 1600/1866/2133/2400

Symbol	Description		DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Units
$^{t}RRD_{(SLR)}$	Active-to-Active (same logical rank)	Short	MAX (4*n*CK, 5ns)	MAX (4*n*CK, 4.2ns)	MAX (4*n*CK, 3.7ns)	MAX (4*n*CK, 3.3ns)	CK/ns
		Long	MAX (4*n*CK, 6ns)	MAX (4*n*CK, 5.3ns)	MAX (4*n*CK, 5.3ns)	MAX (4*n*CK, 4.9ns)	CK/ns
$^{t}RRD_{(DLR)}$	Refresh or Active-to-Active (different logical ranks)		4	4	4	4	CK
$^{t}FAW_{(SLR)}$	Four active windows (same logical rank)	x4	MAX (16*n*CK, 20ns)	MAX (16*n*CK, 17ns)	MAX (16*n*CK, 15ns)	MAX (16*n*CK, 13ns)	CK/ns
		x8	MAX (20*n*CK, 25ns)	MAX (20*n*CK, 23ns)	MAX (20*n*CK, 21ns)	MAX (20*n*CK, 21ns)	CK/ns
$^{t}FAW_{(DLR)}$	Four active windows (different logical ranks)		16	16	16	16	CK
^{t}XS	Exit Self-Refresh to commands not requiring a locked DLL		MAX (5*n*CK, $^{t}RFC_{(SLR)}$min +10ns)	MAX (5*n*CK, $^{t}RFC_{(SLR)}$min +10ns)	MAX (5*n*CK, $^{t}RFC_{(SLR)}$min +10ns)	MAX (5*n*CK, $^{t}RFC_{(SLR)}$min +10ns)	CK/ns

Table 11: 3DS Device ^{t}RRD and ^{t}FAW Timing at 2666/2933/3200

Symbol	Description		DDR4-2666	DDR4-2933	DDR4-3200	Units
$^{t}RRD_{(SLR)}$	Active-to-Active (same logical rank)	Short	MAX (4*n*CK, 3.0ns)	MAX (4*n*CK, 2.7ns)	MAX (4*n*CK, 2.5ns)	CK/ns
		Long	MAX (4*n*CK, 4.9ns)	MAX (4*n*CK, 4.9ns)	MAX (4*n*CK, 4.9ns)	CK/ns
$^{t}RRD_{(DLR)}$	Refresh or Active-to-Active (different logical ranks)		4	4	4	CK
$^{t}FAW_{(SLR)}$	Four active windows (same logical rank)	x4	MAX (16*n*CK, 12ns)	MAX (16*n*CK, 10.875ns)	MAX (16*n*CK, 10ns)	CK/ns
		x8	MAX (20*n*CK, 21ns)	MAX (20*n*CK, 21ns)	MAX (20*n*CK, 21ns)	CK/ns
$^{t}FAW_{(DLR)}$	Four active windows (different logical ranks)		16	16	16	CK
^{t}XS	Exit Self-Refresh to commands not requiring a locked DLL		MAX (5*n*CK, $^{t}RFC_{(SLR)}$min +10ns)	MAX (5*n*CK, $^{t}RFC_{(SLR)}$min +10ns)	MAX (5*n*CK, $^{t}RFC_{(SLR)}$min +10ns)	CK/ns

Column Access Operation (WRITE and READ) Timings

Column accesses, WRITE and READ bursts, on DDR4 3DS components are similar to those for monolithic components. The starting column, bank and die (logical rank) addresses are provided with the WRITE or READ command, and auto precharge is either enabled or disabled for that burst access.

Unlike conventional dual-die package (DDP) and quad-die package (QDP) devices, the 3DS device will allow concatenated column access data from either the same die (C*n*) or from different die (C*m*), as long as the appropriate ^{t}CCDx specification is met. Whenever ^{t}CCD = 4, the first data element from the new burst follows the last element of a completed burst. The new column access command should be issued ^{t}CCD cycles after the first column access command. If BC4 is enabled, ^{t}CCD must still be met (which will cause a gap in the data output).

The table below describes the column access timings for 2-high and 4-high 3DS devices.

Table 12: Minimum Column-to-Column Timing for 2-High and 4-High Stacks at 1600/1866/2133/2400/2666

Die (Logical Rank)	Bank Group	Symbol	Timing Parameter	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	Units
Same	Same	^{t}CCD_L$_{(SLR)}$	READ-to-READ	MAX (4*n*CK, 6.25ns)	MAX (4*n*CK, 5.355ns)	MAX (4*n*CK, 5.355ns)	MAX (4*n*CK, 5ns)	MAX (4*n*CK, 5ns)	*n*CK
			WRITE-to-WRITE						
		^{t}RTW_L$_{(SLR)}$	READ-to-WRITE	CL - CWL + RBL/2 + 1 × ^{t}CK + ^{t}WPRE					
		^{t}WTR_L$_{(SLR)}$	WRITE-to-READ	CWL + WBL/2 + ^{t}WTR_L					
	Different	^{t}CCD_S$_{(SLR)}$	READ-to-READ	4	4	4	4	4	
			WRITE-to-WRITE						
		^{t}RTW_S$_{(SLR)}$	READ-to-WRITE	CL - CWL + RBL/2 + 1 × ^{t}CK + ^{t}WPRE					
		^{t}WTR_S$_{(SLR)}$	WRITE-to-READ	CWL + WBL/2 + ^{t}WTR_S					
Different	Same or Different	^{t}CCD$_{(DLR)}$	READ-to-READ	MAX (4*n*CK, 5ns)	MAX (4*n*CK, 4.284ns)	MAX (4*n*CK, 3.748ns)			
			WRITE-to-WRITE						
		^{t}RTW$_{(DLR)}$	READ-to-WRITE	CL - CWL + RBL/2 + 1 × ^{t}CK + ^{t}WPRE					
		^{t}WTR$_{(DLR)}$	WRITE-to-READ	CWL + WBL/2 + ^{t}WTR_S					

Table 13: Minimum Column-to-Column Timing for 2-High and 4-High Stacks at 2933/3200

Die (Logical Rank)	Bank Group	Symbol	Timing Parameter	DDR4-2933	DDR4-3200	Units
Same	Same	$^{t}CCD\_L_{(SLR)}$	READ-to-READ	MAX (4*n*CK, 5ns)	MAX (4*n*CK, 5ns)	*n*CK
			WRITE-to-WRITE			
		$^{t}RTW\_L_{(SLR)}$	READ-to-WRITE	CL - CWL + RBL/2 + 1 × ^{t}CK + $^{t}WPRE$		
		$^{t}WTR\_L_{(SLR)}$	WRITE-to-READ	CWL + WBL/2 + $^{t}WTR\_L$		
	Different	$^{t}CCD\_S_{(SLR)}$	READ-to-READ	4	4	
			WRITE-to-WRITE			
		$^{t}RTW\_S_{(SLR)}$	READ-to-WRITE	CL - CWL + RBL/2 + 1 × ^{t}CK + $^{t}WPRE$		
		$^{t}WTR\_S_{(SLR)}$	WRITE-to-READ	CWL + WBL/2 + $^{t}WTR\_S$		
Different	Same or Different	$^{t}CCD_{(DLR)}$	READ-to-READ	MAX (4*n*CK, 3.41ns)	MAX (4*n*CK, 3.125ns)	
			WRITE-to-WRITE			
		$^{t}RTW_{(DLR)}$	READ-to-WRITE	CL - CWL + RBL/2 + 1 × ^{t}CK + $^{t}WPRE$		
		$^{t}WTR_{(DLR)}$	WRITE-to-READ	CWL + WBL/2 + $^{t}WTR\_S$		

READ Operation

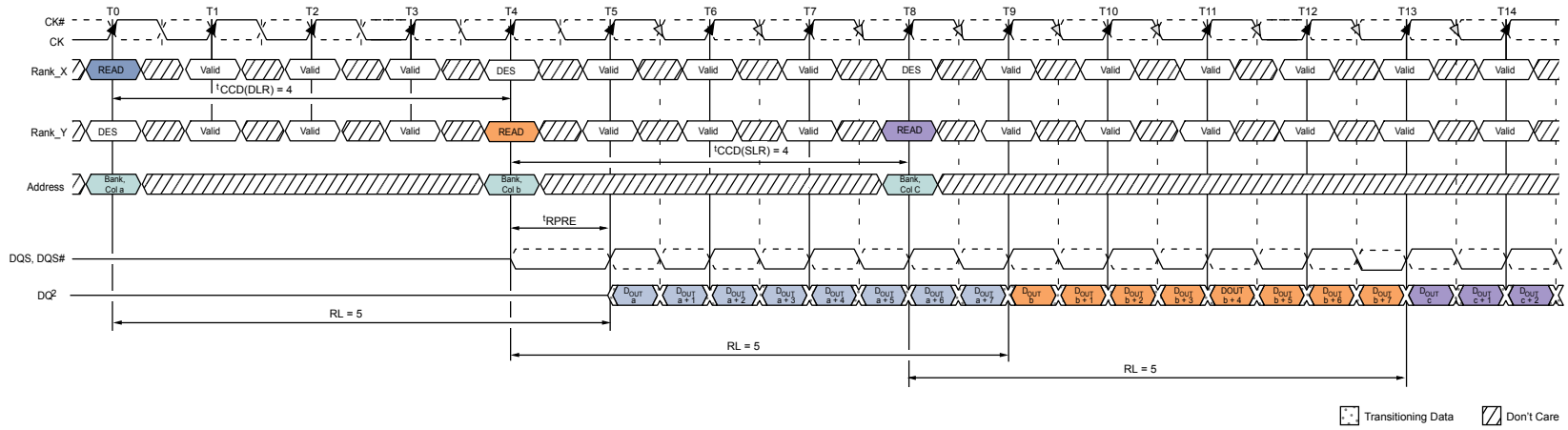
READ bursts are initiated with a READ command. The starting column, bank and die (logical rank) addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access.

READ Operation Examples

READ operations on the 3DS device follow the standard DDR4 SDRAM requirements, but include the following specific conditions for back-to-back READ commands:

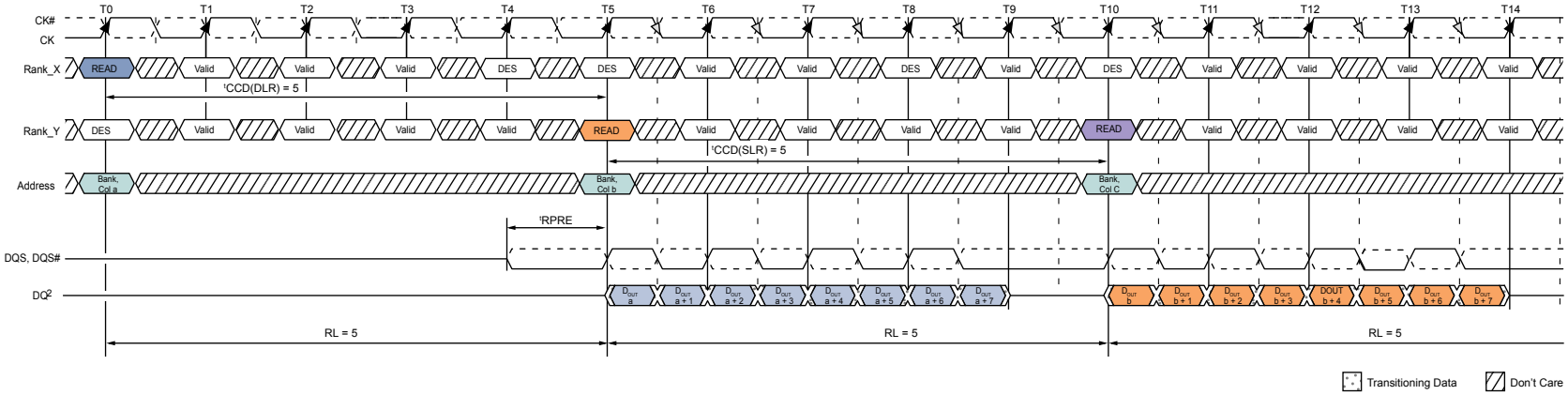
- ^{t}CCD = 4 to the same logical rank (SLR) or different logical ranks (DLR) single ^{t}RPRE, gapless data with continuous DQS_t, DQS_c toggle, see Figure 5 (page 19).
- ^{t}CCD = 5 t to the same logical rank (SLR) or different logical ranks (DLR); DQS_t, DQS_c is maintained between ^{t}RPST and ^{t}RPRE, see Figure 6 (page 19).
- ^{t}CCD ≥ 6 to the same logical rank (SLR) or different logical ranks (DLR); DQS_t, DQS_c is High-Z between ^{t}RPST and ^{t}RPRE, see Figure 7 (page 20).

Figure 5: READ BL8 to READ BL8 (^{t}CCD = 4) Example



Notes:
1. BL8, RL = 5 (CL = 5, AL = 0).
2. D_{OUT} a, b, or c = data-out from column a, b, or c.

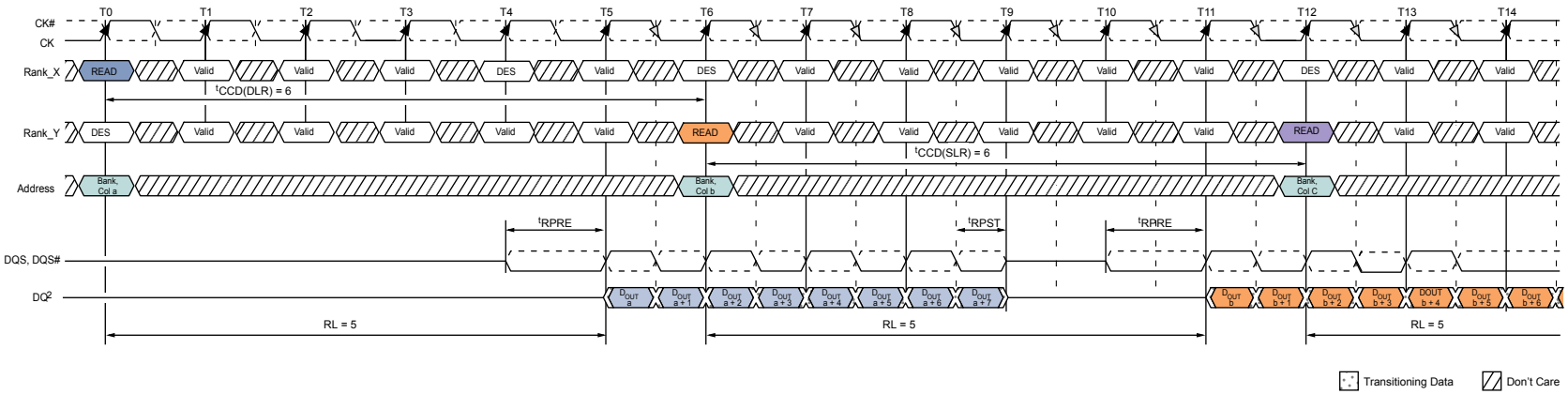
Figure 6: READ BL8 to READ BL8 (^{t}CCD = 5) Example



Notes:
1. BL8, RL = 5 (CL = 5, AL = 0).
2. D_{OUT} a, b, or c = data-out from column a, b, or c.

CCMTD-1725822587-10122
16gb_32gb_3ds.pdf - Rev. C 02/19 EN

Figure 7: READ BL8 to READ BL8 (^{t}CCD = 6) Example



Notes:
1. BL8, RL = 5 (CL = 5, AL = 0).
2. D_{OUT} a, b, or c = data-out from column a, b, or c.

WRITE Operations

WRITE bursts are initiated with a WRITE command. The starting column, bank and die (logical rank) addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst. If auto precharge is not selected, the row will remain open for subsequent accesses. After a WRITE command has been issued, the WRITE burst may not be interrupted.

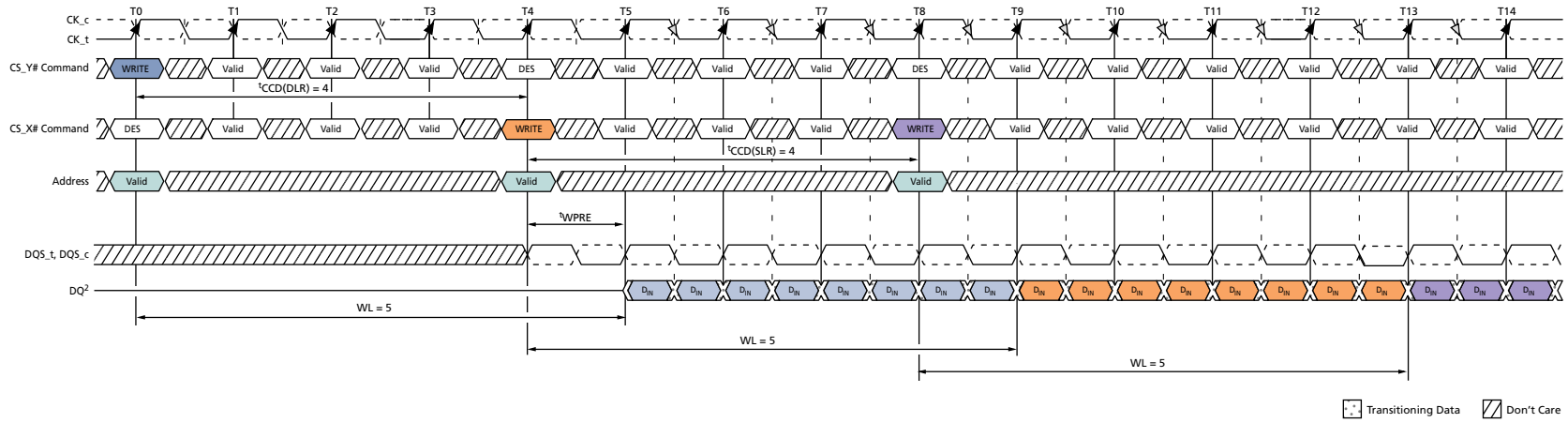
Data for any WRITE burst (if BL = 8) may be concatenated with a subsequent WRITE command to provide a continuous flow of input data. This applies to a sequence of WRITE commands to either $C_{(SLR)}$ or $C_{(DLR)}$. The new WRITE command can be issued ^{t}CCD clocks following the previous WRITE command.

WRITE Operation Examples

WRITE operations for the 3DS device follow the standard DDR4 SDRAM requirements, but include the following specific conditions for back-to-back WRITE commands:

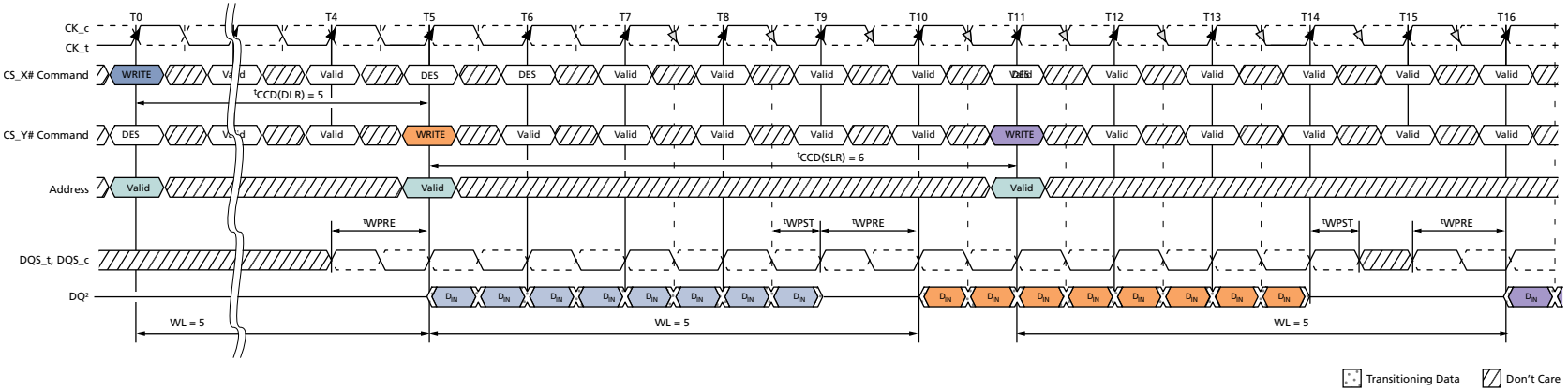
- ^{t}CCD = 4 to the same logical rank (SLR) or different logical ranks (DLR). An example of a single ^{t}WPRE, gapless data with continuous DQS_t, DQS_c toggle is shown in Figure 8 (page 22).
- ^{t}CCD > 4 to the same logical rank (SLR) or different logical rank (DLR). An example of a standard ^{t}WPRE and ^{t}WPST with each associated WRITE burst is shown in Figure 9 (page 22).

Figure 8: WRITE BL8 to WRITE BL8 (^{t}CCD = 4) Example



Notes: 1. BL8, WL = 5 (CWL = 5, AL = 0).
2. D_{IN} = data-in.

Figure 9: WRITE BL8 to WRITE BL8 (^{t}CCD > 4) Example



Notes: 1. BL8, WL = 5 (CWL = 5, AL = 0).
2. D_{IN} = data-in.

CCMTD-1725822587-10122
16gb_32gb_3ds.pdf - Rev. C 02/19 EN

PRECHARGE Commands

PRECHARGE and PRECHARGE ALL commands affect only the die (logical rank) selected by the state of the C[2:0] pins. All precharge timings for a given logical of the 3DS device are the same as those shown in the standard DDR4 SDRAM data sheet.

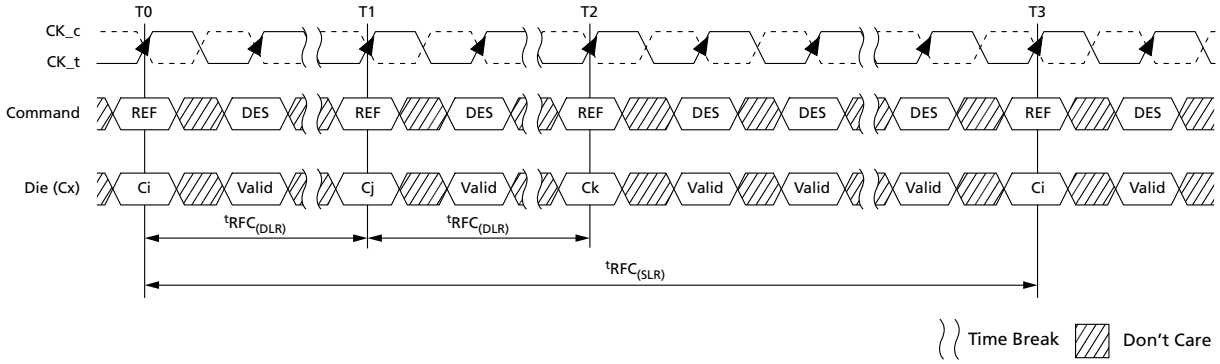
REFRESH Operation

REFRESH operation for each die (logical rank) of the 3DS device follows the standard for a DDR4 SDRAM device. Each logical rank, selected by the state of the C[2:0] pins, must receive REFRESH commands that meet the standard ^{t}REFI interval and ^{t}RFC recovery time. The minimum time between issuing REFRESH commands to different logical ranks is specified as $^{t}RFC_{(DLR)}$. After a REFRESH command to a logical rank, other valid commands (including ACTIVATE commands) can be issued to other logical ranks which are not the target of the REFRESH command before tRFC_dlr expires. REFRESH operations on one rank may overlap the REFRESH operations on another rank, subject to $^{t}RFC_{(DLR)}$. See Table 14.

Table 14: Refresh Timing Parameters

Symbol	Description		8Gb per Rank	Units
$^{t}RFC_{(SLR1)}$	Refresh-to-Refresh (same logical rank, 1X mode)		350	ns
$^{t}RFC_{(SLR2)}$	Refresh-to-Refresh (same logical rank, 2X mode)		260	ns
$^{t}RFC_{(SLR4)}$	Refresh-to-Refresh (same logical rank, 4X mode)		160	ns
$^{t}RFC_{(DLR1)}$	Refresh-to-Refresh (different logical rank,1X mode)		120	ns
$^{t}RFC_{(DLR2)}$	Refresh-to-Refresh (different logical rank, 2X mode)		90	ns
$^{t}RFC_{(DLR4)}$	Refresh-to-Refresh (different logical rank, 4X mode)		55	ns
$^{t}REFI_{(SLR1)}$	Average time between REFRESH commands (same logical rank, 1X mode)	0°C ≤ T_{CASE} ≤ 85°C	7.8	µS
		85°C ≤ T_{CASE} ≤ 95°C	3.9	µS
$^{t}REFI_{(SLR2)}$	Average time between REFRESH commands (same logical rank, 2X mode)	0°C ≤ T_{CASE} ≤ 85°C	3.9	µS
		85°C ≤ T_{CASE} ≤ 95°C	1.95	µS
$^{t}REFI_{(SLR4)}$	Average time between REFRESH commands (same logical rank, 4X mode)	0°C ≤ T_{CASE} ≤ 85°C	1.95	µS
		85°C ≤ T_{CASE} ≤ 95°C	0.975	µS

Figure 10: REFRESH-to-REFRESH Command Timing Example



SELF REFRESH Operation

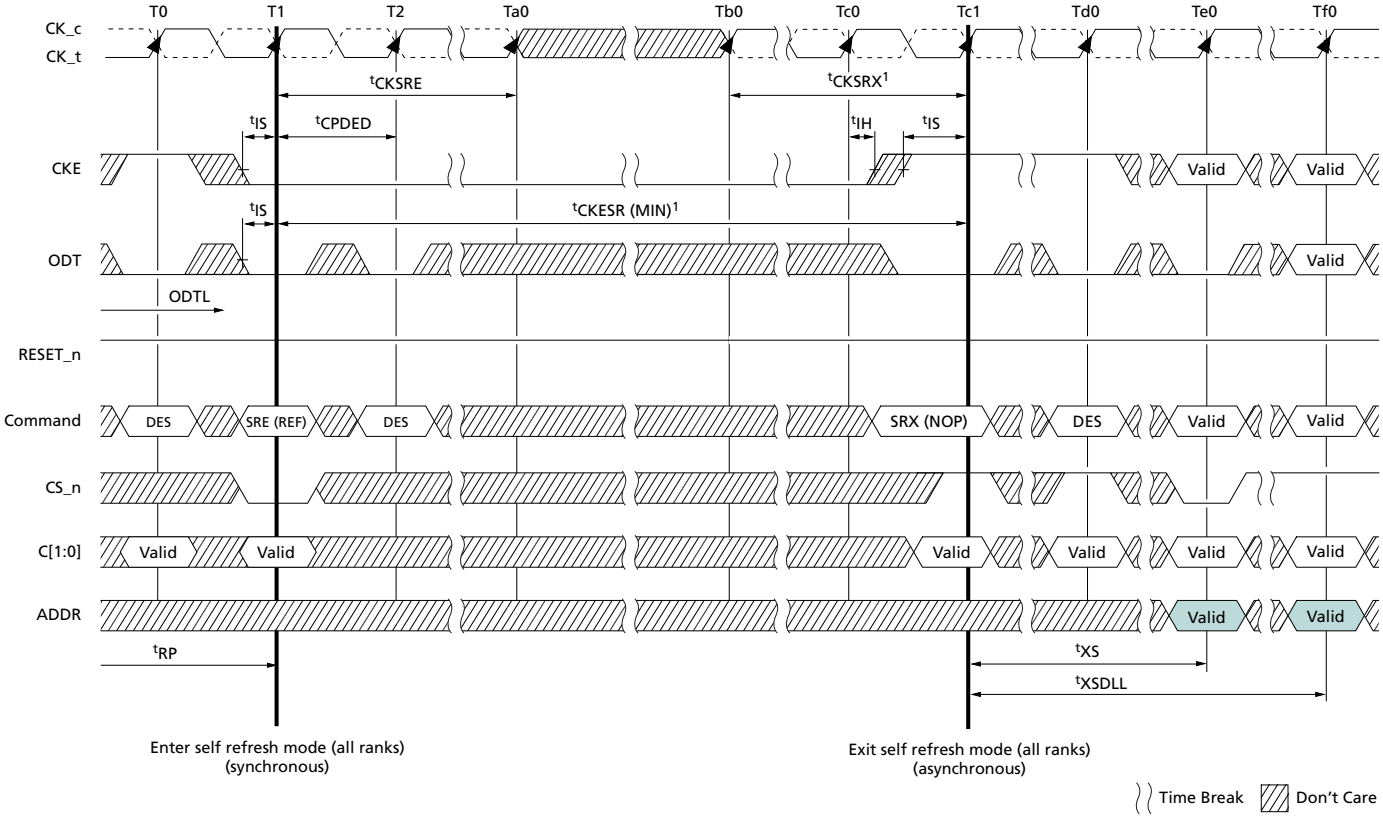
Placing the 3DS device into self refresh mode requires that all ranks (C[1:0]=00, 01, 10...) have been provided PRECHARGE commands and ^{t}RP has been satisfied. SELF REFRSH entry/exit operation and timing requirements follow the standards shown in the Micron DDR4 SDRAM specification.

Table 15: Allowable SELF REFRESH Commands

RAS	CAS	WE	CS_n	C[1:0]	Logical Rank 0	Logical Rank 1	Logical Rank 2	Logical Rank 3
L	L	H	L	VV	Performs SRE	Performs SRE	Performs SRE	Performs SRE
L	L	H	H	VV	Performs PDE	Performs PDE	Performs PDE	Performs PDE

Notes:
1. H = High logic level, L = Low logic level, V = Either H or L (but a defined logic level).
2. If CS_n is not active, the 3DS device ignores the SELF REFRESH command and instead enters the applicable power-down state.

Figure 11: SELF REFRESH Command Timing Example



Note: 1. After tXS has completed, a valid command can be issued to any logical rank (C[1:0]=00,01,10...).

Power-Down Operations

Because the 3DS device has a single CKE input, each rank must be in a valid state prior to toggling CKE LOW. Actual power-down operation follows the standard DDR4 SDRAM specification. Power-down is synchronously entered when CKE is registered LOW coincident with a NOP or DES command. CKE is not allowed to go LOW while an MRS, MPR, ZQCAL, READ, or WRITE operation is in progress to any rank. Each logical rank may be in precharge power-down or active power-down state(s).

On-Die Termination (ODT)

Due to a common external interface, the 3DS device only has a single on-die termination (ODT) ball at location L4. When the ODT feature is enabled via the appropriate MRS setting(s), the ODT input at location L4 is active for any logical rank C[2:0] pin.

DRAM Package Electrical Specifications

Table 16: DRAM Provisional Package Electrical Specifications for x4 and x8 3DS Devices

Parameter		Symbol	1600/1866/2133/2400/2666		2933		3200		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Input/output	Zpkg	Z_{IO}	45	85	48	85	48	85	ohm	1, 2, 4
	Package delay	Td_{IO}	14	42	14	40	14	40	ps	1, 3, 4
	Lpkg	L_{IO}	–	3.3	–	3.3	–	3.3	nH	
	Cpkg	C_{IO}	–	0.78	–	0.78	–	0.78	pF	
DQS_t, DQS_c	Zpkg	$Z_{IO\ DQS}$	45	85	48	85	48	85	ohm	1, 2
	Package delay	$Td_{IO\ DQS}$	14	42	14	40	14	40	ps	1, 3
	Delta Zpkg	$DZ_{IO\ DQS}$	–	10	–	10	–	10	ohm	1, 2, 5
	Delta delay	$DTd_{IO\ DQS}$	–	5	–	5	–	5	ps	1, 3, 5
	Lpkg	$L_{IO\ DQS}$	–	3.3	–	3.3	–	3.3	nH	
	Cpkg	$C_{IO\ DQS}$	–	0.78	–	0.78	–	0.78	pF	
Input CTRL pins	Zpkg	$Z_{I\ CTRL}$	40	80	40	80	40	80	ohm	1, 2, 6
	Package delay	$Td_{I\ CTRL}$	14	42	14	40	14	40	ps	1, 3, 6
	Lpkg	$L_{I\ CTRL}$	–	3.4	–	3.4	–	3.4	nH	
	Cpkg	$C_{I\ CTRL}$	–	0.7	–	0.7	–	0.7	pF	
Input CMD ADD pins	Zpkg	$Z_{I\ ADD\ CMD}$	40	80	40	80	40	80	ohm	1, 2, 7
	Package delay	$Td_{I\ ADD\ CMD}$	14	45	14	40	14	40	ps	1, 3, 7
	Lpkg	$L_{I\ ADD\ CMD}$	–	3.6	–	3.6	–	3.6	nH	
	Cpkg	$C_{I\ ADD\ CMD}$	–	0.74	–	0.74	–	0.74	pF	
CK_t, CK_c	Zpkg	Z_{CK}	40	80	40	80	40	80	ohm	1, 2
	Package delay	Td_{CK}	14	42	14	42	14	42	ps	1, 3
	Delta Zpkg	DZ_{DCK}	–	10	–	10	–	10	ohm	1, 2, 8
	Delta delay	DTd_{DCK}	–	5	–	5	–	5	ps	1, 3, 8
	Lpkg	$L_{I\ CK}$	–	3.4	–	3.4	–	3.4	nH	
	Cpkg	$C_{I\ CK}$	–	0.7	–	0.7	–	0.7	pF	
ZQ Zpkg		$Z_{O\ ZQ}$	–	100	–	100	–	100	ohm	1, 2
ZQ delay		$Td_{O\ ZQ}$	20	90	20	90	20	90	ps	1, 3
ALERT Zpkg		$Z_{O\ ALERT}$	40	100	40	100	40	100	ohm	1, 2
ALERT delay		$Td_{O\ ALERT}$	20	55	20	55	20	55	ps	1, 3

Notes:
1. The package parasitic (L and C) are validated using package only samples. The capacitance is measured with V_{DD}, V_{DDQ}, V_{SS} and V_{SSQ} shorted with all other signal pins floating. The inductance is measured with V_{DD}, V_{DDQ}, V_{SS}, and V_{SSQ} shorted and all other signal pins shorted at the die, not pin, side.
2. Package-only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where: Zpkg (total per pin) = SQRT (Lpkg/Cpkg).
3. Package-only delay (Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where: Tdpkg (total per pin) = SQRT (Lpkg × Cpkg).
4. Z_{IO} and Td_{IO} apply to DQ, DM, DQS_c, DQS_t, TDQS_t, and TDQS_c.

5. Absolute value of ZIO (DQS_t), ZIO (DQS_c) for impedance (Z) or absolute value of TdIO (DQS_t), TdIO (DQS_c) for delay (Td).
6. $Z_{I\ CTRL}$ and $Td_{I\ CTRL}$ apply to ODT, CS_n, CKE, and C0 if 2H, C0 and C1 if 4H, and C0, C1, and C2 if 8H.
7. $Z_{I\ ADD\ CMD}$ and $Td_{I\ ADD\ CMD}$ apply to A[17:0], BA[1:0], BG[1:0], PAR, RAS_n CAS_n, and WE_n.
8. Absolute value of ZCK_t, ZCK_c for impedance (Z) or absolute value of TdCK_t, TdCK_c for delay (Td).
9. Package implementations will meet specification if the Zpkg and package delay fall within the ranges shown, and the maximum Lpkg and Cpkg do not exceed the maximum values shown.
10. It is assumed that Lpkg can be approximated as $Lpkg = Z_O \times Td$.
11. It is assumed that Cpkg can be approximated as $Cpkg = Td/Z_O$.

Table 17: Pad Input/Output Provisional Capacitance for x4 and x8 3DS Devices

Parameter	Symbol	DDR4-1600, 1866, 2133		DDR4-2400, 2666		DDR4-2933		DDR4-3200		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Input/output capacitance: DQ, DM, DQS_t, DQS_c, TDQS_t, TDQS_c	C_{IO}	0.55	1.4	0.55	1.15	0.55	1.0	0.55	1.0	pF	1, 2, 3
Input capacitance: CK_t and CK_c	C_{CK}	0.2	0.8	0.2	0.7	0.2	0.7	0.2	0.7	pF	1, 2, 3, 4
Input capacitance delta: CK_t and CK_c	C_{DCK}	0.0	0.05	0.0	0.05	0.0	0.05	0.0	0.05	pF	1, 2, 3, 5
Input/output capacitance delta: DQS_t and DQS_c	C_{DDQS}	0.0	0.05	0.0	0.05	0.0	0.05	0.0	0.05	pF	1, 2, 3
Input capacitance: CTRL, ADD, CMD input-only pins	C_I	0.2	0.8	0.2	0.7	0.2	0.6	0.2	0.55	pF	1, 2, 3, 6
Input capacitance delta: All CTRL input-only pins	C_{DI_CTRL}	–0.1	0.1	–0.1	0.1	–0.1	0.1	–0.1	0.1	pF	1, 2, 3, 7
Input capacitance delta: All ADD/CMD input-only pins	$C_{DI\_ADD\_CMD}$	–0.1	0.1	–0.1	0.1	–0.1	0.1	–0.1	0.1	pF	1, 2, 3, 8, 9
Input/output capacitance delta: DQ, DM, DQS_t, DQS_c, TDQS_t, TDQS_c	C_{DIO}	–0.1	0.1	–0.1	0.1	–0.1	0.1	–0.1	0.1	pF	1, 2, 10, 11
Input/output capacitance: ALERT pin	C_{ALERT}	0.5	1.5	0.5	1.5	0.5	1.5	0.5	1.5	pF	1, 2, 2, 3
Input/output capacitance: ZQ pin	C_{ZQ}	0.0	2.3	0.0	2.3	0.0	2.3	0.0	2.3	pF	1, 2, 3, 12
Input/output capacitance: TEN pin	C_{TEN}	0.2	2.3	0.2	2.3	0.2	2.3	0.2	2.3	pF	1, 2, 3, 13

Notes:
1. Although the DM, TDQS_t, and TDQS_c pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to a production test; it is verified by design and characterization. The capacitance is measured according to the JEP147 specification, "Procedure for Measuring Input Capacitance Using a Vector Network Analyzer (VNA)," with V_{DD}, V_{DDQ}, V_{SS} and V_{SSQ} applied and all other pins floating (except the pin under test, CKE, RESET_n and ODT, as necessary). $V_{DD} = V_{DDQ} = 1.2V$, $V_{BIAS} = V_{DD}/2$ and on-die termination off. Measured data is rounded using industry standard half-rounded up methodology to the nearest hundredth of the MSB.
3. This parameter applies to monolithic die, obtained by de-embedding the package L and C parasitics.
4. $C_{DIO} = C_{IO}(DQ, DM) - 0.5 \times (C_{IO}(DQS\_t) + C_{IO}(DQS\_c))$.
5. Absolute value of C_{IO} (DQS_t), C_{IO} (DQS_c)
6. Absolute value of CCK_t, CCK_c
7. C_I applies to ODT, CS_n, CKE, and C0 if 2H, C0 and C1 if 4H, and C0, C1, and C2 if 8H, A[17:0], BA[1:0], BG[1:0], PAR, RAS_n, CAS_n, and WE_n.
8. C_{DI_CTRL} apply to ODT, CS_n, CKE, and C0 if 2H, C0 and C1 if 4H, and C0, C1, and C2 if 8H.
9. $C_{DI\_CTRL} = C_I(CTRL) - 0.5 \times (C_I(CK\_t) + C_I(CK\_c))$.

10. $C_{DI\_ADD\_CMD}$ applies to A[17:0], BA[1:0], BG[1:0], PAR, RAS_n, CAS_n, and WE_n.
11. $C_{DI\_ADD\_CMD} = C_I(ADD\_CMD) - 0.5 \times (C_I(CK\_t) + C_I(CK\_c))$.
12. Maximum external load capacitance on ZQ pin: 5pF.
13. Only applicable if TEN pin does not have an internal pull-up.

Speed Bin Tables

The speed bin tables below list the ^{t}AA, ^{t}RCD, ^{t}RP, ^{t}RAS, and ^{t}RC limits of a given speed mark and are applicable to the CL settings in the lower half of the table provided they are applied in the correct clock range, which is noted.

Table 18: DDR4-1600 3DS Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-1600 3DS Speed Bin						-125J		-125H		-125G		
CL-*n*RCD-*n*RP						12-11-10		13-12-11		14-13-12		
Parameter					Symbol	Min	Max	Min	Max	Min	Max	Unit
Internal READ command to first data					^{t}AA	15.00	27.00[6]	16.25	27.00[6]	17.50	27.00[6]	ns
ACTIVATE to internal READ or WRITE delay time					^{t}RCD	13.75	–	15.00	–	16.25	–	ns
PRECHARGE command period					^{t}RP	12.50	–	13.75	–	15.00	–	ns
ACTIVATE-to-PRECHARGE command period					^{t}RAS	35	9 × ^{t}REFI	35	9 × ^{t}REFI	35	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period					^{t}RC[5]	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	ns
Data Rate Max (MT/s)	**Equivalent Speed Bin**	**^{t}AAmin (ns)**	**READ CL**	**WRITE CWL**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
1600	-125J	15.00	12	9, 11	^{t}CK (AVG)	1.250	1.900[6]	Reserved		Reserved		ns
	-125H	16.25	13		^{t}CK (AVG)			1.250	1.900[6]			ns
	-125G	17.50	14		^{t}CK (AVG)					1.250	1.900[6]	ns
Supported CL settings						12–14		13-14		14		*n*CK
Supported CWL settings						9, 11		9, 11		9, 11		*n*CK

CCMTD-1725822587-10122
16gb_32gb_3ds.pdf - Rev. C 02/19 EN

Notes:
1. Speed Bin table is only valid with DLL enabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native ^{t}CK-CL-*n*RCD-*n*RP combinations.
5. When calculating ^{t}RC in clocks, values may not be used in a combination that violate ^{t}RAS or ^{t}RP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Table 19: DDR4-1866 3DS Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-1866 3DS Speed Bin						-107J		-107H		-107G		
CL-*n*RCD-*n*RP						14-13-12		15-14-13		16-15-14		
Parameter					Symbol	Min	Max	Min	Max	Min	Max	Unit
Internal READ command to first data					^{t}AA	15.00	27.00[6]	16.07	27.00[6]	17.14	27.00[6]	ns
ACTIVATE to internal READ or WRITE delay time					^{t}RCD	13.92 (13.75)[4]	–	15.0	–	16.07	–	ns
PRECHARGE command period					^{t}RP	12.85 (12.50)[4]	–	13.92 (13.75)[4]	–	15.00	–	ns
ACTIVATE-to-PRECHARGE command period					^{t}RAS	34	9 × ^{t}REFI	34	9 × ^{t}REFI	34	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period					^{t}RC[5]	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	ns
Data Rate Max (MT/s)	**Equivalent Speed Bin**	**^{t}AAmin (ns)**	**READ CL**	**WRITE CWL**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
1600	-125J	15.00	12	9, 11	^{t}CK (AVG)	1.250	1.900[6]	Reserved		Reserved		ns
	-125H	16.25	13		^{t}CK (AVG)			1.250	1.900[6]			ns
	-125G	17.50	14		^{t}CK (AVG)					1.250	1.900[6]	ns
1866	-107J	15.00	14	10, 12	^{t}CK (AVG)	1.071	<1.250	Reserved		Reserved		ns
	-107H	16.07	15		^{t}CK (AVG)			1.071	<1.250			ns
	-107G	17.14	16		^{t}CK (AVG)					1.071	<1.250	ns
Supported CL settings						12–16		13–16		14, 16		*n*CK
Supported CWL settings						9–12		9–12		9–12		*n*CK

CCMTD-1725822587-10122
16gb_32gb_3ds.pdf - Rev. C 02/19 EN

Notes:
1. Speed Bin table is only valid with DLL enabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native ^{t}CK-CL-*n*RCD-*n*RP combinations.
5. When calculating ^{t}RC in clocks, values may not be used in a combination that violate ^{t}RAS or ^{t}RP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Table 20: DDR4-2133 3DS Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-2133 3DS Speed Bin						-093J		-093H		-093G		Unit
CL-*n*RCD-*n*RP						17-15-15		18-15-15		20-16-16		
Parameter					Symbol	Min	Max	Min	Max	Min	Max	
Internal READ command to first data					^{t}AA	15.95	27.00[6]	16.88	27.00[6]	18.76 (17.14)[4]	27.00[6]	ns
ACTIVATE to internal READ or WRITE delay time					^{t}RCD	14.06	–	14.06	–	15.00	–	ns
PRECHARGE command period					^{t}RP	14.06 (13.75)[4]	–	14.06	–	15.00	–	ns
ACTIVATE-to-PRECHARGE command period					^{t}RAS	33	9 × ^{t}REFI	33	9 × ^{t}REFI	33	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period					^{t}RC[5]	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	ns
Data Rate Max (MT/s)	**Equivalent Speed Bin**	**^{t}AAmin (ns)**	**READ CL**	**WRITE CWL**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
1600	-125J	15.00	12	9, 11	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-125H	16.25	13		^{t}CK (AVG)	1.250	1.900[6]					ns
	-125G	17.50	14		^{t}CK (AVG)			1.250	1.900[6]	1.250	1.900[6]	ns
1866	-107J	15.00	14	10, 12	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-107H	16.07	15		^{t}CK (AVG)	1.071	<1.250					ns
	-107G	17.14	16		^{t}CK (AVG)			1.071	<1.250	1.071	<1.250	ns
2133	-093J	15.95	17	11, 14	^{t}CK (AVG)	0.937	<1.071	Reserved		Reserved		ns
	-093H	16.88	18		^{t}CK (AVG)			0.937	<1.071			ns
	-093G	18.76	20		^{t}CK (AVG)					0.937	<1.071	ns
Supported CL settings						13–18, 20		14, 16, 18, 20		14, 16, 20		*n*CK
Supported CWL settings						9–12, 14		9–12, 14		9–12, 14		*n*CK

CCMTD-1725822587-10122
16gb_32gb_3ds.pdf - Rev. C 02/19 EN

Notes:
1. Speed Bin table is only valid with DLL enabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native ^{t}CK-CL-*n*RCD-*n*RP combinations.
5. When calculating ^{t}RC in clocks, values may not be used in a combination that violate ^{t}RAS or ^{t}RP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Table 21: DDR4-2400 3DS Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-2400 3DS Speed Bin						-083J		-083H		-083G		
CL-*n*RCD-*n*RP						19-17-17		20-17-17		22-18-18		
Parameter					Symbol	Min	Max	Min	Max	Min	Max	Unit
Internal READ command to first data					^{t}AA	15.83	27.00[6]	16.67	27.00[6]	18.33 (17.14)[4]	27.00[6]	ns
ACTIVATE to internal READ or WRITE delay time					^{t}RCD	14.16 (14.06)[4]	–	14.16 (14.06)[4]	–	15.00	–	ns
PRECHARGE command period					^{t}RP	14.16 (13.75)[4]	–	14.16 (14.06)[4]	–	15.00	–	ns
ACTIVATE-to-PRECHARGE command period					^{t}RAS	32	9 × ^{t}REFI	32	9 × ^{t}REFI	32	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period					^{t}RC[5]	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	ns
Data Rate Max (MT/s)	**Equivalent Speed Bin**	**^{t}AAmin (ns)**	**READ CL**	**WRITE CWL**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
1600	-125J	15.00	12	9, 11	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-125H	16.25	13		^{t}CK (AVG)	1.25	1.9[6]					ns
	-125G	17.50	14		^{t}CK (AVG)			1.25	1.9[6]	1.25	1.9[6]	ns
1866	-107J	15.00	14	10, 12	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-107H	16.07	15		^{t}CK (AVG)	1.071	<1.25					ns
	-107G	17.14	16		^{t}CK (AVG)			1.071	<1.25	1.071	<1.25	ns
2133	-093J	15.95	17	11, 14	^{t}CK (AVG)	0.937	<1.071	Reserved		Reserved		ns
	-093H	16.88	18		^{t}CK (AVG)			0.937	<1.071			ns
	-093G	18.76	20		^{t}CK (AVG)	Reserved		Reserved		0.937	<1.071	ns
2400	-083J	15.83	19	12,16	^{t}CK (AVG)	0.833	<0.937	Reserved		Reserved		ns
	-083H	16.67	20		^{t}CK (AVG)			0.833	<0.937			ns
	-083G	18.33	22		^{t}CK (AVG)	Reserved		Reserved		0.833	<0.937	ns
Supported CL settings						13–20		14, 16, 18, 20		14, 16, 20, 22		*n*CK
Supported CWL settings						9–12, 14, 16		9–12, 14, 16		9–12, 14, 16		*n*CK

CCMTD-1725822587-10122
16gb_32gb_3ds.pdf - Rev. C 02/19 EN

Notes:
1. Speed Bin table is only valid with DLL enabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native ^{t}CK-CL-*n*RCD-*n*RP combinations.
5. When calculating ^{t}RC in clocks, values may not be used in a combination that violate ^{t}RAS or ^{t}RP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Table 22: DDR4-2666 3DS Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-2666 3DS Speed Bin						-075J		-075H		-075G		
CL-*n*RCD-*n*RP						20-17-17		22-19-19		24-20-20		
Parameter					Symbol	Min	Max	Min	Max	Min	Max	Unit
Internal READ command to first data					^{t}AA	15.00	27.00[6]	16.50	27.00[6]	18.00 (17.14)[4]	27.00[6]	ns
ACTIVATE to internal READ or WRITE delay time					^{t}RCD	12.75	–	14.25 (14.06)[4]	–	15.00	–	ns
PRECHARGE command period					^{t}RP	12.75	–	14.25 (14.06)[4]	–	15.00	–	ns
ACTIVATE-to-PRECHARGE command period					^{t}RAS	32	9 × ^{t}REFI	32	9 × ^{t}REFI	32	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period					^{t}RC[5]	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	ns
Data Rate Max (MT/s)	**Equivalent Speed Bin**	**^{t}AAmin (ns)**	**READ CL**	**WRITE CWL**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
1600	-125J	15.00	12	9, 11	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-125H	16.25	13		^{t}CK (AVG)	1.25	1.9[6]					ns
	-125G	17.50	14		^{t}CK (AVG)			1.25	1.9[6]	1.25	1.9[6]	ns
1866	-107J	15.00	14	10, 12	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-107H	16.07	15		^{t}CK (AVG)	1.071	<1.25					ns
	-107G	17.14	16		^{t}CK (AVG)			1.071	<1.25	1.071	<1.25	ns
2133	-093J	15.95	17	11, 14	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-093H	16.88	18		^{t}CK (AVG)	0.937	<1.071	0.937	<1.071			ns
	-093G	18.76	20		^{t}CK (AVG)					0.937	<1.071	ns
2400	-083J	15.83	19	12, 16	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-083H	16.67	20		^{t}CK (AVG)	0.833	<0.937	0.833	<0.937			ns
	-083G	18.33	22		^{t}CK (AVG)					0.833	<0.937	ns
2666	-075J	15.00	20	14, 18	^{t}CK (AVG)	0.750	<0.833	Reserved		Reserved		ns
	-075H	16.50	22		^{t}CK (AVG)			0.750	<0.833			ns
	-075G	18.00	24		^{t}CK (AVG)					0.750	<0.833	ns
Supported CL settings						13–16, 18, 20, 22, 24		14, 16, 18, 20, 22, 24		14, 16, 20, 22, 24		*n*CK
Supported CWL settings						9-12, 14, 16, 18		9-12, 14, 16, 18		9-12, 14, 16, 18		*n*CK

CCMTD-1725822587-10122
16gb_32gb_3ds.pdf - Rev. C 02/19 EN

Notes:
1. Speed Bin table is only valid with DLL enabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native ^{t}CK-CL-*n*RCD-*n*RP combinations.
5. When calculating ^{t}RC in clocks, values may not be used in a combination that violate ^{t}RAS or ^{t}RP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Table 23: DDR4-2933 3DS Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-2933 3DS Speed Bin						-068J		-068H		-068G		
CL-*n*RCD-*n*RP						23-20-20		24-21-21		25-22-22		
Parameter					Symbol	Min	Max	Min	Max	Min	Max	Unit
Internal READ command to first data					^{t}AA	15.69	27.00[6]	16.37	27.00[6]	17.05	27.00[6]	ns
ACTIVATE to internal READ or WRITE delay time					^{t}RCD	13.64	–	14.32 (14.06)[4]	–	15.00	–	ns
PRECHARGE command period					^{t}RP	13.64	–	14.32 (14.06)[4]	–	15.00	–	ns
ACTIVATE-to-PRECHARGE command period					^{t}RAS	32	9 × ^{t}REFI	32	9 × ^{t}REFI	32	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period					^{t}RC[5]	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	ns
Data Rate Max (MT/s)	**Equivalent Speed Bin**	**^{t}AAmin (ns)**	**READ CL**	**WRITE CWL**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
1600	-125J	15.00	12	9, 11	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-125H	16.25	13		^{t}CK (AVG)	1.250	1.900[6]					ns
	-125G	17.50	14		^{t}CK (AVG)			1.250	1.900[6]	1.250	1.900[6]	ns
1866	-107J	15.00	14	10, 12	^{t}CK(AVG)	Reserved		Reserved		Reserved		ns
	-107H	16.07	15		^{t}CK(AVG)	1.071	<1.250					ns
	-107G	17.14	16		^{t}CK (AVG)			1.071	<1.250	1.071	<1.250	ns
2133	-093J	15.95	17	11, 14	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-093H	16.88	18		^{t}CK (AVG)	0.937	<1.071	0.937	<1.071			ns
	-093G	18.76	20		^{t}CK (AVG)					0.937	<1.071	ns
2400	-083J	15.83	19	12, 16	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-083H	16.67	20		^{t}CK (AVG)	0.833	<0.937	0.833	<0.937			ns
	-083G	18.33	22		^{t}CK (AVG)					0.833	<0.937	ns
2666	-075J	15.00	20	14, 18	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-075H	16.50	22		^{t}CK (AVG)	0.750	<0.833	0.750	<0.833			ns
	-075G	18.00	24		^{t}CK (AVG)					0.750	<0.833	ns
2933	-068J	15.69	23	16, 20	^{t}CK (AVG)	0.682	<0.750	Reserved		Reserved		ns
	-068H	16.37	24		^{t}CK (AVG)			0.682	<0.750			ns
	-068G	17.05	25		^{t}CK (AVG)					0.682	<0.750	ns
Supported CL settings						13–16, 18, 20, 22–25		14, 16, 18, 20, 22, 24-25		14, 16, 20, 22, 24-25		*n*CK

CCMTD-1725822587-10122
16gb_32gb_3ds.pdf - Rev. C 02/19 EN

Table 23: DDR4-2933 3DS Speed Bins and Operating Conditions (Continued)

Notes 1–3 apply to the entire table

DDR4-2933 3DS Speed Bin		-068J		-068H		-068G		
CL-*n*RCD-*n*RP		23-20-20		24-21-21		25-22-22		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit
Supported CWL settings		9-12, 14, 16, 18, 20		9-12, 14, 16, 18, 20		9-12, 14, 16, 18, 20		*n*CK

CCMTD-1725822587-10122
16gb_32gb_3ds.pdf - Rev. C 02/19 EN

Notes:
1. Speed Bin table is only valid with DLL enabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native ^{t}CK-CL-*n*RCD-*n*RP combinations.
5. When calculating ^{t}RC in clocks, values may not be used in a combination that violate ^{t}RAS or ^{t}RP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Table 24: DDR4-3200 3DS Speed Bins and Operating Conditions

Notes 1–3 apply to the entire table

DDR4-3200 3DS Speed Bin						-062J		-062H		-062G		
CL-*n*RCD-*n*RP						24-20-20		26-22-22		28-24-24		
Parameter					Symbol	Min	Max	Min	Max	Min	Max	Unit
Internal READ command to first data					^{t}AA	15.00	27.00[6]	16.25	27.00[6]	17.50 (17.14)[4]	27.00[6]	ns
ACTIVATE to internal READ or WRITE delay time					^{t}RCD	12.50	–	13.75	–	15.00	–	ns
PRECHARGE command period					^{t}RP	12.50	–	13.75	–	15.00	–	ns
ACTIVATE-to-PRECHARGE command period					^{t}RAS	32	9 × ^{t}REFI	32	9 × ^{t}REFI	32	9 × ^{t}REFI	ns
ACTIVATE-to-ACTIVATE or REFRESH command period					^{t}RC[5]	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	^{t}RAS + ^{t}RP	–	ns
Data Rate Max (MT/s)	**Equivalent Speed Bin**	**^{t}AAmin (ns)**	**READ CL**	**WRITE CWL**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
1600	-125J	15.00	12	9, 11	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-125H	16.25	13		^{t}CK (AVG)	1.250	1.900[6]	1.250	1.900[6]			ns
	-125G	17.50	14		^{t}CK (AVG)					1.25	1.900[6]	ns
1866	-107J	15.00	14	10, 12	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-107H	16.07	15		^{t}CK (AVG)	1.071	<1.250					ns
	-107G	17.14	16		^{t}CK (AVG)			1.071	<1.250	1.071	<1.250	ns
2133	-093J	15.95	17	11, 14	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-093H	16.88	18		^{t}CK (AVG)	0.937	<1.071	0.937	<1.071			ns
	-093G	18.76	20		^{t}CK (AVG)					0.937	<1.071	ns
2400	-083J	15.83	19	12, 16	^{t}CK (AVG)	Reserved		Reserved		Reserved		ns
	-083H	16.67	20		^{t}CK (AVG)	0.833	<0.937	0.833	<0.937			ns
	-083G	18.33	22		^{t}CK (AVG)					0.833	<0.937	ns
2666	-075J	15.00	20	14, 18	^{t}CK (AVG)	0.750	<0.833	Reserved		Reserved		ns
	-075H	16.50	22		^{t}CK (AVG)			0.750	<0.833			ns
	-075G	18.00	24		^{t}CK (AVG)					0.750	<0.833	ns
2933	-068J	15.69	23	16, 20	^{t}CK (AVG)	0.682	<0.750	Reserved		Reserved		ns
	-068H	16.37	24		^{t}CK (AVG)			0.682	<0.750			ns
	-068G	17.05	25		^{t}CK (AVG)							ns
	-	17.74	26		^{t}CK (AVG)					0.682	<0.750	ns
	-	19.10	28		^{t}CK (AVG)							ns

Table 24: DDR4-3200 3DS Speed Bins and Operating Conditions (Continued)

Notes 1–3 apply to the entire table

DDR4-3200 3DS Speed Bin						-062J		-062H		-062G		
CL-*n*RCD-*n*RP						24-20-20		26-22-22		28-24-24		
Parameter					Symbol	Min	Max	Min	Max	Min	Max	Unit
3200	-062J	15.00	24	16, 20	^{t}CK (AVG)	0.625	<0.682	Reserved		Reserved		ns
	-062H	16.25	26		^{t}CK (AVG)			0.625	<0.682			ns
	-062G	17.50	28		^{t}CK (AVG)					0.625	<0.682	ns
Supported CL settings						13–16, 18, 20, 22, 23-26, 28		13-14, 16, 18, 20, 22, 24-26, 28		14, 16, 20, 22, 24, 26, 28		*n*CK
Supported CWL settings						9-12, 14, 16, 18, 20		9-12, 14, 16, 18, 20		9-12, 14, 16, 18, 20		*n*CK

CCMTD-1725822587-10122
16gb_32gb_3ds.pdf - Rev. C 02/19 EN

Notes:
1. Speed Bin table is only valid with DLL enabled.
2. When operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.
3. The programmed value of CWL must be less than or equal to the programmed value of CL.
4. This value applies to non-native ^{t}CK-CL-*n*RCD-*n*RP combinations.
5. When calculating ^{t}RC in clocks, values may not be used in a combination that violate ^{t}RAS or ^{t}RP.
6. This value exceeds the JEDEC requirement in order to allow additional flexibility, especially for components. However, JEDEC SPD compliance may force modules to only support the JEDEC defined value, please refer to the SPD documentation.

Current Specifications – Measurement Conditions

I_{DD}, I_{PP}, and I_{DDQ} Measurement Conditions

- I_{DD} currents (I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2P}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, I_{DD5B1}, I_{DD5B2}, I_{DD6N}, I_{DD6E}, I_{DD6R}, I_{DD6A}, I_{DD7}, and I_{DD8}) are measured as time-averaged currents with all V_{DD} balls of the device under test grouped together.
- I_{PP} currents are I_{PP3N} for standby cases (I_{DD2N}, I_{DD2NT}, I_{DD2P}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD8}), I_{PP0} for active cases (I_{DD0},I_{DD1}, I_{DD4R}, I_{DD4W}), I_{PP5B1} and I_{PP5B2} for burst-refresh cases (I_{DD5B1} and I_{DD5B2}), I_{PP6x} for self refresh cases (I_{DD6N}, I_{DD6E}, I_{DD6R}, I_{DD6A}) and I_{PP7} for the operating bank interleave read case (I_{DD7}). These have the same definitions as the I_{DD} currents referenced but are measured on the V_{PP} supply.
- I_{DDQ} currents are measured as time-averaged currents with V_{DDQ} balls of the device under test grouped together. Micron does not specify I_{DDQ} currents.
- I_{PP} and I_{DDQ} currents are not included in I_{DD} currents, I_{DD} and I_{DDQ} currents are not included in I_{PP} currents, and I_{DD} and I_{PP} currents are not included in I_{DDQ} currents.

Note: I_{DDQ} values cannot be directly used to calculate the I/O power of the device. They can be used to support correlation of simulated I/O power to actual I/O power. In DRAM module application, I_{DDQ} cannot be measured separately because V_{DD} and V_{DDQ} are using a merged-power layer in the module PCB.

The following definitions apply for I_{DD}, I_{PP} and I_{DDQ} measurements.

- "0" and "LOW" are defined as $V_{IN} \leq V_{IL(AC)max}$
- "1" and "HIGH" are defined as $V_{IN} \geq V_{IH(AC)min}$
- "Midlevel" is defined as inputs $V_{REF} = V_{DD}/2$
- Timings used for I_{DD}, I_{PP} and I_{DDQ} measurement-loop patterns are provided in the Current Test Definition and Patterns section.
- Basic I_{DD}, I_{PP} and I_{DDQ} measurement conditions are described in the Current Test Definition and Patterns section.
- Detailed I_{DD}, I_{PP} and I_{DDQ} measurement-loop patterns are described in the Current Test Definition and Patterns section.
- Current measurements are done after properly initializing the device. This includes, but is not limited to, setting:
  $R_{ON} = R_{ZQ}/7$ (34 ohm in MR1);
  Qoff = 0B (output buffer enabled in MR1);
  $R_{TT(NOM)} = R_{ZQ}/6$ (40 ohm in MR1);
  $R_{TT(WR)} = R_{ZQ}/2$ (120 ohm in MR2);
  $R_{TT(Park)}$ = disabled;
  TDQS Feature disabled in MR1; CRC disabled in MR2; CA parity feature disabled in MR3; Gear-down mode disabled in MR3; DM disabled in MR5
- Define D = {CS_n, RAS_n, CAS_n, WE_n}: = {HIGH, LOW, LOW, LOW}; apply BG/BA changes when directed.
- Define D_n = {CS_n, RAS_n, CAS_n, WE_n}: = {HIGH, HIGH, HIGH, HIGH}; apply invert of BG/BA changes when directed above.

Note: The measurement-loop patterns must be executed at least once before actual current measurements can be taken.

Figure 12: Measurement Setup and Test Load for I_{DDx}, I_{PPx} and I_{DDQx}

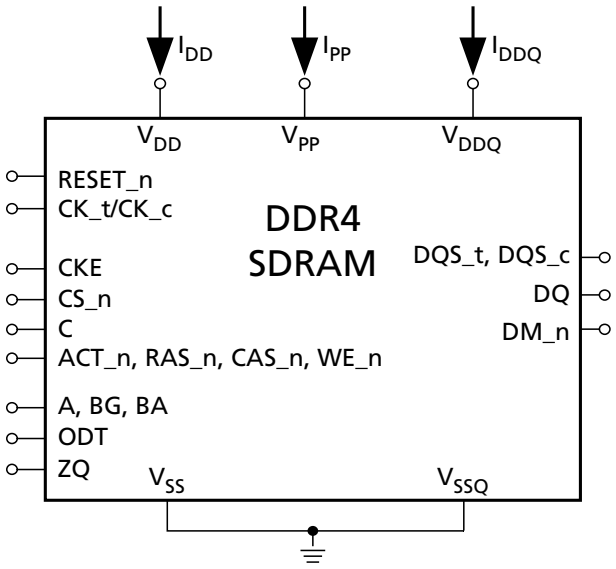
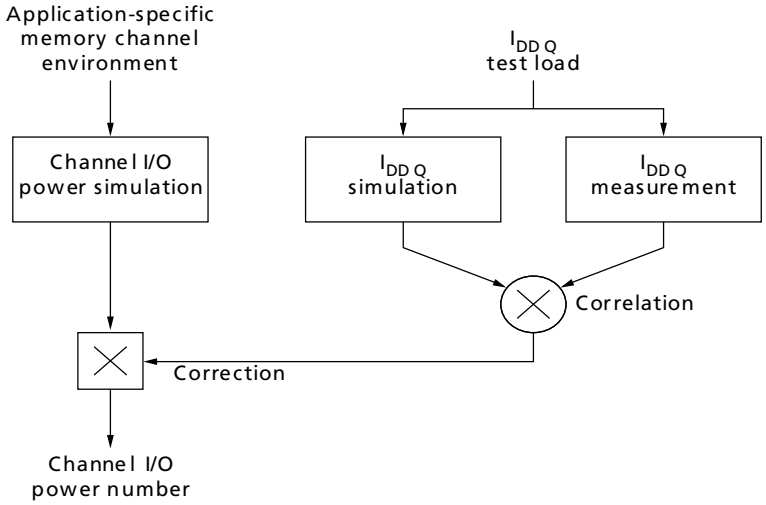


Figure 13: Correlation: Simulated Channel I/O Power to Actual Channel I/O Power



Note: 1. Supported by I_{DDQ} measurement.

I_{DD} Definitions

Table 25: Basic I_{DD}, I_{PP} and I_{DDQ} Measurement Conditions

Symbol	Description
I_{DD0}	**Operating One Bank Active-Precharge Current (AL = 0)** CKE: HIGH; External clock: On; ^{t}CK, *n*RC, *n*RAS, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: HIGH between ACT and PRE; Command, address, bank group address, bank address inputs: partially toggling according to the next table; Data I/O: V_{DDQ}; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see the I_{DD0} Measurement-Loop Pattern table); Logical Rank Activity: Cycling with one logical rank active at a time; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD0} Measurement-Loop Pattern table
I_{PP0}	**Operating One Bank Active-Precharge I_{PP} Current (AL = 0)** Same conditions as I_{DD0} above
I_{DD1}	**Operating One Bank Active-Read-Precharge Current (AL = 0)** CKE: HIGH; External clock: on; ^{t}CK, *n*RC, *n*RAS, *n*RCD, CL: see the previous table; BL: 8;[15] AL: 0; CS_n: HIGH between ACT, RD and PRE; Command, address, bank group address, bank address inputs, Data I/O: partially toggling according to the I_{DD1} Measurement-Loop Pattern table; DM_n: stable at 0; Bank activity: cycling with one bank active at a time: 0, 0, 1, 1, 2, 2, ... (see the following table); Logical Rank Activity: Cycling with one logical rank active at a time; Output buffer and R_{TT}: enabled in mode registers;[2] ODT Signal: stable at 0; Pattern details: see the I_{DD1} Measurement-Loop Pattern table
I_{DD2N}	**Precharge Standby Current (AL = 0)** CKE: HIGH; External clock: On; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address Inputs: partially toggling according to the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table
I_{DD2NT}	**Precharge Standby ODT Current** CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank gropup address, bank address inputs: partially toggling according to the I_{DD2NT} Measurement-Loop Pattern table; Data I/O: V_{SSQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: toggling according to the I_{DD2NT} Measurement-Loop Pattern table; Pattern details: see the I_{DD2NT} Measurement-Loop Pattern table
I_{DD2P}	**Precharge Power-Down Current** CKE: LOW; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0
I_{DD2Q}	**Precharge Quiet Standby Current** CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0
I_{DD3N}	**Active Standby Current (AL = 0)** CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks open; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD2N} and I_{DD3N} Measurement-Loop Pattern table
I_{PP3N}	**Active Standby I_{PP3N} Current (AL = 0)** Same conditions as I_{DD3N} above

Table 25: Basic I_{DD}, I_{PP} and I_{DDQ} Measurement Conditions (Continued)

Symbol	Description
I_{DD3P}	**Active Power-Down Current (AL = 0)** CKE: LOW; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 1; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks open; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0
I_{DD4R}	**Operating Burst Read Current (AL = 0)** CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[15] AL: 0; CS_n: HIGH between RD; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD4R} and I_{DDQ4R} Measurement-Loop Pattern table; Data I/O: seamless read data burst with different data between one burst and the next one according to the I_{DD4R} and I_{DDQ4R} Measurement-Loop Pattern table; DM_n: stable at 1; Bank activity: all banks open, RD commands cycling through banks: 0, 0, 1, 1, 2, 2, ... (see the I_{DD4R} and I_{DDQ4R} Measurement-Loop Pattern table); Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD4R} and I_{DDQ4R} Measurement-Loop Pattern table
I_{DD4W}	**Operating Burst Write Current (AL = 0)** CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: HIGH between WR; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD4W} Measurement-Loop Pattern table; Data I/O: seamless write data burst with different data between one burst and the next one according to the I_{DD4W} Measurement-Loop Pattern table; DM: stable at 1; Bank activity: all banks open, WR commands cycling through banks: 0, 0, 1, 1, 2, 2, ... (see I_{DD4W} Measurement-Loop Pattern table); Output buffer and R_{TT}: enabled in mode registers (see Note 2); ODT signal: stable at HIGH; Pattern details: see the I_{DD4W} Measurement-Loop Pattern table
I_{DD5B1}	**Burst Refresh Current (1X REF)** CKE: HIGH; External clock: on; ^{t}CK, CL, nRFC$_{(DLR)}$: see the previous table; BL: 8;[1] AL: 0; CS_n: HIGH between REF; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD5B1} Measurement-Loop Pattern table; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: REF command every nRFC$_{(DLR)}$ (see the I_{DD5B1} Measurement-Loop Pattern table); Logical Rank Activity: REF command staggered nRFC$_{(DLR)}$ between REF command to REF command; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD5B1} Measurement-Loop Pattern table
I_{PP5B1}	**Burst Refresh Current (1X REF)** Same conditions as I_{DD5B1} above
I_{DD5B2}	**Burst Refresh Current (1X REF)** CKE: HIGH; External clock: on; ^{t}CK, CL, nRFC$_{(SLR)}$: see the previous table; BL: 8;[1] AL: 0; CS_n: HIGH between REF; Command, address, bank group address, bank address inputs: partially toggling according to the I_{DD5B2} Measurement-Loop Pattern table; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: REF command every nRFC$_{(SLR)}$ (see the I_{DD5B2} Measurement-Loop Pattern table); Logical Rank Activity: REF command staggered nRFC$_{(SLR)}$ between REF command to REF command; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD5B2} Measurement-Loop Pattern table
I_{PP5B2}	**Burst Refresh Current (1X REF)** Same conditions as I_{DD5B2} above
I_{DD6N}	**Self Refresh Current: Normal Temperature Range** T_C: 0–85°C; Auto self refresh (ASR): disabled;[3] Self refresh temperature range (SRT): normal;[4] CKE: LOW; External clock: off; CK_t and CK_c: LOW; CL: see the table above; BL: 8;[1] AL: 0; CS_n, command, address, bank group address, bank address, data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: SELF REFRESH operation; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: midlevel

Table 25: Basic I_{DD}, I_{PP} and I_{DDQ} Measurement Conditions (Continued)

Symbol	Description
I_{DD6E}	**Self Refresh Current: Extended Temperature Range [4]** T_C: 0–95°C; Auto self refresh (ASR): disabled;[4] Self refresh temperature range (SRT): extended;[4] CKE: LOW; External clock: off; CK_t and CK_c: LOW; CL: see the previous table; BL: 8;[1] AL: 0; CS_n, command, address, group bank address, bank address, data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: EXTENDED TEMPERATURE SELF REFRESH operation; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: midlevel
I_{PP6x}	**Self Refresh I_{PP} Current** Same conditions as I_{DD6E} above
I_{DD6R}	**Self Refresh Current: Reduced Temperature Range** T_C: 0–45°C; Auto self refresh (ASR): disabled; Self refresh temperature range (SRT): reduced;[4] CKE: LOW; External clock: off; CK_t and CK_c: LOW; CL: see the previous table; BL: 8;[1] AL: 0; CS_n, command, address, bank group address, bank address, data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: EXTENDED TEMPERATURE SELF REFRESH operation; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: midlevel
I_{DD7}	**Operating Bank Interleave Read Current** CKE: HIGH; External clock: on; ^{t}CK, *n*RC, *n*RAS, *n*RCD, *n*RRD, *n*FAW, CL: see the previous table; BL: 8;[15] AL: CL - 1; CS_n: HIGH between ACT and RDA; Command, address, group bank address, bank address inputs: partially toggling according to the I_{DD7} Measurement-Loop Pattern table; Data I/O: read data bursts with different data between one burst and the next one according to the I_{DD7} Measurement-Loop Pattern table; DM: stable at 0; Bank activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see the I_{DD7} Measurement-Loop Pattern table; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0; Pattern details: see the I_{DD7} Measurement-Loop Pattern table
I_{PP7}	**Operating Bank Interleave Read I_{PP} Current** Same conditions as I_{DD7} above
I_{DD8}	**Maximum Power Down Current** Place DRAM in MPSM then CKE: HIGH; External clock: on; ^{t}CK, CL: see the previous table; BL: 8;[1] AL: 0; CS_n: stable at 1; Command, address, bank group address, bank address inputs: stable at 0; Data I/O: V_{DDQ}; DM_n: stable at 1; Bank activity: all banks closed; Output buffer and R_{TT}: enabled in mode registers;[2] ODT signal: stable at 0

Notes:
1. Burst length: BL8 fixed by MRS: set MR0 [1:0] 00.
2. Output buffer enable: set MR1 [12] 0 (output buffer enabled); set MR1 [2:1] 00 (R_{ON} = RZQ/7); $R_{TT(NOM)}$ enable: set MR1 [10:8] = 011 (RZQ/6); $R_{TT(WR)}$ enable: set MR2 [11:9] 001 (RZQ/2) and $R_{TT(Park)}$ enable: set MR5 [8:6] 000 (disabled).
3. Auto self refresh (ASR): set MR2 [6] 0 to disable or MR2 [6] 1 to enable feature.
4. Self refresh temperature range (SRT): set MR2 [7] 0 for normal or MR2 [7] 1 for extended temperature range.
5. READ burst type: Nibble sequential, set MR0 [3] 0.

Current Specifications – Patterns and Test Conditions

Current Test Definitions and Patterns

Table 26: I_{DD0} and I_{PP0} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Logical Rank Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	0	ACT	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	–
				1, 2	D, D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	–
				3, 4	D_n, D_n	1	1	1	1	1	0	000	3	3	0	0	0	7	F	0	–
				...	Repeat pattern 1...4 until *n*RAS - 1; truncate if necessary																
				*n*RAS	PRE	0	1	0	1	0	0	000	0	0	0	0	0	0	0	0	–
				...	Repeat pattern 1...4 until *n*RC - 1; truncate if necessary																
			1	1 × *n*RC	Repeat Logical Rank Loop 0, use C[2:0] = 001 instead[2]																
			2	2 × *n*RC	Repeat Logical Rank Loop 0, use C[2:0] = 010 instead[2]																
			3	3 × *n*RC	Repeat Logical Rank Loop 0, use C[2:0] = 011 instead[2]																
			4	4 × *n*RC	Repeat Logical Rank Loop 0, use C[2:0] = 100 instead[2]																
			5	5 × *n*RC	Repeat Logical Rank Loop 0, use C[2:0] = 101 instead[2]																
			6	6 × *n*RC	Repeat Logical Rank Loop 0, use C[2:0] = 110 instead[2]																
			7	7 × *n*RC	Repeat Logical Rank Loop 0, use C[2:0] = 111 instead[2]																
		1		8 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 1 instead																
		2		16 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead																
		3		24 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 3 instead																
		4		32 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead																
		5		40 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 2 instead																
		6		48 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead																
		7		56 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 0 instead																
		8		64 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead																
		9		72 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 1 instead																
		10		80 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead																
		11		88 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 3 instead																
		12		96 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead																
		13		104 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 2 instead																
		14		112 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead																
		15		120 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 0 instead																

Notes: 1. DQS_t, DQS_c are V_{DDQ}.

2. C2 is a "Don't Care" for 2-high and 4-high devices; C1 is a "Don't Care" for 2-high devices.
3. DQ signals are V_{DDQ}.

Table 27: I_{DD1} Measurement-Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Logical Rank Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	0	ACT	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	–
				1, 2	D, D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	–
				3, 4	D_n, D_n	1	1	1	1	1	0	000	3	3	0	0	0	7	F	0	–
				...	Repeat pattern 1...4 until *n*RCD - AL - 1; truncate if necessary																
				*n*RCD - AL	RD	0	1	1	0	1	0	000	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF, D2 = FF, D3 = 00, D4 = FF, D5 = 00, D5 = 00, D7 = FF
				...	Repeat pattern 1...4 until *n*RAS - 1; truncate if necessary																
				*n*RAS	PRE	0	1	0	1	0	0	000	0	0	0	0	0	0	0	0	
				...	Repeat pattern 1...4 until *n*RC - 1; truncate if necessary																
			1	1 × *n*RC	Repeat logical rank loop 0, use C[2:0] = 001 instead [2]																
			2	2 × *n*RC	Repeat logical rank loop 0, use C[2:0] = 010 instead [2]																
			3	3 × *n*RC	Repeat logical rank loop 0, use C[2:0] = 011 instead [2]																
			4	4 × *n*RC	Repeat logical rank loop 0, use C[2:0] = 100 instead [2]																
			5	5 × *n*RC	Repeat logical rank loop 0, use C[2:0] = 101 instead [2]																
			6	6 × *n*RC	Repeat logical rank loop 0, use C[2:0] = 110 instead [2]																
			7	7 × *n*RC	Repeat logical rank loop 0, use C[2:0] = 111 instead [2]																
		1	0	8 × *n*RC + 0	ACT	0	0	0	1	1	0		1	1	0	0	0	0	0	0	–
				8 × *n*RC + 1, 2	D, D	1	0	0	0	0	0		0	0	0	0	0	0	0	0	–
				8 × *n*RC + 3, 4	D_n, D_n	1	1	1	1	1	0		3	3	0	0	0	7	F	0	–
				...	Repeat pattern *n*RC + 1...4 until 1 × *n*RC + *n*RAS - 1; truncate if necessary																
				8 × *n*RC +*n*RCD - AL	RD	0	1	1	0	1	0		1	1	0	0	0	0	0	0	D0 = FF, D1 = 00, D2 = 00, D3 = FF, D4 = 00, D5 = FF, D5 = FF, D7 = 00
				...	Repeat pattern 1...4 until *n*RAS - 1; truncate if necessary																
				8 × *n*RC + *n*RAS	PRE	0	1	0	1	0	0		1	1	0	0	0	0	0	0	
				...	Repeat pattern *n*RC + 1...4 until 2 × *n*RC - 1; truncate if necessary																

Table 27: I_{DD1} Measurement-Loop Pattern[1] (Continued)

CK_c, CK_t,	CKE	Sub-Loop	Logical Rank Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	1	1	9 × *n*RC	Repeat logical rank loop 0, use C[2:0] = 001 instead[2]																
			2	10 × *n*RC	Repeat logical rank loop 0, use C[2:0] = 010 instead [2]																
			3	11 × *n*RC	Repeat logical rank loop 0, use C[2:0] = 011 instead [2]																
			4	12 × *n*RC	Repeat logical rank loop 0, use C[2:0] = 100 instead [2]																
			5	13 × *n*RC	Repeat logical rank loop 0, use C[2:0] = 101 instead [2]																
			6	14 × *n*RC	Repeat logical rank loop 0, use C[2:0] = 110 instead [2]																
			7	15 × *n*RC	Repeat logical rank loop 0, use C[2:0] = 111 instead [2]																
		2		16 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead																
		3		24 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 3 instead																
		4		32 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead																
		5		40 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 2 instead																
		6		48 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead																
		7		56 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 0 instead																
		8		64 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead																
		9		72 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 1 instead																
		10		80 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead																
		11		88 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 3 instead																
		12		96 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead																
		13		104 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 2 instead																
		14		112 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead																
		15		120 × *n*RC	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 0 instead																

Notes:
1. DQS_t, DQS_c are V_{DDQ} when not toggling.
2. C2 is a "Don't Care" for 2-high and 4-high devices; C1 is a "Don't Care" for 2-high devices.
3. DQ signals are V_{DDQ} except when burst sequence drives each DQ signal by a READ command.

Table 28: I_{DD2N}, I_{DD3N} and I_{PP3P} Measurement-Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	–
			2	D_n	1	1	1	1	1	0	000	3	3	0	0	0	7	F	0	–
			3	D_n	1	1	1	1	1	0	000	3	3	0	0	0	7	F	0	–
		1	4–7	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 1 instead																
		2	8–11	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead																
		3	12–15	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 3 instead																
		4	16–19	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead																
		5	20–23	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 2 instead																
		6	24–27	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead																
		7	28–31	Repeat sub-loop 0, use BG[1:0] = 1, use BA[1:0] = 0 instead																
		8	32–35	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead																
		9	36–39	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 1 instead																
		10	40–43	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead																
		11	44–47	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 3 instead																
		12	48–51	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead																
		13	52–55	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 2 instead																
		14	56–59	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead																
		15	60–63	Repeat sub-loop 0, use BG[1:0] = 3, use BA[1:0] = 0 instead																

Notes:
1. DQS_t, DQS_c are V_{DDQ}.
2. C2 is a "Don't Care" for 2-high and 4-high devices; C1 is a "Don't Care" for 2-high devices.
3. DQ signals are V_{DDQ}.

Table 29: I_{DD2NT} Measurement-Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	–
			1	D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	–
			2	D_n	1	1	1	1	1	0	000	3	3	0	0	0	7	F	0	–
			3	D_n	1	1	1	1	1	0	000	3	3	0	0	0	7	F	0	–
		1	4–7	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 1, use BA[1:0] = 1 instead															
		2	8–11	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 0, use BA[1:0] = 2 instead															
		3	12–15	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 1, use BA[1:0] = 3 instead															
		4	16–19	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 0, use BA[1:0] = 1 instead															
		5	20–23	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 1, use BA[1:0] = 2 instead															
		6	24–27	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 0, use BA[1:0] = 3 instead															
		7	28–31	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 1, use BA[1:0] = 0 instead															
		8	32–35	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 2, use BA[1:0] = 0 instead															
		9	36–39	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 3, use BA[1:0] = 1 instead															
		10	40–43	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 2, use BA[1:0] = 2 instead															
		11	44–47	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 3, use BA[1:0] = 3 instead															
		12	48–51	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 2, use BA[1:0] = 1 instead															
		13	52–55	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 3, use BA[1:0] = 2 instead															
		14	56–59	Repeat sub-loop 0 with ODT = 0, use BG[1:0] = 2, use BA[1:0] = 3 instead															
		15	60–63	Repeat sub-loop 0 with ODT = 1, use BG[1:0] = 3, use BA[1:0] = 0 instead															

Notes:
1. DQS_t, DQS_c are V_{SSQ}.
2. C2 is a "Don't Care" for 2-high and 4-high devices; C1 is a "Don't Care" for 2-high devices.
3. DQ signals are V_{SSQ}.

Table 30: I_{DD4R} Measurement-Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Logical Rank Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	0	RD	0	1	1	0	1	0	000	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF, D2 = FF, D3 = 00, D4 = FF, D5 = 00, D5 = 00, D7 = FF
				1	D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	
				2, 3	D_n, D_n	1	1	1	1	1	0	000	3	3	0	0	0	7	F	0	
		1		4	RD	0	1	1	0	1	0	000	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D5 = FF, D7 = 00
				5	D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	
				6, 7	D_n, D_n	1	1	1	1	1	0	000	3	3	0	0	0	7	F	0	
		2		8–11	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead																
		3		12–15	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 3 instead																
		4		16–19	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead																
		5		20–23	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 2 instead																
		6		24–27	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead																
		7		28–31	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 0 instead																
		8		32–35	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead																
		9		36–39	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 1 instead																
		10		40–43	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead																
		11		44–47	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 3 instead																
		12		48–51	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead																
		13		52–55	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 2 instead																
		14		56–59	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead																
		15		60–63	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 0 instead																
Toggling	Static High		1	64–127	Repeat logical rank loop 0, use C[2:0] = 001 instead[2]																
			2	128–191	Repeat logical rank loop 0, use C[2:0] = 010 instead[2]																
			3	192–255	Repeat logical rank loop 0, use C[2:0] = 011 instead[2]																
			4	256–319	Repeat logical rank loop 0, use C[2:0] = 100 instead[2]																
			5	320–383	Repeat logical rank loop 0, use C[2:0] = 101 instead[2]																
			6	384–447	Repeat logical rank loop 0, use C[2:0] = 110 instead[2]																
			7	448–511	Repeat logical rank loop 0, use C[2:0] = 111 instead[2]																

Notes:
1. DQS_t, DQS_c are V_{DDQ} when not toggling.
2. C2 is a "Don't Care" for 2-high and 4-high devices; C1 is a "Don't Care" for 2-high devices.
3. Burst sequence driven on each DQ signal by a READ command. Outside burst operation, DQ signals are V_{DDQ}.

Table 31: I_{DD4W} Measurement-Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Logical Rank Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	0	WR	0	1	1	0	0	1	000	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF, D2 = FF, D3 = 00, D4 = FF, D5 = 00, D5 = 00, D7 = FF
				1	D	1	0	0	0	0	1	000	0	0	0	0	0	0	0	0	
				2, 3	D_n, D_n	1	1	1	1	0	1	000	3	3	0	0	0	7	F	0	
		1		4	WR	0	1	1	0	0	1	000	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00 D2 = 00, D3 = FF D4 = 00, D5 = FF D5 = FF, D7 = 00
				5	D	1	0	0	0	0	1	000	0	0	0	0	0	0	0	0	
				6, 7	D_n, D_n	1	1	1	1	0	1	000	3	3	0	0	0	7	F	0	
		2		8–11	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead																
		3		12–15	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 3 instead																
		4		16–19	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead																
		5		20–23	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 2 instead																
		6		24–27	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead																
		7		28–31	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 0 instead																
		8		32–35	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead																
		9		36–39	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 1 instead																
		10		40–43	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead																
		11		44–47	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 3 instead																
		12		48–51	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead																
		13		52–55	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 2 instead																
		14		56–59	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead																
		15		60–63	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 0 instead																
Toggling	Static High		1	64–127	Repeat logical rank loop 0, use C[2:0] = 001 instead																
			2	128–191	Repeat logical rank loop 0, use C[2:0] = 010 instead																
			3	192–255	Repeat logical rank loop 0, use C[2:0] = 011 instead																
			4	256–319	Repeat logical rank loop 0, use C[2:0] = 100 instead																
			5	320–383	Repeat logical rank loop 0, use C[2:0] = 101 instead																
			6	384–447	Repeat logical rank loop 0, use C[2:0] = 110 instead																
			7	448–511	Repeat logical rank loop 0, use C[2:0] = 111 instead																

Notes:
1. DQS_t, DQS_c are V_{DDQ} when not toggling.
2. C2 is a "Don't Care" for 2-high and 4-high devices. C1 is a "Don't Care" for 2-high devices.
3. Burst sequence driven on each DQ signal by WRITE command. Outside burst operation, DQ signals are V_{DDQ}.

Table 32: I_{DD4Wc} Measurement-Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
Toggling	Static High	0	0	WR	0	1	1	0	0	0	000	0	0	0	0	0	0	0	0	D0 = 00, D1 = FF, D2 = FF, D3 = 00, D4 = FF, D5 = 00, D8 = CRC
			1, 2	D, D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	
			3, 4	D_n, D_n	1	1	1	1	0	0	000	3	3	0	0	0	7	F	0	
		1	5	WR	0	1	1	0	0	0	000	1	1	0	0	0	7	F	0	D0 = FF, D1 = 00, D2 = 00, D3 = FF, D4 = 00, D5 = FF, D5 = FF, D7 = 00 D8 = CRC
			6, 7	D, D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	
			8, 9	D_n, D_n	1	1	1	1	0	0	000	3	3	0	0	0	7	F	0	
		2	10–14	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead																
		3	15–19	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 3 instead																
		4	20–24	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead																
		5	25–29	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 2 instead																
		6	30–34	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead																
		7	35–39	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 0 instead																
		8	40–44	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead																
		9	45–49	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 1 instead																
		10	50–54	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead																
		11	55–59	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 3 instead																
		12	60–64	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead																
		13	65–69	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 2 instead																
		14	70–74	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead																
		15	75–79	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 0 instead																

Notes:
1. Pattern provided for reference only.
2. DQS_t, DQS_c are V_{DDQ} when not toggling.
3. C2 is a "Don't Care" for 2-high and 4-high devices; C1 is a "Don't Care" for 2-high devices.
4. Burst sequence driven on each DQ signal by WRITE command. Outside burst operation, DQ signals are V_{DDQ}.

Table 33: I_{DD5B1} Measurement-Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Logical Rank Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	0	REF	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	–
		1		1	D	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	–
				2	D	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	–
				3	D_n	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	–
				4	D_n	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	–
				5–8	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 1 instead																
				9–12	Repeat pattern 1...4, use BG[1:0] = 0, use BA[1:0] = 2 instead																
				13–16	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 3 instead																
				17–20	Repeat pattern 1...4, use BG[1:0] = 0, use BA[1:0] = 1 instead																
				21–24	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 2 instead																
				25–28	Repeat pattern 1...4, use BG[1:0] = 0, use BA[1:0] = 3 instead																
				29–32	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 0 instead																
				33–36	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 0 instead																
				37–40	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 1 instead																
				41–44	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 2 instead																
				45–48	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 3 instead																
				49–52	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 1 instead																
				53–56	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 2 instead																
				57–60	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 3 instead																
				61–64	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 0 instead																
		2		65...nRFC$_{(DLR)}$ - 1[4]	Repeat sub-loop 1; truncate if necessary																
			1	nRFC$_{(DLR)}$ ... 2 × nRFC$_{(DLR)}$ - 1[4]	Repeat logical rank loop 0, use C[2:0] = 001 instead[2]																
			2	2 × nRFC$_{(DLR)}$ ... 3 × nRFC$_{(DLR)}$ - 1[4]	Repeat logical rank loop 0, use C[2:0] = 010 instead[2]																
			3	3 × nRFC$_{(DLR)}$ ... 4 × nRFC$_{(DLR)}$ - 1[4]	Repeat logical rank loop 0, use C[2:0] = 011 instead[2]																

Table 33: I_{DD5B1} Measurement-Loop Pattern[1] (Continued)

CK_c, CK_t,	CKE	Sub-Loop	Logical Rank Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High		4	4 × $nRFC_{(DLR)}$ ... 5 × $nRFC_{(DLR)}$ - 1 [4]	Repeat logical rank loop 0, use C[2:0] = 100 instead[2]																
			5	5 × $nRFC_{(DLR)}$ ... 6 × $nRFC_{(DLR)}$ - 1 [4]	Repeat logical rank loop 0, use C[2:0] = 101 instead[2]																
			6	6 × $nRFC_{(DLR)}$ ... 7 × $nRFC_{(DLR)}$ - 1 [4]	Repeat logical rank loop 0, use C[2:0] = 110 instead[2]																
			7	7 × $nRFC_{(DLR)}$ ... 8 × $nRFC_{(DLR)}$ - 1 [4]	Repeat logical rank loop 0, use C[2:0] = 111 instead[2]																

Notes:
1. DQS_t, DQS_c are V_{DDQ}.
2. C2 is a "Don't Care" for 2-high and 4-high devices; C1 is a "Don't Care" for 2-high devices.
3. DQ signals are V_{DDQ}.
4. $nRFC_{(SLR)}$ must be met for 2-high devices.

Table 34: I_{DD5B2} Measurement-Loop Pattern[1]

CK_c, CK_t,	CKE	Sub-Loop	Logical Rank Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	0	REF	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	–
		1		1	D	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	–
				2	D	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	–
				3	D_n	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	–
				4	D_n	1	1	1	1	1	0	0	3	3	0	0	0	7	F	0	–
				5–8	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 1 instead																
				9–12	Repeat pattern 1...4, use BG[1:0] = 0, use BA[1:0] = 2 instead																
				13–16	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 3 instead																
				17–20	Repeat pattern 1...4, use BG[1:0] = 0, use BA[1:0] = 1 instead																
				21–24	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 2 instead																
				25–28	Repeat pattern 1...4, use BG[1:0] = 0, use BA[1:0] = 3 instead																
				29–32	Repeat pattern 1...4, use BG[1:0] = 1, use BA[1:0] = 0 instead																
				33–36	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 0 instead on page																
				37–40	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 1 instead on page																
				41–44	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 2 instead on page																
				45–48	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 3 instead on page																
				49–52	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 1 instead on page																
				53–56	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 2 instead on page																
				57–60	Repeat pattern 1...4, use BG[1:0] = 2, use BA[1:0] = 3 instead on page																
				61–64	Repeat pattern 1...4, use BG[1:0] = 3, use BA[1:0] = 0 instead on page																
		2		65...nRFC$_{(SLR)}$ - 1	Repeat sub-loop 1; truncate if necessary																
			1	nRFC$_{(SLR)}$ ... 2 × nRF$_{(SLR)}$ - 1	Repeat logical rank loop 0, use C[2:0] = 001 instead[2]																
			2	2 × nRFC$_{(SLR)}$ ... 3 × nRF$_{(SLR)}$ - 1	Repeat logical rank loop 0, use C[2:0] = 010 instead[2]																
			3	3 × nRFC$_{(SLR)}$ ... 4 × nRF$_{(SLR)}$ - 1	Repeat logical rank loop 0, use C[2:0] = 011 instead[2]																

Table 34: I_{DD5B2} Measurement-Loop Pattern[1] (Continued)

CK_c, CK_t,	CKE	Sub-Loop	Logical Rank Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High		4	4 × $nRFC_{(SLR)}$ … 5 × $nRF_{(SLR)}$ - 1	Repeat logical rank loop 0, use C[2:0] = 100 instead[2]																
			5	5 × $nRFC_{(SLR)}$ … 6 × $nRF_{(SLR)}$ - 1	Repeat logical rank loop 0, use C[2:0] = 101 instead[2]																
			6	6 × $nRFC_{(SLR)}$ … 7 × $nRF_{(SLR)}$ - 1	Repeat logical rank loop 0, use C[2:0] = 110 instead[2]																
			7	7 × $nRFC_{(SLR)}$ … 8 × $nRFC_{(SLR)}$ - 1	Repeat logical rank loop 0, use C[2:0] = 111 instead[2]																

Notes:
1. DQS_t, DQS_c are V_{DDQ}.
2. C2 is a "Don't Care" for 2-high and 4-high devices; C1 is a "Don't Care" for 2-high devices.
3. DQ signals are V_{DDQ}.

Table 35: I_{DD7} Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][2]	BG[1:0]	BA[1:0]	A12/BC_n	A[17, 13, 11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[3]
Toggling	Static High	0	0	ACT	0	0	0	0	0	0	000	0	0	0	0	0	0	0	0	–
			1	RDA	0	1	1	0	1	0	000	0	0	0	0	1	0	0	0	
			2	D	1	0	0	0	0	0	000	0	0	0	0	0	0	0	0	–
			3	D_n	1	1	1	1	1	0	000	3	3	0	0	0	7	F	0	–
			...	Repeat pattern 2...3 until *n*RRD - 1, if *n*RCD > 4. Truncate if necessary																
		1	*n*RRD	ACT	0	0	0	0	0	0	000	1	1	0	0	0	0	0	0	–
			*n*RRD+1	RDA	0	1	1	0	1	0	000	1	1	0	0	1	0	0	0	
			...	Repeat pattern 2...3 until 2 × *n*RRD - 1, if *n*RCD > 4. Truncate if necessary																
		2	2 × *n*RRD	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 2 instead																
		3	3 × *n*RRD	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 3 instead																
		4	4 × *n*RRD	Repeat pattern 2...3 until *n*FAW - 1, if *n*FAW > 4 × *n*RCD. Truncate if necessary																
		5	*n*FAW	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 1 instead																
		6	*n*FAW + *n*RRD	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 2 instead																
		7	*n*FAW + 2 × *n*RRD	Repeat sub-loop 0, use BG[1:0] = 0, use BA[1:0] = 3 instead																
		8	*n*FAW + 3 × *n*RRD	Repeat sub-loop 1, use BG[1:0] = 1, use BA[1:0] = 0 instead																
		9	*n*FAW + 4 × *n*RRD	Repeat sub-loop 4																
		10	2 × *n*FAW	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 0 instead																
		11	2 × *n*FAW + *n*RRD	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 1 instead																
		12	2 × *n*FAW + 2 × *n*RRD	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 2 instead																
		13	2 × *n*FAW + 3 × *n*RRD	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 3 instead																
		14	2 × *n*FAW + 4 × *n*RRD	Repeat sub-loop 4																
		15	3 × *n*FAW	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 1 instead																
		16	3 × *n*FAW + *n*RRD	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 2 instead																
		17	3 × *n*FAW + 2 × *n*RRD	Repeat sub-loop 0, use BG[1:0] = 2, use BA[1:0] = 3 instead																
		18	3 × *n*FAW + 3 × *n*RRD	Repeat sub-loop 1, use BG[1:0] = 3, use BA[1:0] = 0 instead																
		19	3 × *n*FAW + 4 × *n*RRD	Repeat sub-loop 4																
		20	4 × *n*FAW	Repeat pattern 2...3 until *n*RC - 1, if *n*RC > 4 × *n*FAW. Truncate if necessary																

Notes:
1. DQS_t, DQS_c are V_{DDQ}.
2. C2 is a "Don't Care" for 2-high and 4-high devices; C1 is a "Don't Care" for 2-high devices.

3. DQ signals are V_{DDQ} except when burst sequence drives each DQ signal by a READ command.

I_{DD} Specifications

Table 36: Timings used for I_{DD}, I_{PP}, and I_{DDQ} Measurement – Loop Patterns

Symbol		DDR4-1600			DDR4-1866			DDR4-2133			DDR4-2400			DDR4-2666			DDR4-2933			DDR4-3200			Unit
		12-11-10	13-12-11	14-13-12	14-13-12	15-14-13	16-15-14	17-15-15	18-15-15	20-16-16	19-17-17	20-17-17	22-18-18	20-17-17	22-19-19	24-20-20	23-20-20	24-21-21	25-22-22	24-20-20	26-22-22	28-24-24	
^{t}CK		1.25			1.071			0.937			0.833			0.750			0.682			0.625			ns
CL		12	13	14	14	15	16	17	18	20	19	20	22	20	22	24	23	24	25	24	26	28	CK
CWL		11			12			14			16			18			20			20			CK
*n*RCD		11	12	13	13	14	15	15	15	16	17	17	18	17	19	20	20	21	22	20	22	24	CK
*n*RC		38	39	40	44	45	46	51	51	52	56	56	57	60	62	63	67	68	69	72	74	76	CK
*n*RP		10	11	12	12	13	14	15	15	16	17	17	18	17	19	20	20	21	22	20	22	24	CK
*n*RAS		28			32			36			39			43			47			52			CK
*n*FAW$_{(SLR)}$	x4 on page	16			16			16			16			16			16			16			CK
	x8	20			22			23			26			28			31			34			CK
*n*RRD_S$_{(SLR)}$	x4	4			4			4			4			4			4			4			CK
	x8	4			4			4			4			4			4			4			CK
*n*RRD_L$_{(SLR)}$	x4	5			5			6			6			7			8			8			CK
	x8	5			5			6			6			7			8			8			CK
*n*RFC$_{(SLR)}$ 4Gb		208			243			278			313			347			382			416			CK
*n*RFC$_{(SLR)}$ 8Gb		280			327			374			421			467			514			560			CK
*n*RFC$_{(SLR)}$ 16Gb		440			514			587			661			734			807			880			CK
*n*RFC$_{(DLR)}$ 4Gb		72			85			97			109			120			132			144			CK
*n*RFC$_{(DLR)}$ 8Gb		96			113			129			145			160			176			192			CK
*n*RFC$_{(DLR)}$ 16Gb		152			178			203			229			254			279			304			CK

Note: 1. 1KB based x4 use same numbers of clocks for *n*FAW as the x8.

Current Specifications – Limits

Table 37: 2-High I_{DD}, I_{PP} and I_{DDQ} Current Limits; Die Rev. G (0° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	Unit
I_{DD0}: One bank ACTIVATE-to-PRECHARGE current	x4	51	52	53	mA
	x8	63	64	65	mA
I_{PP0}: One bank ACTIVATE-to-PRECHARGE I_{PP} current	ALL	5	5	5	mA
I_{DD1}: One bank ACTIVATE-to-READ-to- PRECHARGE current	x4	67	68	69	mA
	x8	83	84	85	mA
I_{DD2N}: Precharge standby current	ALL	49	51	53	mA
I_{DD2NT}: Precharge standby ODT current	ALL	71	73	75	mA
I_{DD2P}: Precharge power-down current	ALL	49	51	53	mA
I_{DD2Q}: Precharge quiet standby current	ALL	46	48	50	mA
I_{DD3N}: Active standby current	x4	47	48	49	mA
	x8	58	59	60	mA
I_{PP3N}: Active standby I_{PP} current	ALL	6	6	6	mA
I_{DD3P}: Active power-down current	ALL	52	55	58	mA
I_{DD4R}: Burst read current	x4	150	160	170	mA
	x8	205	215	225	mA
I_{DD4W}: Burst write current	x4	155	165	175	mA
	x8	210	215	250	mA
I_{DD5B1}: Different logic rank burst refresh current (1X REF)	ALL	403	403	403	mA
I_{PP5B1}: Different logic rank burst refresh I_{PP} current (1X REF)	ALL	32	32	32	mA
I_{DD5B2}: Same logic rank burst refresh current (1X REF)	ALL	250	250	250	mA
I_{PP5B2}: Same logic rank burst refresh I_{PP} current (1X REF)	ALL	22	22	22	mA
I_{DD6N}: Self refresh current; 0–85°C[1]	ALL	30	30	30	mA
I_{PP6x}: Self refresh I_{PP} current; 0–95°C [26]	ALL	10	10	10	mA
I_{DD6E}: Self refresh current; 0–95°C[2]	ALL	45	45	45	mA
I_{DD6R}: Self refresh current; 0–45°C[3,4]	ALL	21	21	21	mA
I_{DD6A}: Auto self refresh current (25°C)[4]	ALL	9	9	9	mA
I_{DD6A}: Auto self refresh current (45°C)[4]	ALL	12	12	12	mA
I_{DD6A}: Auto self refresh current (75°C)[4]	ALL	30	30	30	mA
I_{DD7}: Bank interleave read current	x4	210	230	250	mA
	x8	220	225	230	mA
I_{PP7}: Bank interleave read I_{PP} current	ALL	13	13	13	mA
I_{DD8}: Maximum power-down current	ALL	35	35	35	mA

Notes: 1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).

2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0–95°C).
3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0–45°C).
4. I_{DD6A}, I_{DD6R}, and I_{DD6E} are verified by design and characterization, and may not be subject to production test.
5. When additive latency is enabled for I_{DD0}, current changes by approximately 0%.
6. When additive latency is enabled for I_{DD1}, current changes by approximately +5%.
7. When additive latency is enabled for I_{DD2N}, current changes by approximately +0.6%.
8. When DLL is disabled for I_{DD2N}, current changes by approximately 0%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately –44%.
10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +14%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately +0.6%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +5%.
14. When additive latency is enabled for I_{DD4W}, current changes by approximately +1.6%.
15. When write CRC is enabled for I_{DD4W}, current changes by approximately –8%(2133/2400), –5%(1600/1866).
16. When CA parity is enabled for I_{DD4W}, current changes by approximately +14% (x8).
17. When 2X REF is enabled for I_{DD5B1}, current changes by approximately -14%.
18. When 4X REF is enabled for I_{DD5B1}, current changes by approximately -33%.
19. When 2X REF is enabled for I_{PP5B1}, current changes by approximately -14%.
20. When 4X REF is enabled for I_{PP5B1}, current changes by approximately -33%.
21. When 2X REF is enabled for I_{DD5B2}, current changes by approximately –14%.
22. When 4X REF is enabled for I_{DD5B2}, current changes by approximately –33%.
23. When 2X REF is enabled for I_{PP5B2}, current changes by approximately -14%.
24. When 4X REF is enabled for I_{PP5B2}, current changes by approximately -33%.
25. I_{PP0} test and limit is applicable for I_{DD6N} and I_{DD1} conditions.
26. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x}, I_{DD6} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
27. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133
28. The I_{DD} values must be derated (increased) when operated between 85°C ≤ T_C ≤ 95°C:

    I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, I_{DD5B1} and I_{DD5B2} must be derated by +3%; I_{DD2P} must be derated by +40%; All I_{PP} currents except I_{PP6x} must be derated by +3%. These values are verified by design and characterization, and may not be subject to production test.

Table 38: 4-High I_{DD}, I_{PP} and I_{DDQ} Current Limits; Die Rev. G (0° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	Unit
I_{DD0}: One bank ACTIVATE-to-PRECHARGE current	x4	78	79	80	mA
	x8	93	94	95	mA
I_{PP0}: One bank ACTIVATE-to-PRECHARGE I_{PP} current	ALL	8	8	8	mA
I_{DD1}: One bank ACTIVATE-to-READ-to- PRECHARGE current	x4	92	93	94	mA
	x8	110	112	115	mA
I_{DD2N}: Precharge standby current	ALL	74	74	74	mA
I_{DD2NT}: Precharge standby ODT current	ALL	100	103	105	mA
I_{DD2P}: Precharge power-down current	ALL	66	69	69	mA

Table 38: 4-High I_{DD}, I_{PP} and I_{DDQ} Current Limits; Die Rev. G (0° ≤ T_C ≤ 85°C) (Continued)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	Unit
I_{DD2Q}: Precharge quiet standby current	ALL	69	69	69	mA
I_{DD3N}: Active standby current	x4	68	70	72	mA
	x8	83	84	85	mA
I_{PP3N}: Active standby I_{PP} current	ALL	11	11	11	mA
I_{DD3P}: Active power-down current	ALL	80	83	85	mA
I_{DD4R}: Burst read current	x4	205	220	230	mA
	x8	260	280	310	mA
I_{DD4W}: Burst write current	x4	210	225	240	mA
	x8	290	310	330	mA
I_{DD5B1}: Different logic rank burst refresh current (1X REF)	ALL	600	600	600	mA
I_{PP5B1}: Different logic rank burst refresh I_{PP} current (1X REF)	ALL	46	46	46	mA
I_{DD5B2}: Same logic rank burst refresh current (1X REF)	ALL	270	270	270	mA
I_{PP5B2}: Same logic rank burst refresh I_{PP} current (1X REF)	ALL	23	23	23	mA
I_{DD6N}: Self refresh current; 0–85°C[1]	ALL	58	58	58	mA
I_{PP6x}: Self refresh I_{PP} current; 0–95°C [26]	ALL	20	20	20	mA
I_{DD6E}: Self refresh current; 0–95°C[2]	ALL	88	88	88	mA
I_{DD6R}: Self refresh current; 0–45°C[3,4]	ALL	42	42	42	mA
I_{DD6A}: Auto self refresh current (25°C)[4]	ALL	18	18	18	mA
I_{DD6A}: Auto self refresh current (45°C)[4]	ALL	24	24	24	mA
I_{DD6A}: Auto self refresh current (75°C)[4]	ALL	60	60	60	mA
I_{DD7}: Bank interleave read current	x4	250	270	290	mA
	x8	255	260	270	mA
I_{PP7}: Bank interleave read I_{PP} current	ALL	14	14	14	mA
I_{DD8}: Maximum power-down current	ALL	60	60	60	mA

Notes:
1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0–95°C).
3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0–45°C).
4. I_{DD6A}, I_{DD6R}, and I_{DD6E} are verified by design and characterization, and may not be subject to production test.
5. When additive latency is enabled for I_{DD0}, current changes by approximately 0%.
6. When additive latency is enabled for I_{DD1}, current changes by approximately +5%.
7. When additive latency is enabled for I_{DD2N}, current changes by approximately +0.6%.
8. When DLL is disabled for I_{DD2N}, current changes by approximately 0%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately –44%.

10. When gear-down is enabled for I_{DD2N}, current changes by approximately 0%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +14%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately +0.6%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +5%.
14. When additive latency is enabled for I_{DD4W}, current changes by approximately +1.6%.
15. When write CRC is enabled for I_{DD4W}, current changes by approximately –8%(2133/2400), –5%(1600/1866).
16. When CA parity is enabled for I_{DD4W}, current changes by approximately +14% (x8).
17. When 2X REF is enabled for I_{DD5B1}, current changes by approximately -14%.
18. When 4X REF is enabled for I_{DD5B1}, current changes by approximately -33%.
19. When 2X REF is enabled for I_{PP5B1}, current changes by approximately -14%.
20. When 4X REF is enabled for I_{PP5B1}, current changes by approximately -33%.
21. When 2X REF is enabled for I_{DD5B2}, current changes by approximately –14%.
22. When 4X REF is enabled for I_{DD5B2}, current changes by approximately –33%.
23. When 2X REF is enabled for I_{PP5B2}, current changes by approximately -14%.
24. When 4X REF is enabled for I_{PP5B2}, current changes by approximately -33%.
25. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
26. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x}, I_{DD6} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
27. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133
28. The I_{DD} values must be derated (increased) when operated between 85°C ≤ T_C ≤ 95°C:

    I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, I_{DD5B1} and I_{DD5B2} must be derated by +3%; I_{DD2P} must be derated by +40%; All I_{PP} currents except I_{PP6x} must be derated by +3%. These values are verified by design and characterization, and may not be subject to production test.

Table 39: 2-High I_{DD}, I_{PP} and I_{DDQ} Current Limits; Die Rev. E (0° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD0}: One bank ACTIVATE-to-PRE-CHARGE current	x4	44	46	48	50	52	mA
I_{PP0}: One bank ACTIVATE-to-PRE-CHARGE I_{PP} current	x4	5	5	5	5	5	mA
I_{DD1}: One bank ACTIVATE-to-READ-to-PRECHARGE current	x4	62	65	66	68	70	mA
I_{DD2N}: Precharge standby current	x4	36	37	38	39	40	mA
I_{DD2NT}: Precharge standby ODT current	x4	43	45	47	49	51	mA
I_{DD2P}: Precharge power-down current	x4	28	28	28	28	28	mA
I_{DD2Q}: Precharge quiet standby current	x4	33	33	33	33	33	mA
I_{DD3N}: Active standby current	x4	41	43	45	47	49	mA
I_{PP3N}: Active standby I_{PP} current	x4	5	5	5	5	5	mA
I_{DD3P}: Active power-down current	x4	35	36	37	38	39	mA
I_{DD4R}: Burst read current	x4	150	160	170	180	190	mA
I_{DD4W}: Burst write current	x4	160	174	188	202	216	mA
I_{DD5B1}: Different logic rank burst refresh current (1X REF)	x4	700	700	700	700	700	mA

Table 39: 2-High I_{DD}, I_{PP} and I_{DDQ} Current Limits; Die Rev. E (0° ≤ T_C ≤ 85°C) (Continued)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{PP5B1}: Different logic rank burst refresh I_{PP} current (1X REF)	x4	49	49	49	49	49	mA
I_{DD5B2}: Same logic rank burst refresh current (1X REF)	x4	375	375	375	375	375	mA
I_{PP5B2}: Same logic rank burst refresh I_{PP} current (1X REF)	x4	26	26	26	26	26	mA
I_{DD6N}: Self refresh current; 0–85°C	x4	55	55	55	55	55	mA
I_{PP6x}: Self refresh I_{PP} current; 0–95°C [26]	x4	10	10	10	10	10	mA
I_{DD6E}: Self refresh current; 0–95°C[2]	x4	95	95	95	95	95	mA
I_{DD6R}: Self refresh current; 0–45°C[3,4]	x4	28	28	28	28	28	mA
I_{DD6A}: Auto self refresh current (25°C)[4]	x4	18	18	18	18	18	mA
I_{DD6A}: Auto self refresh current (45°C)[4]	x4	28	28	28	28	28	mA
I_{DD6A}: Auto self refresh current (75°C)[4]	x4	51	51	51	51	51	mA
I_{DD6A}: Auto self refresh current (95°C)[4]	x4	95	95	95	95	95	mA
I_{DD7}: Bank interleave read current	x4	205	225	245	265	285	mA
I_{PP7}: Bank interleave read I_{PP} current	x4	13	13	13	13	13	mA
I_{DD8}: Maximum power-down current	x4	24	24	24	24	24	mA

Notes:
1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0–95°C).
3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0–45°C).
4. I_{DD6A}, I_{DD6R}, and I_{DD6E} are verified by design and characterization, and may not be subject to production test.
5. When additive latency is enabled for I_{DD0}, current changes by approximately +1%.
6. When additive latency is enabled for I_{DD1}, current changes by approximately +15%.
7. When additive latency is enabled for I_{DD2N}, current changes by approximately +0.5%.
8. When DLL is disabled for I_{DD2N}, current changes by approximately -4%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately –28%.
10. When gear-down is enabled for I_{DD2N}, current changes by approximately -4%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +10%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately +1%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +5%.
14. When additive latency is enabled for I_{DD4W}, current changes by approximately +5%.
15. When write CRC is enabled for I_{DD4W}, current changes by approximately -10%.
16. When CA parity is enabled for I_{DD4W}, current changes by approximately +8%.
17. When 2X REF is enabled for I_{DD5B1}, current changes by approximately –25%.
18. When 4X REF is enabled for I_{DD5B1}, current changes by approximately –26%.
19. When 2X REF is enabled for I_{PP5B1}, current changes by approximately –25%.
20. When 4X REF is enabled for I_{PP5B1}, current changes by approximately –26%.
21. When 2X REF is enabled for I_{DD5B2}, current changes by approximately –25%.

22. When 4X REF is enabled for I_{DD5B2}, current changes by approximately –36%.
23. When 2X REF is enabled for I_{PP5B2}, current changes by approximately –25%.
24. When 4X REF is enabled for I_{PP5B2}, current changes by approximately –36%.
25. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
26. I_{PP6x} is applicable to I_{DD6N},I_{DD6E},I_{DD6R} and I_{DD6A} conditions.
27. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x}, I_{DD6} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
28. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x}, I_{DD6} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
29. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133
30. The I_{DD} values must be derated (increased) when operated between 85°C ≤ T_C ≤ 95°C:

    I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, I_{DD5B1} and I_{DD5B2} must be derated by +3%; I_{DD2P} must be derated by +10%; All I_{PP} currents except I_{PP6x} must be derated by +3%. These values are verified by design and characterization, and may not be subject to production test.

Table 40: 4-High I_{DD}, I_{PP} and I_{DDQ} Current Limits; Die Rev. E (0° ≤ T_C ≤ 85°C)

Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD0}: One bank ACTIVATE-to-PRE-CHARGE current	x4	73	75	77	79	81	mA
I_{PP0}: One bank ACTIVATE-to-PRE-CHARGE I_{PP} current	x4	8	8	8	8	8	mA
I_{DD1}: One bank ACTIVATE-to-READ-to-PRECHARGE current	x4	86	88	90	92	94	mA
I_{DD2N}: Precharge standby current	x4	65	66	67	68	69	mA
I_{DD2NT}: Precharge standby ODT current	x4	72	74	76	78	80	mA
I_{DD2P}: Precharge power-down current	x4	58	58	58	58	58	mA
I_{DD2Q}: Precharge quiet standby current	x4	62	62	62	62	62	mA
I_{DD3N}: Active standby current	x4	65	67	69	71	73	mA
I_{PP3N}: Active standby I_{PP} current	x4	8	8	8	8	8	mA
I_{DD3P}: Active power-down current	x4	64	65	66	67	68	mA
I_{DD4R}: Burst read current	x4	205	220	230	240	250	mA
I_{DD4W}: Burst write current	x4	210	225	240	255	270	mA
I_{DD5B1}: Different logic rank burst refresh current (1X REF)	x4	1025	1025	1025	1025	1025	mA
I_{PP5B1}: Different logic rank burst refresh I_{PP} current (1X REF)	x4	71	71	71	71	71	mA
I_{DD5B2}: Same logic rank burst refresh current (1X REF)	x4	390	390	390	390	390	mA
I_{PP5B2}: Same logic rank burst refresh I_{PP} current (1X REF)	x4	27	27	27	27	27	mA
I_{DD6N}: Self refresh current; 0–85°C[1]	x4	108	108	108	108	108	mA
I_{PP6x}: Self refresh I_{PP} current; 0–95°C [26]	x4	20	20	20	20	20	mA
I_{DD6E}: Self refresh current; 0–95°C[2]	x4	180	180	180	180	180	mA

Table 40: 4-High I_{DD}, I_{PP} and I_{DDQ} Current Limits; Die Rev. E (0° ≤ T_C ≤ 85°C) (Continued)

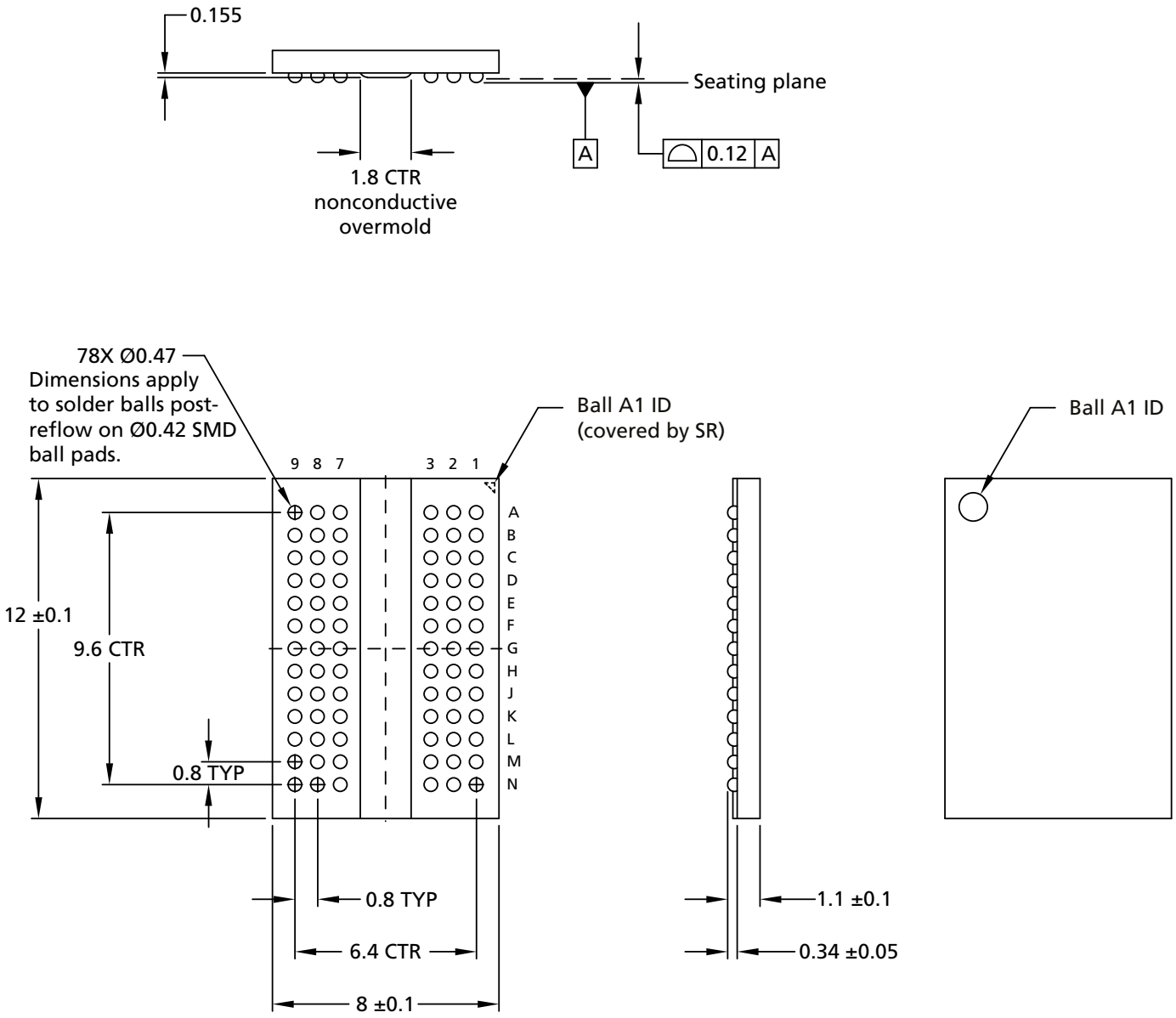
Symbol	Width	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-2933	DDR4-3200	Unit
I_{DD6R}: Self refresh current; 0–45°C[3,4]	x4	54	54	54	54	54	mA
I_{DD6A}: Auto self refresh current (25°C)[4]	x4	36	36	36	36	36	mA
I_{DD6A}: Auto self refresh current (45°C)[4]	x4	54	54	54	54	54	mA
I_{DD6A}: Auto self refresh current (75°C)[4]	x4	100	100	100	100	100	mA
I_{DD6A}: Auto self refresh current (95°C)[4]	x4	180	180	180	180	180	mA
I_{DD7}: Bank interleave read current	x4	250	270	290	310	330	mA
I_{PP7}: Bank interleave read I_{PP} current	x4	14	14	14	14	14	mA
I_{DD8}: Maximum power-down current	x4	46	46	46	46	46	mA

Notes:
1. Applicable for MR2 settings A7 = 0 and A6 = 0; manual mode with normal temperature range of operation (0–85°C).
2. Applicable for MR2 settings A7 = 1 and A6 = 0; manual mode with extended temperature range of operation (0–95°C).
3. Applicable for MR2 settings A7 = 0 and A6 = 1; manual mode with reduced temperature range of operation (0–45°C).
4. I_{DD6A}, I_{DD6R}, and I_{DD6E} are verified by design and characterization, and may not be subject to production test.
5. When additive latency is enabled for I_{DD0}, current changes by approximately +1%.
6. When additive latency is enabled for I_{DD1}, current changes by approximately +15%.
7. When additive latency is enabled for I_{DD2N}, current changes by approximately +0.5%.
8. When DLL is disabled for I_{DD2N}, current changes by approximately -4%.
9. When CAL is enabled for I_{DD2N}, current changes by approximately –18%.
10. When gear-down is enabled for I_{DD2N}, current changes by approximately -4%.
11. When CA parity is enabled for I_{DD2N}, current changes by approximately +10%.
12. When additive latency is enabled for I_{DD3N}, current changes by approximately +1%.
13. When additive latency is enabled for I_{DD4R}, current changes by approximately +5%.
14. When additive latency is enabled for I_{DD4W}, current changes by approximately +5%.
15. When write CRC is enabled for I_{DD4W}, current changes by approximately -10%.
16. When CA parity is enabled for I_{DD4W}, current changes by approximately +8%.
17. When 2X REF is enabled for I_{DD5B1}, current changes by approximately –28%.
18. When 4X REF is enabled for I_{DD5B1}, current changes by approximately –42%.
19. When 2X REF is enabled for I_{PP5B1}, current changes by approximately –28%.
20. When 4X REF is enabled for I_{PP5B1}, current changes by approximately –42%.
21. When 2X REF is enabled for I_{DD5B2}, current changes by approximately –25%.
22. When 4X REF is enabled for I_{DD5B2}, current changes by approximately –36%.
23. When 2X REF is enabled for I_{PP5B2}, current changes by approximately –25%.
24. When 4X REF is enabled for I_{PP5B2}, current changes by approximately –36%.
25. I_{PP0} test and limit is applicable for I_{DD0} and I_{DD1} conditions.
26. I_{PP6x} is applicable to I_{DD6N},I_{DD6E},I_{DD6R} and I_{DD6A} conditions.
27. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x}, I_{DD6} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
28. I_{PP3N} test and limit is applicable for all I_{DD2x}, I_{DD3x}, I_{DD4x}, I_{DD6} and I_{DD8} conditions; that is, testing I_{PP3N} should satisfy the I_{PP}s for the noted I_{DD} tests.
29. DDR4-1600 and DDR4-1866 use the same I_{DD} limits as DDR4-2133
30. The I_{DD} values must be derated (increased) when operated between 85°C ≤ T_C ≤ 95°C:

I_{DD0}, I_{DD1}, I_{DD2N}, I_{DD2NT}, I_{DD2Q}, I_{DD3N}, I_{DD3P}, I_{DD4R}, I_{DD4W}, I_{DD5B1} and I_{DD5B2} must be derated by +3%; I_{DD2P} must be derated by +10%; All I_{PP} currents except I_{PP6x} must be derated by +3%. These values are verified by design and characterization, and may not be subject to production test.

Package Dimensions

Figure 14: 78-Ball FBGA Die Rev. G (package codes HPR and KVA)



Notes:
1. All dimensions are in millimeters.
2. Solder ball material: SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

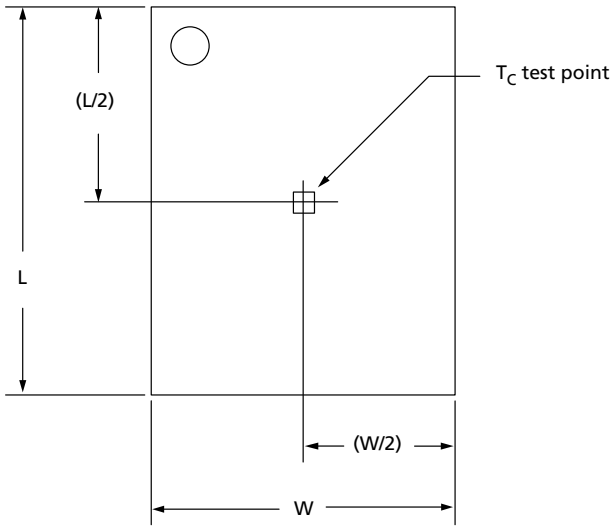
Thermal Characteristics

Table 41: Thermal Characteristics

Parameter/Condition			Value	Units	Symbol	Notes
Operating case temperature: Commercial			0 to +85	°C	T_C	1, 2, 3
			0 to +95	°C	T_C	1, 2, 3, 4
REV G	2H 78-ball "HPR"	Junction-to-case (TOP)	5.0	°C/W	ΘJC	5
		Junction-to-board	13.9	°C/W	ΘJB	
	4H 78-ball "KVA"	Junction-to-case (TOP)	3.4	°C/W	ΘJC	5
		Junction-to-board	14.1	°C/W	ΘJB	
REV E	2H 78-ball "DVN"	Junction-to-case (TOP)	6.3	°C/W	ΘJC	5
		Junction-to-board	15.4	°C/W	ΘJB	
	4H 78-ball "CLU"	Junction-to-case (TOP)	4.2	°C/W	ΘJC	5
		Junction-to-board	15.6	°C/W	ΘJB	

Notes:
1. MAX operating case temperature. T_C is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9µs interval refresh rate.
5. The thermal resistance data is based off of a typical number.

Figure 15: Thermal Measurement Point



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-4000
www.micron.com/products/support Sales inquiries: 800-932-4992

This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.