CML Microcircuits
COMMUNICATION SEMICONDUCTORS

CMX7241/CMX7341
PMR Common Platform Processor

7241/7341FI-1.x: dPMR™ and Analogue PMR Processor with Rx I/Q Support

D/7241_7341_FI1.x/5 November 2015 **DATASHEET** Advance Information

Features

- **Auto detect of Digital and Analogue Receive**
- **Digital PMR Functions:**
  - dPMR™ (ETSI TS 102 658) Compliant
  - Air Interface Physical Layer (Layer 1)
  - Air Interface Data Link Layer (Layer 2)
  - Mode 1: peer-to-peer mode
  - Mode 2: peer-to-peer mode with repeater operation
  - Mode 3: trunked mode support
  - Status, Type 1, Type 2 and Packet Data
- **Tx Sequencer**
- **Analogue PMR EN 300 086 / TIA 603D:**
  - Voice processing
  - De-emphasis / Pre-emphasis
  - Tx Limiter and splatter filter
  - Voice Scrambler
  - Voice Compander
  - CTCSS and DCS generation and detection
  - Support for external CTCSS and DCS
  - Selcall generation and detection
  - DTMF generation and detection
  - 1200/2400 bps FFSK modem (MPT1327 compatible)

Additional Features

- **2 Auxiliary ADCs (4 Multiplexed Inputs)**
- **4 Auxiliary DACs**
- **2 Auxiliary System Clock Outputs**
- **Tx Outputs for Two-point or I/Q Modulation**
- **Rx Inputs for Limiter/discriminator or CMX994 Direct Conversion (I/Q) Receiver**
- **C-BUS serial interface to CMX994 transceiver**
- **Vocoder Management and Control (CMX6x8 RALCWI Vocoder or CMX7262 TWELP Vocoder)**
- **Voice Codec supports external vocoders (SPI/PCM/I2S compatible - e.g. AMBE+2)**
- **C-BUS Serial Interface to Host micro**
- **Flexible Powersave Modes**
- **Low-power (3.3V) Operation**
- **Dedicated hardware reset pin**
- **Single-ended inputs (CMX7241)**
- **Differential inputs (CMX7341)**
- **Available in LQFP or VQFN Packages (CMX7341 – VQFN only)**

Applications

- **Multi-mode PMR radio**
- **FDMA digital PMR**
- **Analogue PMR**

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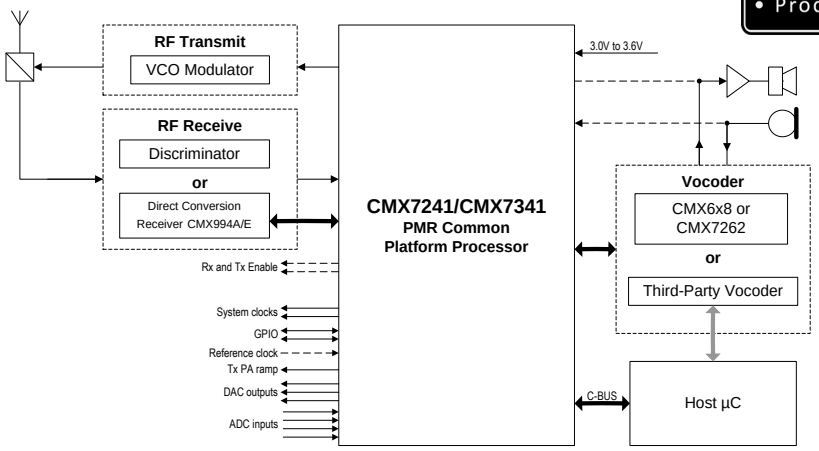

Datasheet User Manual

1 Brief Description

The 7241/7341FI-1.x Function Image™ (FI) implements a half-duplex 4FSK modem and a large proportion of the dPMR™ Air Interface (physical) layer and Data Link layer. In addition, the device also supports Analogue FM voice modes with flexible signalling options. In conjunction with a suitable host and an RF transceiver, a compact, low-cost, low-power digital PMR radio conforming to ETSI's dPMR™ standard TS 102 658 and Analogue EN 300 086 / TIA 603D can be realised. The device analyses incoming traffic, detects the modulation type and switches to the associated operating mode. This ensures that dual mode, analogue/digital PMR/ dPMR™ operation can be achieved on a single radio platform without the need to re-configure hardware or software by loading alternative FIs.

The CMX7241 and CMX7341 when loaded with the FI are identical in functionality; the only difference between the two devices is in the input stage: the CMX7241 has single-ended inputs and the CMX7341 is a differential input version.

The embedded functionality of the 7241/7341FI-1.x, managing voice and data systems autonomously, including CMX6x8 RALCWI Vocoder or CMX7262 TWELP Vocoder control (via the Auxiliary SPI/C-BUS interface), minimises host microcontroller interactions enabling the lowest operating power and therefore the longest battery life for a dPMR™ radio. The CMX7241/7341 can also provide audio codec functionality for vocoders under direct host control.

The in-built signalling options allow the device to be implemented into legacy Analogue FM systems making use of CTCSS / DCS sub-audio signalling, Selcall / DTMF signalling or 1200/2400 bps FFSK trunked systems using MPT1327 or custom protocols.

Both digital and analogue functionality can be active at the same time, allowing the host to auto-detect the type of signalling on the channel.

The device allows the designer to choose between a conventional limiter/discriminator receiver architecture or an I/Q-based direct conversion architecture utilising the built-in support for the CMX994 Direct Conversion Receiver.

The device utilises CML's proprietary *FirmASIC®* component technology. On-chip sub-systems are configured by a Function Image™: This is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from an external serial memory or host microcontroller over the built-in C-BUS serial interface. The device's functions and features may be enhanced by future Function Image™ releases, facilitating in-the-field upgrades. This document refers specifically to the features provided by Function Image™ 7241/7341FI-1.1.x.x

Other features include two auxiliary ADCs with four selectable inputs and four auxiliary DAC interfaces (with an optional RAMDAC on the first DAC output, to facilitate transmitter power ramping).

The device has flexible powersaving modes and is available in the following packages: CMX7241 (VQFN and LQFP), CMX7341 (VQFN only).

Note that text shown in pale grey indicates features that will be supported in future versions of the Function Image™.

This datasheet is the first part of a two-part document comprising datasheet and user manual: the datasheet/user manual combination can be obtained by registering your interest in this product with your local CML representative.

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History

Version	Changes	Date
5	• 8.3.1: Add P0.4 and P0.5, Input Fine Gain adjust • Table 10 and 11: corrected pin connections • Add support for CMX994A and CMX994E and additional power-saving descriptions • Change R20, 21 to 47k (was 470k). • Corrected Table 12 (swap DVss and DVdd).	November 2015
4	• Changes to Program Block 3 (ordering) for compatibility with 7241/7341FI-2 – **not backwards compatible.** Defined timers for GPIO A/B Tx Sequencer control. • Changes to Program Block 6 (GPIO A/B Tx Sequencer control enable) • Added description for No Tone bit in DTMF generation and $B6 definition • Default Audio Tone Tx level updated • Corrected GPIOA/B allocation in SPI mode (B is SCLK)	February 2015
3	Updated to reflect changes to improve commonality with 7241/7341FI-2: • Xtal frequency set to 19.2MHz, new settings for P3.13-21 • Moved 4FSK Modem Configuration register from $C7 to $A1 (and updated references throughout) • Moved Aux Data 2 register from $A3 to $A2 • Moved SPI control bits (b1:0) from $B1 to new register in $A0 • Added SPI mux control and GPIO A/B controls to P6.0 • Updated programming block write mechanism and CMX994 pass-through mode. • Moved GPIO write function from $A7 to $A8 under new steering nibble option (1) • Program blocks 0 and 3 rearranged • Some IQ related functions moved from P2.0 to P3.0 • Serial Memory FI load section removed • Legacy FI load section removed • FI load section updated to support FIFO / streaming mode • FFSK Modem Format option added to Analogue Control ($C3)	December 2014
2	• Added Analogue PMR Status register ($9B) • Updated Mode Control Readback description ($9A) • Tx I/Q control moved to P1.6 from $C7	September 2014
1	• First release, Advance Information	August 2014

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document.
Information in this datasheet should not be relied upon for final product design.

2 Block Diagram

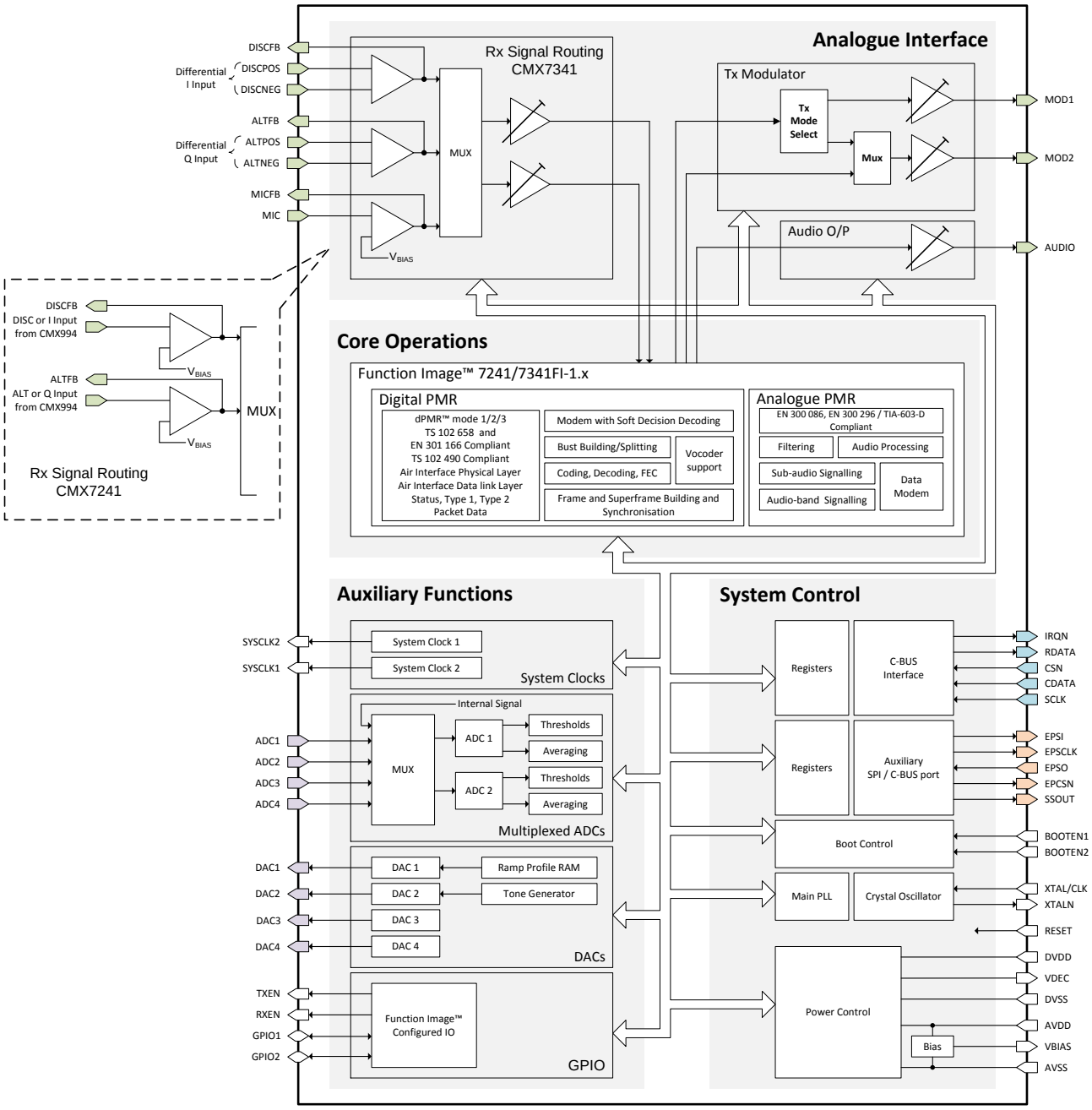


Figure 1 CMX7241/CMX7341 Block Diagram

3 Signal List

CMX7241 48-pin Q3/L4	CMX7341 48-lead Q3	Pin Name	Type	Description	
1	**1**	EPSI	OP	Serial Data Output	Auxiliary SPI/C-BUS
2	**2**	EPSCLK	OP	Serial Clock Output	
3	**3**	EPSO	IP+PD	Serial Data Input	
4	**4**	EPCSN	OP	Serial Chip Select for CMX994	
5	**5**	BOOTEN1	IP+PD	Used in conjunction with BOOTEN2 to determine the operation of the bootstrap program	
6	**6**	BOOTEN2	IP+PD	Used in conjunction with BOOTEN1 to determine the operation of the bootstrap program	
7	**7**	RESET	PWR	Dedicated reset function – active high. When asserted has the same effect as a power on reset. If unused, tie to DVSS	
8	**8**	IRQN	OP	A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.	Host C-BUS
9	**9**	VDEC	PWR	Internally-generated 1.8V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed. If the device is to be run from a 1.8V external supply then the VDEC pin must be connected directly to the external 1.8V regulated supply.	
10	**10**	RXENA	OP	Rx Enable – active when in Rx mode ($C1:b0 = 1)	
11	**11**	GPIOA	BI	General Purpose I/O pin	
12	**12**	GPIOB	BI	General Purpose I/O pin	
13	**13**	SYSCLK1	OP	Synthesised Digital System Clock Output 1	
14	**14**	DVSS	PWR	Digital ground	
15	**15**	TXENA	OP	Tx Enable – active when in Tx mode ($C1:b1 = 1)	
16		DISC	IP	Discriminator inverting input or I input from CMX994	
17		DISCFB	OP	Discriminator input amplifier feedback	
18		ALT	IP	Alternate inverting input or Q input from CMX994	
19		ALTFB	OP	Alternate input amplifier feedback	
	16	DISCPOS	IP	Differential input1, positive and negative. I input from CMX994	
	17	DISCNEG	IP		
	18	DISCFB	OP	Input1 amplifier feedback	
	19	ALTPOS	IP	Differential input2, positive and negative. Q input from CMX994	
	20	ALTNEG	IP		

CMX7241 48-pin Q3/L4	CMX7341 48-lead Q3	Pin Name	Type	Description	
	21	ALTFB	OP	Input2 amplifier feedback	
20	**22**	MICFB	OP	Microphone input amplifier feedback	
21	**23**	MIC	IP	Microphone inverting input	
22	n/c	AVSS	PWR	Analogue ground	
23	**24**	MOD1	OP	Modulator 1 output	
24	**25**	MOD2	OP	Modulator 2 output	
25	**26**	VBIAS	OP	Internally generated bias voltage of approx. $AV_{DD}/2$, except when the device is in 'Powersave' mode when V_{BIAS} will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed unless buffered.	
26	**27**	AUDIO	OP	Audio Output in SPI-Codec mode	
27	**28**	ADC1	IP	Auxiliary ADC input 1	Each of the two ADC blocks can select its input signal from any one of these input pins, or from the MIC, ALT or DISC input pins. See section 6.14 for details.
28	**29**	ADC2	IP	Auxiliary ADC input 2	
29	**30**	ADC3	IP	Auxiliary ADC input 3	
30	**31**	ADC4	IP	Auxiliary ADC input 4	
31	**32**	AVDD	PWR	Analogue +3.3V supply rail. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.	
32	**33**	DAC1	OP	Auxiliary DAC output 1 / RAMDAC	
33	**34**	DAC2	OP	Auxiliary DAC output 2 / Tone Generator output	
34	n/c	AVSS	PWR	Analogue ground	
35	**35**	DAC3	OP	Auxiliary DAC output 3. See Note 2	
36	**36**	DAC4	OP	Auxiliary DAC output 4	
37	**37**	DVSS	PWR	Digital Ground	
38	**38**	VDEC	PWR	Internally generated 1.8V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed. If the device is to be run from a 1.8V external supply, then VDEC pin must be connected directly to the 1.8V external regulated supply.	
39	**39**	XTAL/CLK	IP	Input from the external clock source or Xtal	
40	**40**	XTALN	OP	The output of the on-chip Xtal oscillator inverter. NC if external clock used.	
41	**41**	DVDD	PWR	Digital +3.3V supply rail. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins.	
42	**42**	CDATA	IP	Command Data input from the µC	Host C-BUS
43	**43**	RDATA	TS OP	Reply Data tri-state output to the µC (high impedance when not sending data to the µC).	

CMX7241 48-pin Q3/L4	CMX7341 48-lead Q3	Pin Name	Type	Description	
44	**44**	SSOUT	OP	Serial Chip Select for CMX6x8/CMX7262 or Frame Sync for SPI Codec	Auxiliary SPI/C-BUS
45	**45**	DVSS	PWR	Digital ground	
46	**46**	SCLK	IP	Serial clock input from the µC	Host C-BUS
47	**47**	SYSCLK2	OP	Synthesised Digital System Clock 2	
48	**48**	CSN	IP	Chip Select input from the µC (no internal pullup on this input)	Host C-BUS
Exposed Metal Pad	**Exposed Metal Pad**	SUBSTRATE	~	The central metal pad (which is exposed on Q3 package only) must be connected to analogue ground (AV_{SS}). **No other electrical connection is permitted.**	

Note 1: IP = Input (+ PU/PD = internal pullup / pulldown resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal.

Colour Definitions:

= Aux SPI/C-BUS
= Host C-BUS
= Analogue Inputs/Outputs
= ADCs/DACs

Note 2: In CMX7341 only, this is a dual-purpose pin which, for some FIs, may have an alternative configuration. However for FI-1, this pin ONLY functions as DAC3.

3.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
V_{DEC}	VDEC	Power supply for core logic, derived from DVDD by on-chip regulator
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AVDD
AV_{SS}	AVSS	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits

4 Component and PCB Recommendations

4.1 Recommended External Components

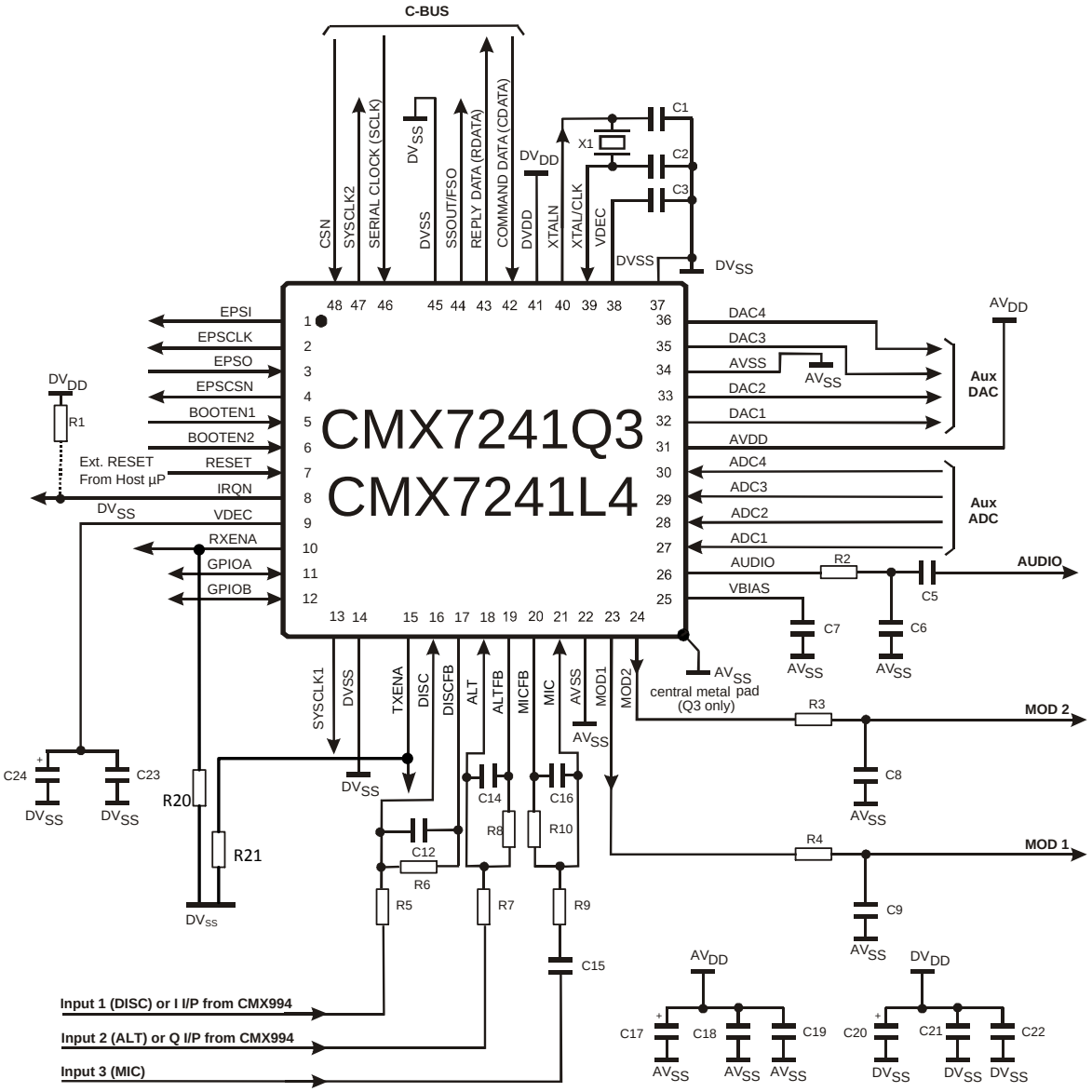


Figure 2 CMX7241 (L4 and Q3) Recommended External Components

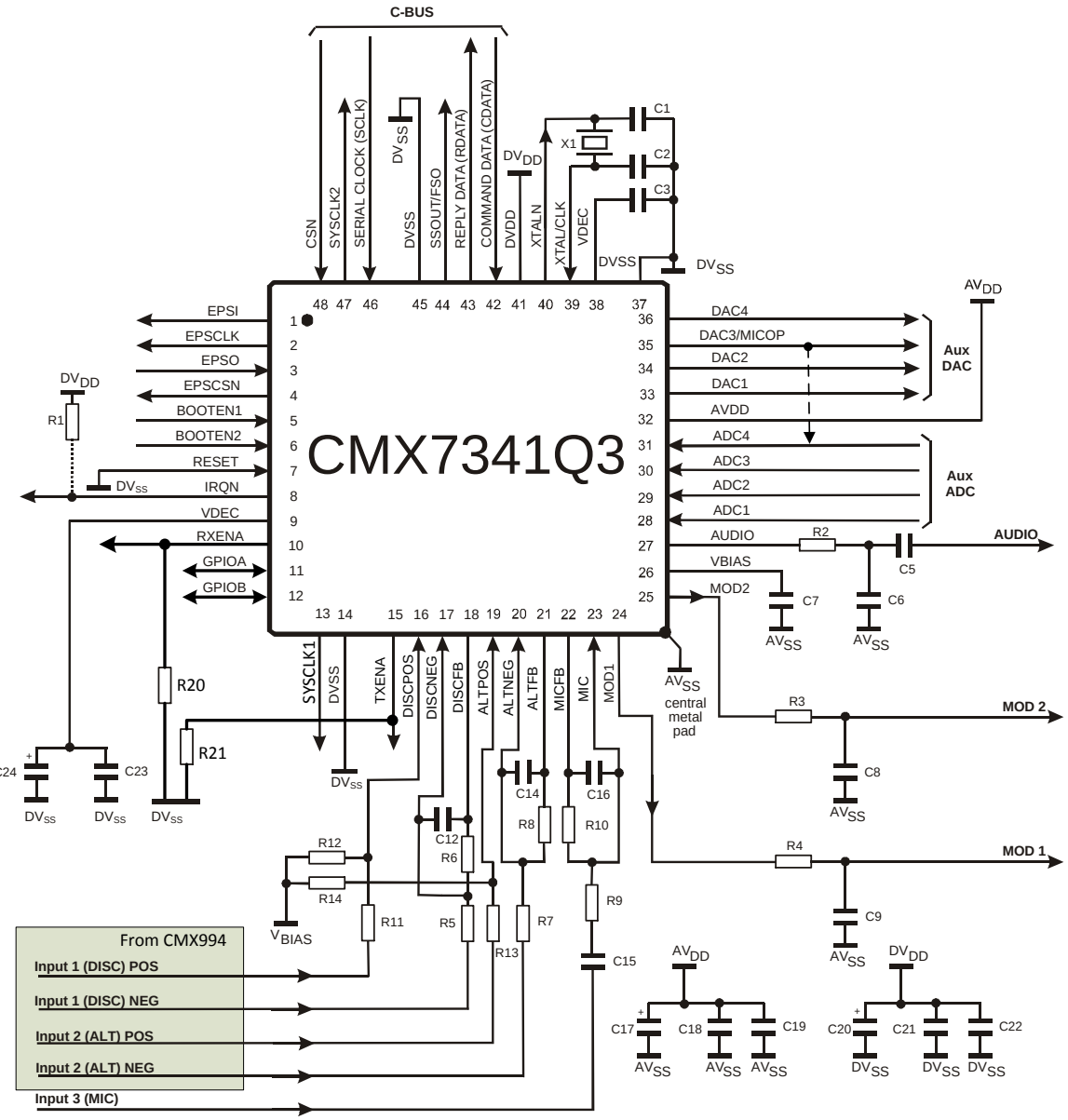


Figure 3 CMX7341 (Q3) Recommended External Components

Table 2 Recommended External Components

R1	100kΩ	C1	18pF	C11	not used	C21	10nF
R2	20kΩ	C2	18pF	C12	100pF	C22	10nF
R3	20kΩ	C3	10nF	C13	not used	C23	10nF
R4	20kΩ	C4	not used	C14	100pF	C24	10µF
R5	100kΩ (note 2)	C5	1nF	C15	note 5		
R6	100kΩ	C6	100pF	C16	200pF		
R7	100kΩ (note 3)	C7	1µF	C17	10µF		

R8	100kΩ	C8	100pF	C18	10nF	X1	19.2MHz
R9	See note 4	C9	100pF	C19	10nF		See note 1
R10	100kΩ	C10	not used	C20	10µF		
R11	100kΩ						
R12	100kΩ	R20	47kΩ				
R13	100kΩ	R21	47kΩ				
R14	100kΩ						

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. By default, a 19.2MHz oscillator is assumed (in which case C1 and C2 are not required), other values could be used if the various internal clock dividers are set to appropriate values.

2. For CMX7241 operation, R5 should be selected to provide the desired dc gain of the discriminator input, as follows:

$$|GAIN_{DISC}| = 100k\Omega / R5$$

   The gain should be such that the resultant output at the DISCFB pin is within the DISC input signal range specified in 6.17.2. For 4FSK modulation, this signal should be dc coupled from the Limiter/ Discriminator output.

3. For CMX7241 operation, R7 should be selected to provide the desired dc gain of the alternative input as follows:

$$|GAIN_{ALT}| = 100k\Omega / R7$$

   The gain should be such that the resultant output at the ALTFB pin is within the alternative input signal range specified in 6.17.

4. R9 should be selected to provide the desired dc gain (assuming C15 is not present) of the microphone input as follows:

$$|GAIN_{MIC}| = 100k\Omega / R9$$

   The gain should be such that the resultant output at the MICFB pin is within the microphone input signal range specified in 6.17.1. For optimum performance with low signal microphones, an additional external gain stage may be required.

5. C15 should be selected to maintain the lower frequency roll-off of the MIC input as follows:

$$C15 \geq 30nF \times |GAIN_{MIC}|$$

6. When used with a Limiter/Discriminator Receiver, ALT and ALTFB connections allow the user to have a second discriminator or microphone input. Component connections and values are as for the respective DISC and MIC networks. If this input is not required, the ALT pin should be connected to AV_{SS}.

7. AUDIO output is used when SPI-Codec or Analogue mode has been selected.

8. A single 10µF electrolytic capacitor (C24, fitted as shown) may be used for smoothing the power supply to both VDEC pins, providing they are connected together on the pcb with an adequate width power supply trace. Alternatively, separate smoothing capacitors should be connected to each VDEC pin. High frequency decoupling capacitors (C3 and C23) must always be fitted as close as possible to both VDEC pins.

9. TXENA and RXENA should be pulled down by an external resistor (R20, R21) to be directly compatible with the CMX994 (active high signals). For compatibility with earlier 7141-based FI operation, they should be pulled high (active low signals).

4.2 PCB Layout Guidelines and Power Supply Decoupling

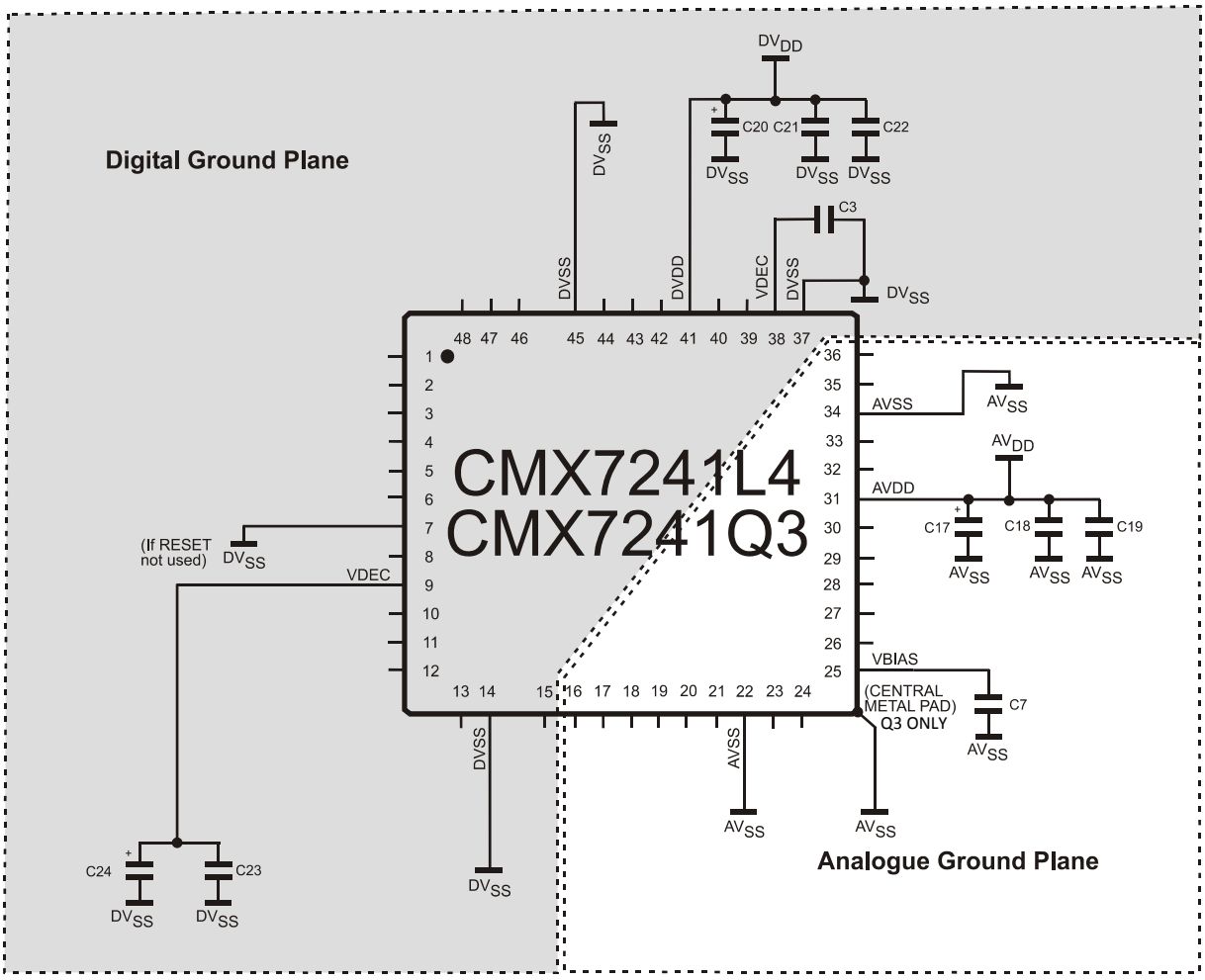


Figure 4 CMX7241 (L4/Q3) Power Supply and De-coupling

Component Values as per Figure 2

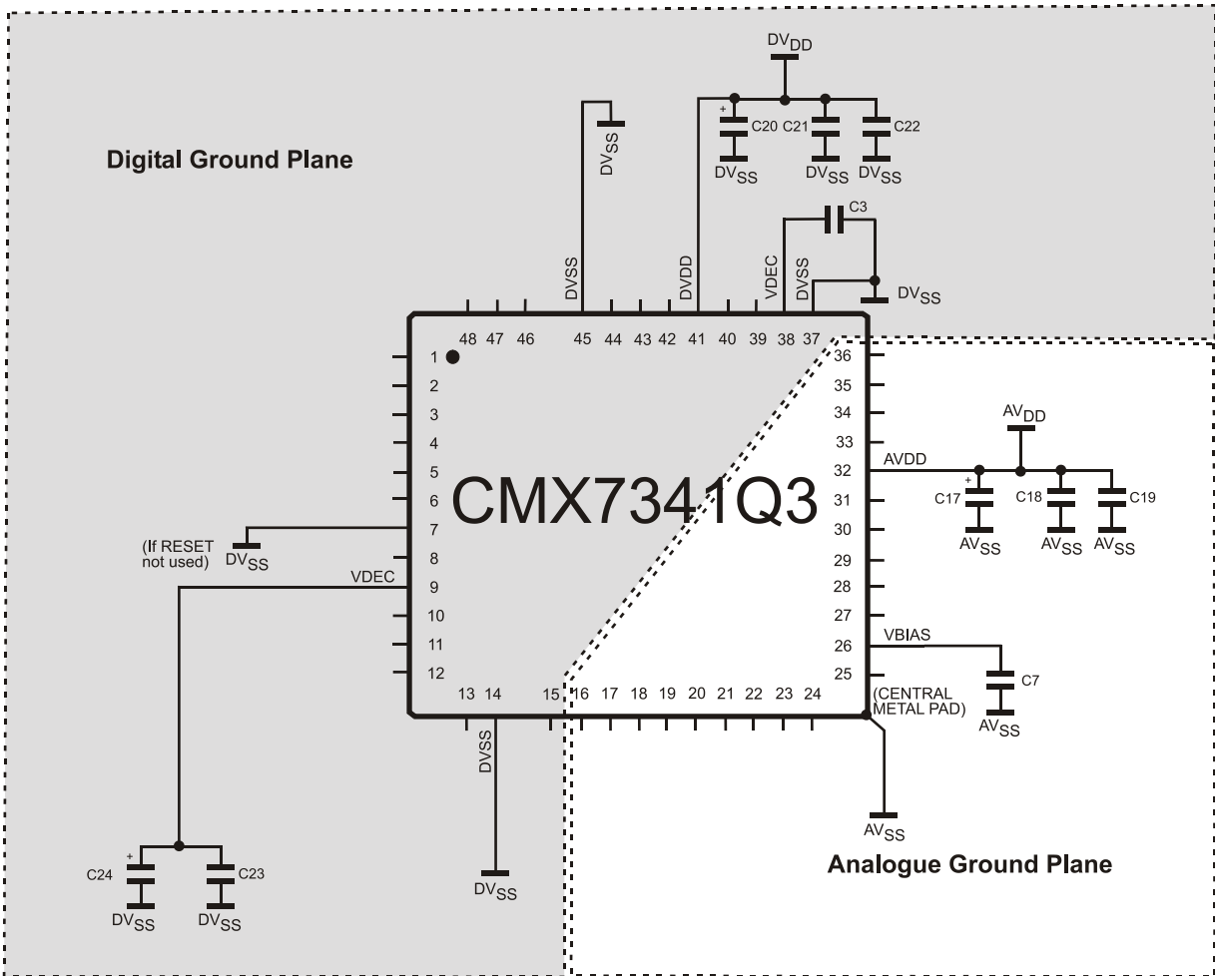


Figure 5 CMX7341 (Q3) Power Supply and De-coupling

Component Values as per Figure 2

Notes:

It is important to protect the analogue pins from extraneous in-band noise and to minimise the impedance between the CMX7241/7341 and the supply and bias de-coupling capacitors. The de-coupling capacitors C3, C7, C18, C19, C21, C22 and C24 should be as close as possible to the CMX7241/7341. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AVSS and DVSS supplies in the area of the device, with provision to make links between them, close to the device. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

VBIAS is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If VBIAS needs to be used elsewhere in the design, it should be buffered with a high input impedance buffer.

The single ended microphone input and audio output must be ac coupled (as shown), so that their return paths can be connected to AVSS without introducing dc offsets. Further buffering of the audio output is advised.

The crystal, X1, may be replaced with an external clock source.

The device executes an internal scheduler running at 4kHz, which may result in current “spikes” on the DVDD line, which must be taken into account when designing the power supply circuitry.

4.3 CMX994/CMX994A/CMX994E Interface

When operating the CMX7241 and CMX7341 in I/Q mode, the interface to the CMX994 shown in Figure 6 and Figure 7 respectively should be used. Component values are shown in Table 3. Where values are not shown refer to the CMX994/A/E Datasheet. The CMX7341 allows for a differential interface directly to the CMX994. Resistors R20 and R21 are required to ensure that the TXENA and RXENA signals are kept in an inactive state during FI loading, and to inform the FI that these signals should be implemented active high.

The CMX994 and the CMX7341 may share the same 19.2MHz reference (however note that the CMX7341 requires a CMOS logic compatible signal).

AuxADC1 is configured to sense the Adjacent / Alternate channel power levels and so improve the performance of the CMX994 AGC system in situations where high levels of interference may be encountered. The CMX994 should be connected to the Auxilliary SPI/C-BUS using EPCSN as the chip select.

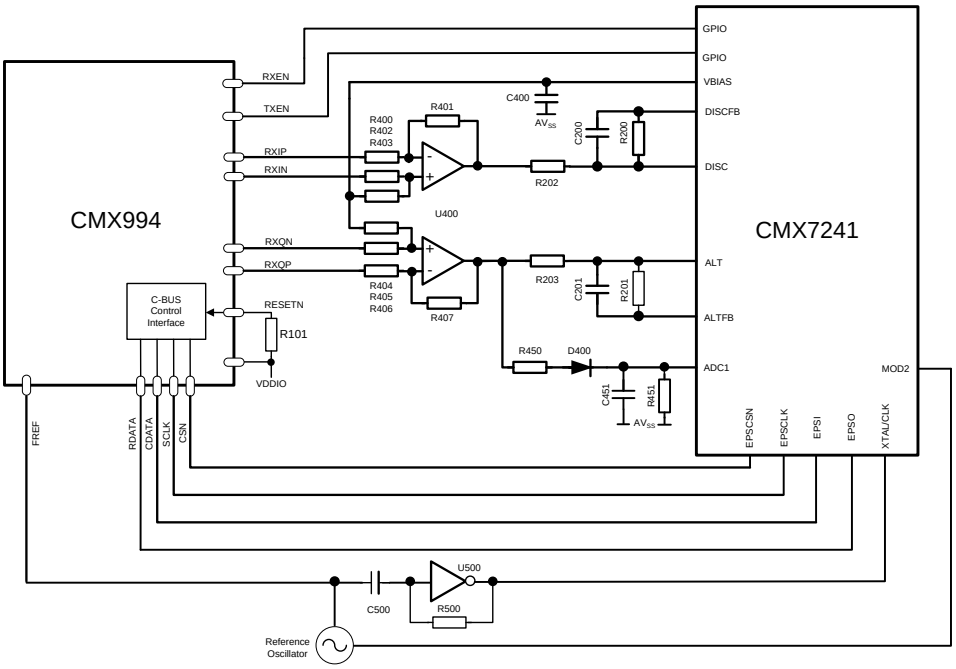


Figure 6 CMX7241/CMX994 Interface

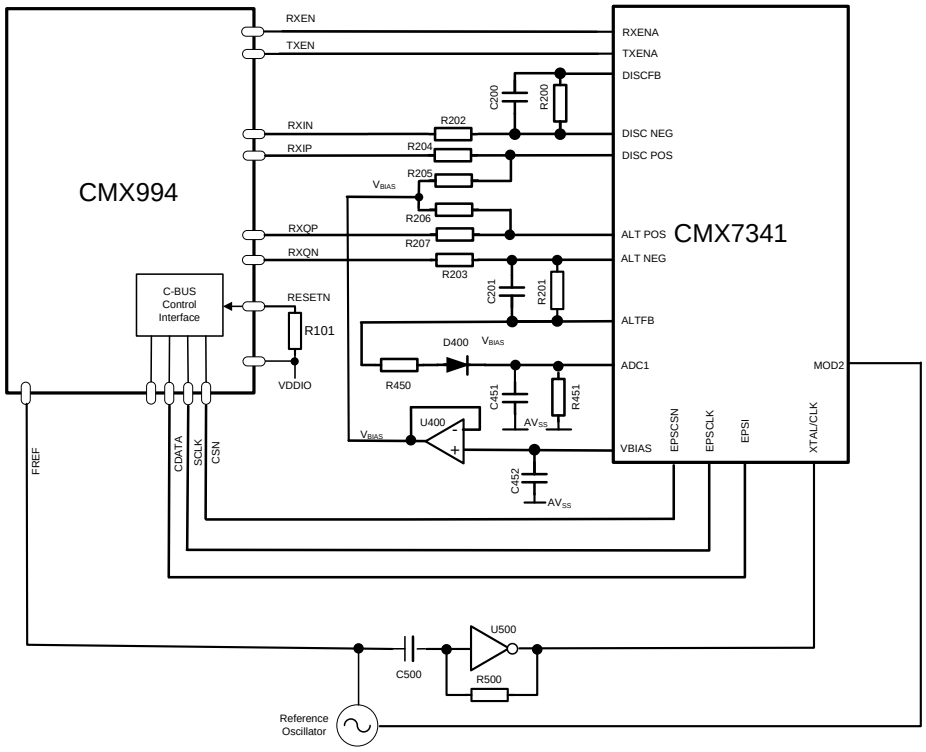


Figure 7 CMX7341/CMX994 Interface

Table 3 Recommended External Components when using CMX994

R101	100kΩ	C200	100pF	D400	MMBD1503A
R200 to R207	100kΩ	C201	100pF	U400	e.g. LMV931MG
R450	22kΩ	C400	100nF	U500	e.g. SN74AHC1G04DRL
R451	1MΩ	C451	1nF		
R500	100kΩ	C452	100nF		
		C500	1nF		

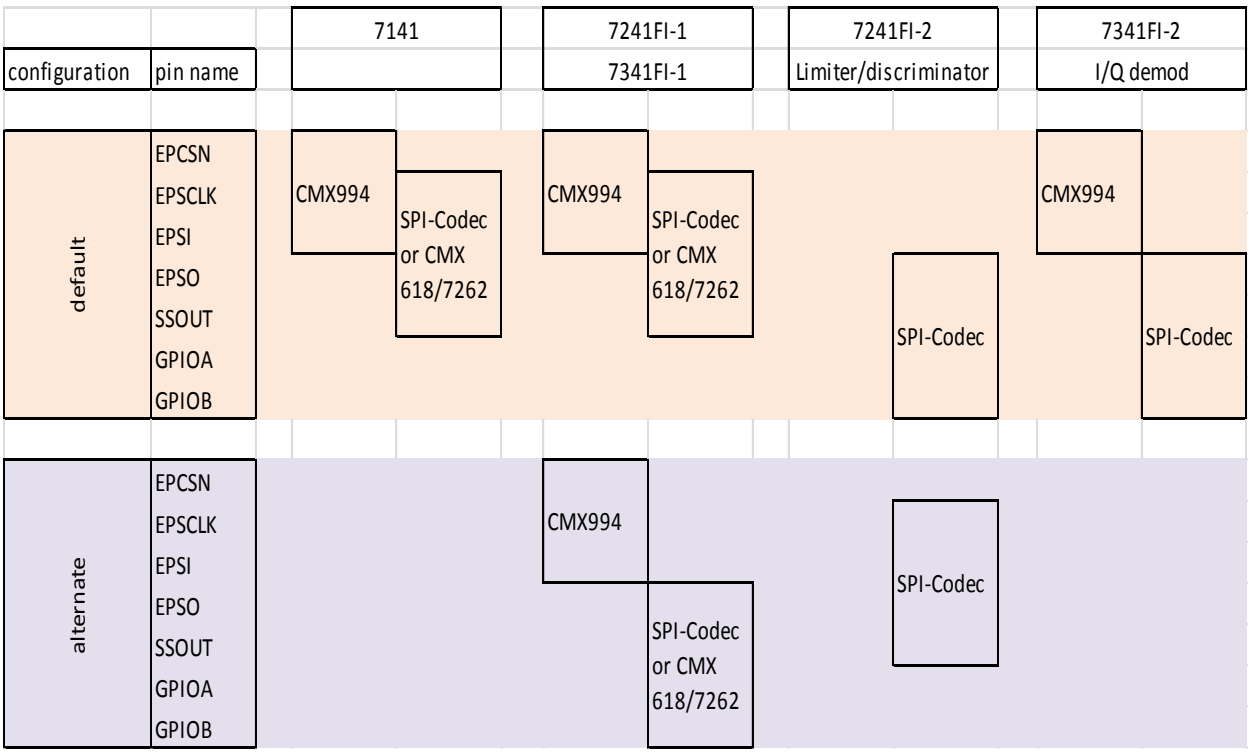
4.4 Serial Port Interfaces

Two serial ports are available on the device to interface to a CMX994 and provide an audio SPI-codec interface. On the 7241FI-1 these can be multiplexed together (with separate CSN signals) or entirely separate, whilst on the 7241/7341FI-2 they must be kept separate.

Further information is available in Sections 5.6.2 and 5.6.3

Table 4 shows the options available and includes the CMX7141 to show where backwards compatibility is feasible.

Table 4 Serial Port Assignments



4.5 RESET Pin

This pin (pin 7) provides a dedicated reset function when connected to a suitable host microprocessor. To use reset the pin must be held high for a minimum of 100ns and then released. When the state of reset changes from 1 to 0, the same effect as a power-on reset is achieved.

5 General Description

5.1 7241/7341FI-1 Features

The 7241/7341FI-1.x Function Image™ is intended for use in half duplex digital PMR equipment using 4FSK modulation at 4.8kbps suitable for 6.25kHz channels and analogue FM using 12.5/25kHz channels. Both Analogue and Digital modes may be enabled simultaneously, allowing automatic detection of the signal type on the RF channel.

A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The device includes a crystal clock generator, with buffered output, to provide a common system clock if required. Block diagrams of the devices are shown in Figure 1. The signal processing blocks can be routed from any of the three DISC/ALT/MIC input pins.

5.2 Digital Features

Much of the dPMR™ ETSI TS 102 658 standard Air Interface protocol is embedded in the 7241/7341FI-1.x Function Image™ operation namely:

Air Interface Physical Layer 1

- 4FSK modulation and demodulation
- Bit and symbol definition
- Frequency and symbol synchronisation
- Transmission burst building and splitting

Air Interface Data Link Layer 2

- Channel coding (FEC, CRC)
- Interleaving, de-interleaving and bit ordering
- Frame and superframe building and synchronising
- Burst and parameter definition
- Link addressing (source and destination)
- Interfacing of voice applications (voice data) with the Physical Layer
- Data bearer services
- Exchanging signalling and/or user data with the Call Control Layer
- Automatic Own-ID and Group-ID detection

Mode 1 – Peer-to-peer direct communication network (without repeaters or infrastructure), using a single frequency channel.

Mode 2 – Centralised repeater network. Includes the functionality of Mode 1, and introduces compatibility with repeaters and infrastructure whereby all communication between devices is via a repeater/base station.

Mode 3 – Managed centralised repeater network. This is a fully-managed access mode which includes the functionality of Modes 1 and 2 but is also compatible with multi-channel and multi-site trunked networks using multiple repeaters/base stations. Note that, for Mode 3 operation, the host must be capable of handling the Beacon Channel and associated messages used by this mode. The Beacon Channel carries messages which are continuously monitored by the listening devices to control call set up.

5.3 Analogue Features

The device provides full audio/voice processing to suit the requirements of EN 300 086 and TIA 603D as well as comprehensive signalling to suit professional radio environments:

- Selectable pre-emphasis and de-emphasis

- Selectable voice compander
- Selectable frequency inversion scrambling
- Tx limiter and splatter filter
- Mic AGC
- Selectable sub-audio rejection filter
- CTCSS and DCS generator and decoder (including phase reversal detection)
- Support for external CTCSS/DCS generation and decoding with selectable filters
- 1200/2400 bps FFSK modem for MPT1327
- ADSW and CCSW reporting in MPT1327 mode
- 16-tone Selcall generator and decoder
- DTMF generator and decoder
- Tone generator

5.4 Auxiliary Functions

- Automatic Tx sequencer simplifies host control
- RAMDAC operation
- TXENA and RXENA hardware signals
- Two-point or I/Q modulation outputs
- Hard or soft data output options
- Two programmable system clock outputs
- Two auxiliary ADCs with four selectable external input paths
- Four auxiliary DACs, one with built-in programmable RAMDAC

5.5 Interface

- Optimised C-BUS (4-wire, high-speed synchronous serial command/data bus) interface to host for control and data transfer
- Open drain IRQ to host
- Auxiliary SPI/C-BUS interface to CMX6x8/CMX7262 or CMX994 with pass-through mode from host
- Auxiliary SPI-Codec bus interface for PCM speech codec to support third-party vocoders, e.g. AMBE+2
- Two GPIO pins
- C-BUS (host) boot mode.

5.6 System Design

5.6.1 General

A number of system architectures can be supported by the device. The two most significant architectural decisions are:

RF receiver:

- Limiter/Discriminator or
- I/Q using the CMX994 Direct Conversion Receiver

Vocoder:

- External/host based (all encoded data is transferred over the host C-BUS interface. The SPI interface may be used as an Audio Codec for PCM data – this is appropriate for use with the DVSI AMBE devices)
- Automatic control using either the CMX6x8 or CMX7262

The most highly-integrated solution uses a CMX6x8/CMX7262 Vocoder under full control of the device, relieving the host of all vocoder management duties. In this mode audio codec functions are provided by the CMX6x8/CMX7262. Other architectures using third-party vocoders are supported using SPI-Codec mode in

which the device acts as an external audio codec attached to the vocoder. In this mode the host must issue all control commands to the vocoder, and also transfer coded data packets between the vocoder and device. In both modes, the auxiliary SPI/C-BUS may be shared with the CMX994 if I/Q mode is selected.
The configuration of the auxiliary SPI/C-BUS port is controlled by the Program Register P6.0: b3-0. In SPI-Codec mode 16-bit PCM audio samples are transferred at 8ksps. When this mode is selected:

in Tx: the MIC input should be routed from MIC to Input1. The input signal is lowpass filtered, converted to 16-bit linear PCM at 8ksps and then output on the EPSI pin of the SPI-Codec port for the external vocoder to process.

in Rx: the AUDIO output should be routed from Output1. 16-bit linear PCM samples are read from the EPSO pin of the SPI-Codec port, then filtered and output via the Audio Output Attenuator. This mode can also be used for voice annunciations/warnings etc.

5.6.2 Implementation using the CMX6x8 and CMX7262

Figure 8 and Figure 9 show the configuration using the CMX6x8 RALCWI Vocoder or CMX7262 TWELP Vocoder where all control and data is handled by the device with minimal host CPU involvement. Speaker and Mic signals must be routed to both the CMX7241/7341 and the Vocoder to allow for both Analogue and Digital operation. See also Section 6.4

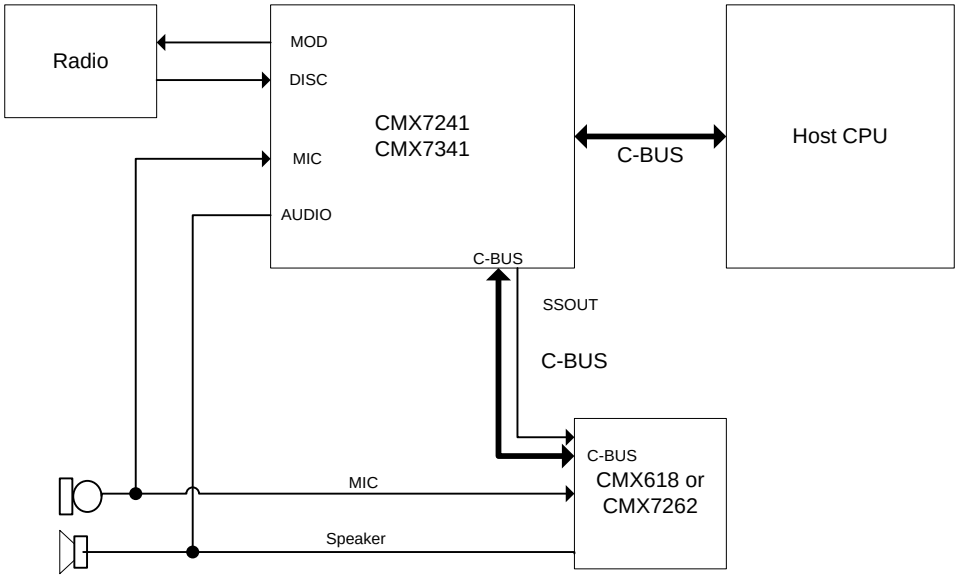


Figure 8 CMX618/CMX7262 Vocoder Connection

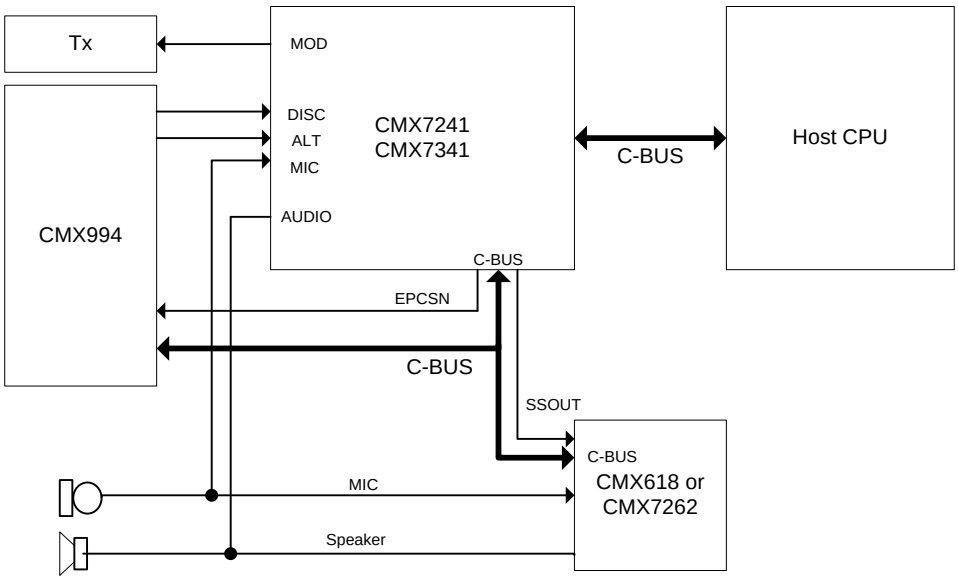


Figure 9 CMX6x8/CMX7262 and CMX994

If the CMX608 is to be used then there are two possible architectures available. If an external audio codec is available then the device can take full control over the CMX608 as in Figure 8. Otherwise the audio codecs within the device can be used at the expense of additional host activity. In this case, all channel data (control, addressing and payload) is transferred from the device to the host over the main C-BUS interface, and the host must then transfer the voice payload (TCH) data to the CMX608 using another C-BUS interface, as shown in Figure 10.

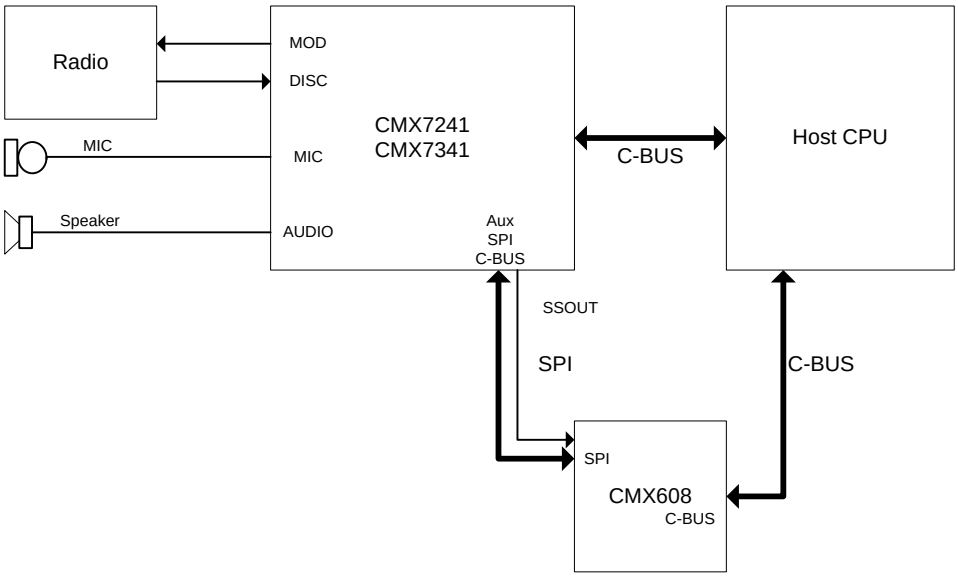


Figure 10 CMX608 Vocoder Connection

5.6.3 Implementing with Third-party Vocoders

As an alternative to the integrated architecture using the CMX6x8/CMX7262, it is possible to use a third-party vocoder by routing all payload data (including voice traffic channel data) through the main C-BUS to the host. The host can then transfer it to/from the third party vocoder over a suitable port supported by the chosen vocoder. Typically these vocoders do not include audio Digital-to-Analogue and Analogue-to-Digital converters, so the device can be configured to use the auxiliary C-BUS as an SPI interface and use its built-in

DAC/ADCs as audio converters to accept or deliver PCM audio samples. This architecture is shown in Figure 11 and Figure 12. See also section 6.5. Note that the vocoder functionality could be provided by the host micro in this mode.

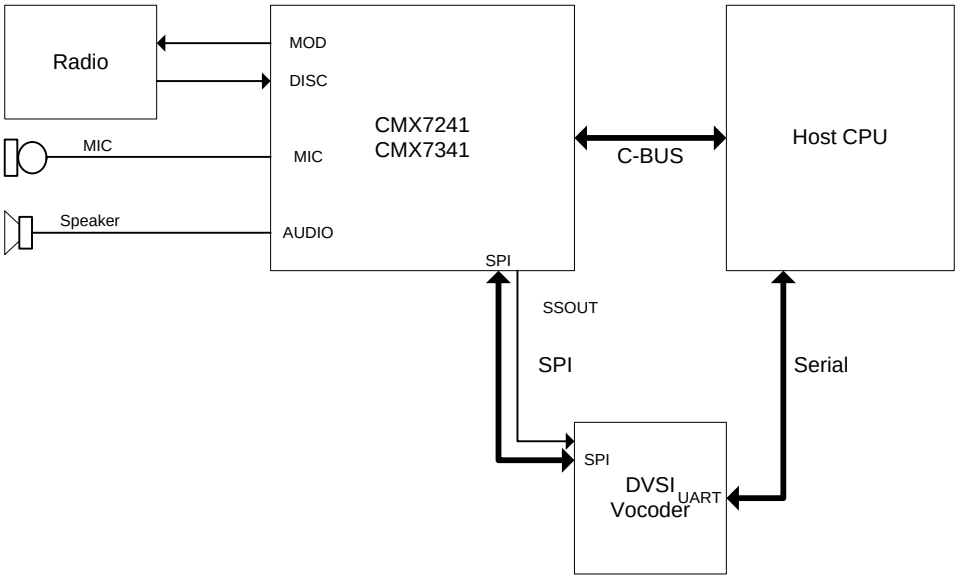


Figure 11 DVSI Vocoder Connection

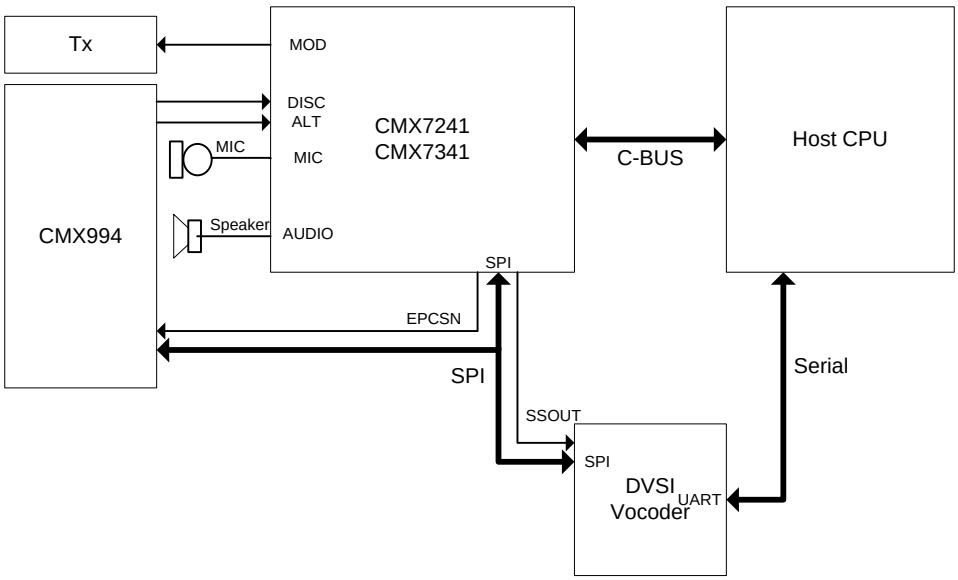


Figure 12 CMX994 and DVSI Vocoder Connection

5.6.4 Data Transfer

When transmitting, an initial block of payload or control channel data will need to be loaded from the host into the C-BUS TxData registers. The device can then format and transmit that data while at the same time loading in the following data blocks from the host or vocoder.

When receiving, the host needs to consider that when a signal is received over the air there will be a processing delay while the device filters, demodulates and decodes the output data before presenting it to the host or vocoder. For best performance, voice payload data can be output in soft-decision (4-bit log-likelihood ratio) format compatible with the CMX6x8, CMX7262 and other third-party vocoders, although this mode increases the data transfer rate over C-BUS by a factor of four.

5.6.5 CMX994 Connection (I/Q Mode)

The CMX994 can be connected via the C-BUS connection in place of the serial memory (Table 5). This allows the CMX994 to be used along with either the CMX6x8, CMX7262, DVSI vocoder or other third party vocoder. Note that the data and clock connections to the CMX994 may be common with the Vocoder so the data traffic on the interface is a potential source of noise / interference in the radio.

Table 5 CMX994 Connections

CMX7241/7341 Pin	CMX994 Pin
EPCSN	CSN
EPSI	CDATA
EPSCLK	SCLK
No connection	RDATA

The operation of the CMX994 is generally automatic, however specific data may be written to CMX994 registers using the pass-through mode available using register $C8. For example if the CMX994 PLL and VCO are used in the radio design then it is necessary to programme the appropriate frequency data to the CMX994 PLL-M Divider, PLL N-Divider and VCO Control registers using the pass-through mode before attempting reception.

The CMX994A/CMX994E devices are pin compatible with CMX994 and may be used instead. In order to make use of the advanced features Program Block P6.3 should be set appropriately.

5.6.6 Hardware AGC – AuxADC1 Connection

In I/Q mode the AuxADC1 input can be used to improve the adjacent/alternate channel rejection with the addition of suitable external components (shown in Figure 6). This function provides a broadband signal detector which is used in the AGC process. This is required to prevent the DISC/ALT ADC inputs limiting internally in the presence of strong alternate channel signals, which are attenuated by the inherent filtering of the ADC.

This functionality is enabled by setting:

- Program Block P6.0:b3=1 (enable hardware AGC)
- $C0:b6 = 1 (enable BIAS)
- $93 = $xx3C (AuxADC1 Enabled, averaging = 3, Routed from AuxADC input 1)
- $95 = $0185 (hi threshold)
- $94 = $0180 (lo threshold)

Note that threshold levels may need adjustment to suit particular hardware implementations.

5.6.7 RSSI Measurement (I/Q Mode)

In I/Q mode the RSSI is calculated from the signal levels present at the I and Q inputs and the AGC levels currently in use. Figure 13 shows a typical response.

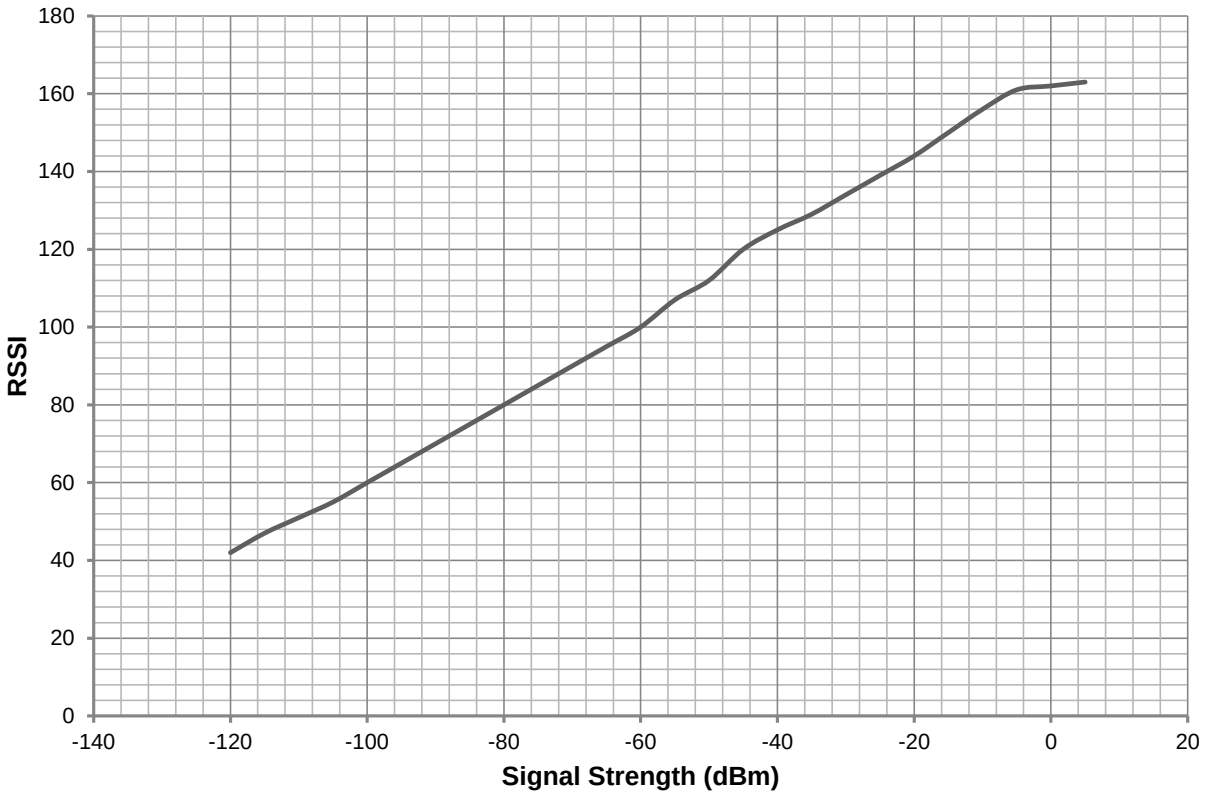


Figure 13 RSSI in I/Q Mode

5.6.8 RSSI Measurement (LD mode)

The AuxADC provided by the device can be used to detect the Squelch or RSSI signal from the RF section while the device is in Rx or Idle mode. This allows a significant degree of powersaving within the device and avoids the need to wake the host up unnecessarily. The host-programmable AuxADC thresholds allow for user selection of squelch threshold settings.

5.7 dPMR Modem Description

This modem can run at 4.8kbps occupying a 6.25kHz bandwidth RF channel. It has been designed such that, when combined with suitable RF, host controller, CMX6x8 or CMX7262 Vocoder and appropriate control software, it meets the requirements of the EN 301 166 standard. See www.etsi.org for details of these standards.

TS 102 658 is available on the ETSI web site (www.etsi.org) which describes a 6.25kHz channel spacing FDMA dPMR system. This standard uses a 4FSK modulation scheme with an over-air bit rate of 4800 bps (i.e. 2.4 ksymbols/s). With respect to dPMR formatted modes of operation, this document should be read in conjunction with the ETSI standard. TS 102 658. Mode 1 is largely compatible with (but not identical to) TS 102 490 (dPMR peer-to-peer mode for license-free operation) in CSF mode. TS 102 658 Mode 2 introduces repeater operation, whilst Mode 3 covers a fully-featured trunked mode. The additional features in Mode 2 and Mode 3 operation require significantly more host processing than Mode 1. For example, for Mode 3 operation the device must monitor the beacon channel for incoming frame types which are specific to trunked networks. This is described in more detail in Section 6.7.

The dPMR standard does not specify a voice coding algorithm, but the CMX618/CMX608 or CMX7262 (also available from CML) are suitable devices for this purpose. Alternatively, the device can be configured to act as an external Audio Codec for a third-party Vocoder (such as DVSI AMBE-3000).

5.7.1 Modulation

The dPMR 4FSK modulation scheme operates in a 6.25kHz channel bandwidth with a deviation index of 0.29 and has an over-air bit rate of 4.8 kbps (2.4 ksymbols/s). RRC filters are implemented in both Tx and Rx with a filter 'alpha' of 0.2. The maximum frequency error is +/-625 Hz and the CMX7241/7341 can adapt to the maximum time-base clock drift of 2ppm over the duration of a 180-second burst. Figure 16 shows the basic parameters of the 4FSK modulation, symbol mapping and filtering requirements.

Figure 14 and Figure 15 show a transmitted PRBS waveform, as recorded on a spectrum analyser in 36kHz span and zero-span mode, having been two-point modulated using a suitable RF transmitter.

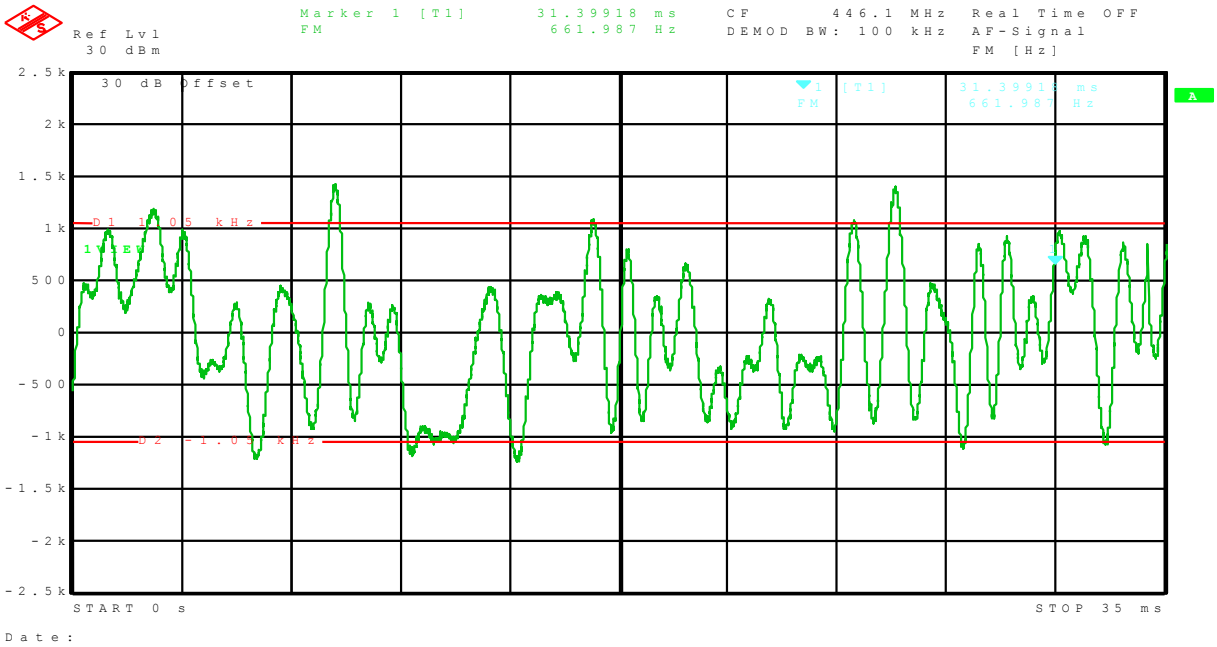


Figure 14 4FSK PRBS Waveform - Modulation

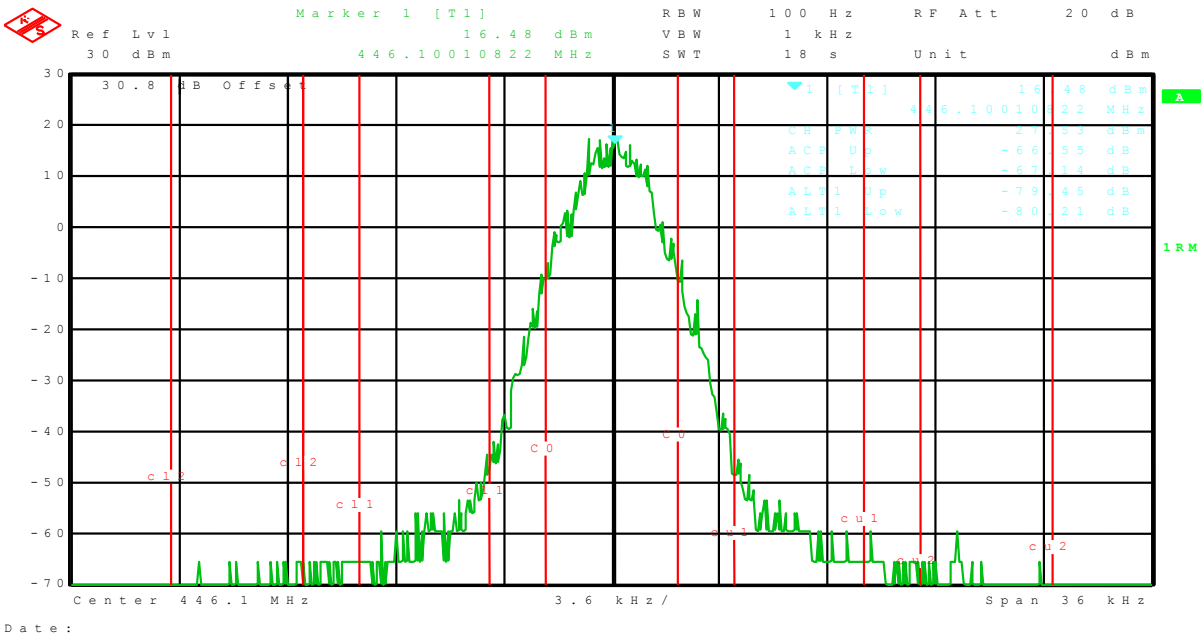
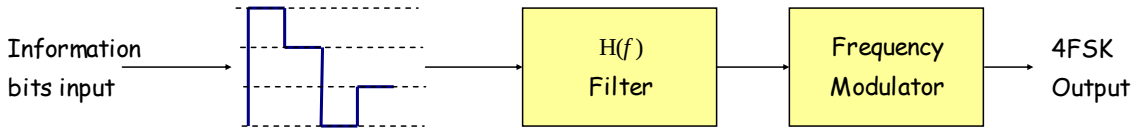


Figure 15 4FSK PRBS Waveform - Spectrum

*Tx Baseband Filter

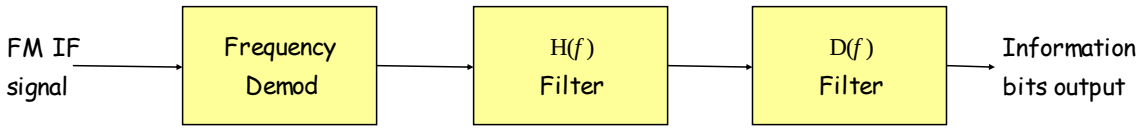


$$|H(f)| = \begin{cases} 1 & , \quad 0 \le |f| < (1-\alpha)/2T \\ \cos[(T/4\alpha)(2\pi|f| - \pi(1-\alpha)/T] & , \quad (1-\alpha)/2T \le |f| < (1+\alpha)/2T \\ 0 & , \quad (1+\alpha)/2T \le |f| \end{cases}$$

$\alpha = 0.2 \quad T = 1/2400$

4 FSK Deviation		
Di-bit	Symbol	Deviation
01_2	+3	+1 050Hz
00_2	+1	+350Hz
10_2	-1	-350Hz
11_2	-3	-1050Hz

*Rx Baseband Filter



$$|H(f)| = \begin{cases} 1 & , \quad 0 \le |f| < (1-\alpha)/2T \\ \cos[(T/4\alpha)(2\pi|f| - \pi(1-\alpha)/T] & , \quad (1-\alpha)/2T \le |f| < (1+\alpha)/2T \\ 0 & , \quad (1+\alpha)/2T \le |f| \end{cases}$$

$$|D(f)| = \frac{\pi f T}{\sin(\pi f T)}$$

$\alpha = 0.2 \quad T = 1/2400$

Figure 16 dPMR Modulation Characteristics

5.7.2 Internal Data Processing

The device operates as a half-duplex device, either receiving signals from the RF circuits in Rx mode, or sourcing signals to the RF circuits in Tx mode. It also has a low power Idle mode to support battery saving protocols. The internal data processing blocks for Tx and Rx modes are illustrated in Figure 17.

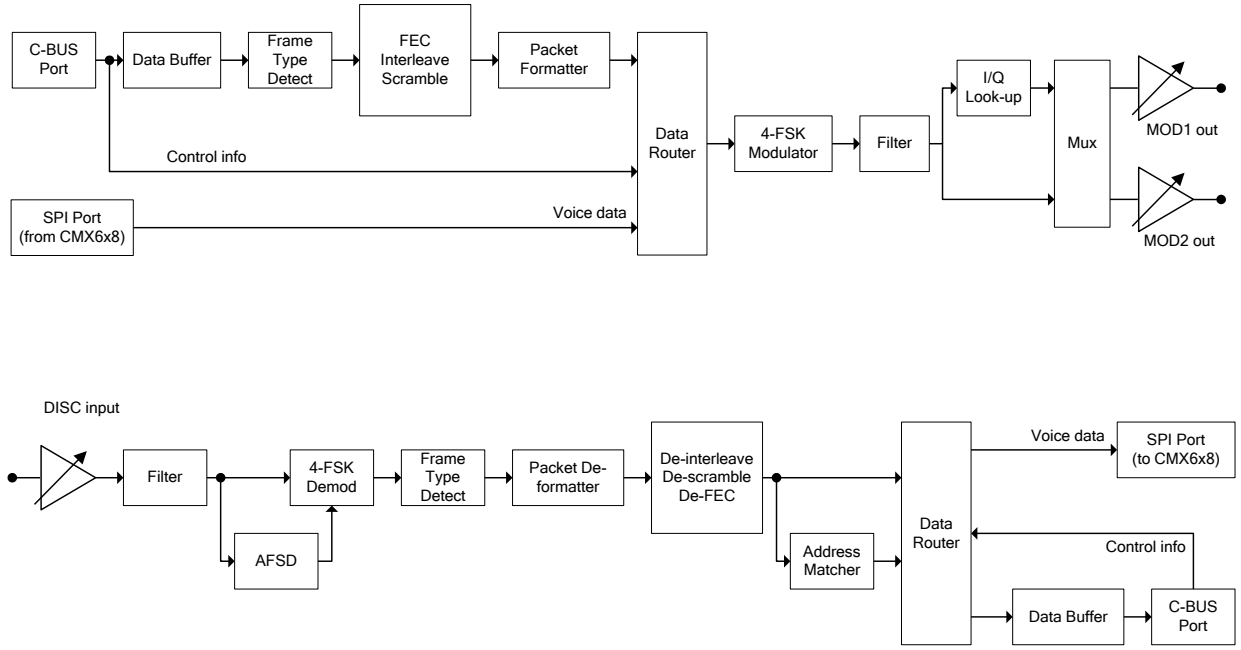


Figure 17 Internal dPMR Data Processing Blocks

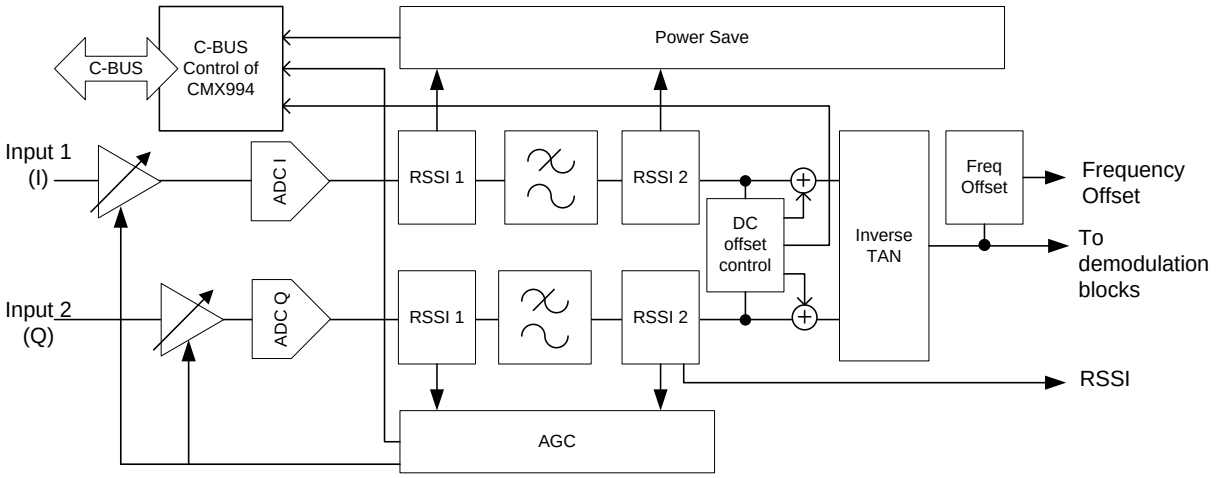


Figure 18 Additional Internal Data Processing in I/Q Mode

5.7.3 Frame Sync Detection and Demodulation

The analogue signal from the receiver may be from either a CMX994 I/Q interface or a limiter/discriminator (LD) output. The signal(s) from the RF section should be applied to the CMX7241/7341 input(s) (normally the DISC input for LD Rx and DISC and ALT inputs for I/Q Rx). The signals can be adjusted to the correct level either by selection of the feedback resistor(s) or using the CMX7241/7341 Input Gain settings. In LD mode the signal is filtered using a Root-Raised Cosine filter and Inverse Rx Sinc filter matching the filters applied in the transmitter, then passed to the AFSD (Automated Frame Sync Detector) block which extracts symbol and frame synchronisation. During this process the 4FSK demodulator and the data-processing sections that follow are dormant to minimise power consumption. When frame synchronisation has been achieved the AFSD section is powered down, and timing and symbol-level information is passed to the 4FSK demodulator which starts decoding the subsequent data bits. The CMX7241/7341 can detect the end of a burst by

scanning the received control channel fields and will automatically disable the demodulator and restart frame sync search when required without host intervention.

In I/Q mode filtering is applied to the input signals and dc offsets are removed before an inverse tan function performs the FM demodulation function. The output of this stage has an offset depending on the frequency error of the received signal compared to the nominal frequency of the receiver. This offset is removed before RRC filtering, after which the signal chain is then the same as the LD case. In I/Q mode the CMX7241/7341 provides measurements of frequency error and RSSI (which are not available in LD mode).

A dPMR burst begins with a 72-bit (or longer) preamble sequence followed by a 80ms Header Frame, which contains a 48-bit frame sync (FS1 or FS4). Payload frames contain either a 24-bit frame sync (FS2) or a 24-bit Colour Code. The CMX7241/7341 can scan for all dPMR frame syncs concurrently. It uses FS1 to detect the start of a transmission, and can optionally use FS2 to perform 'late entry' into an existing burst. The short length of FS2 gives a high probability of false detects, so the CMX7241/7341 only accepts an incoming burst from an FS2 detect if a second FS2 is received at the correct frame spacing. Frame sync detects are reported with an FS Detect IRQ and a code in the 4FSK Modem Status register ($C9).

When frame synchronisation has been achieved, the 4FSK demodulator is enabled, frame sync detection is switched off and subsequent frame sync sequences embedded in the received frames are not reported.
Table 6 and Table 7 show an example of typical call setup sequence in Mode 1 (peer-to-peer or direct mode). Mode 2 (repeater mode) is similar; however different RF frequencies may be used by the Rx and Tx paths. Call set-up in Mode 3 (trunked mode) is more complex as the trunking controller manages the data transactions over the RF channels.
Mode 3 (trunked) operation differs significantly from Modes 1 and 2 by the use of a Control/Signalling channel (the Beacon Channel) which conveys signalling and system information to the terminals using the SYScast frame types. The device includes support for receiving and decoding these additional frame types.

Table 6 dPMR Frame Format - Call set-up, no ACK

Bit no.		24	48	72	96	120	144	168	192	216	240	264	288	312	336	360	384
		press PTT															
Header	Tx	Preamble			FS1		Header Info 0					CC	Header Info 1				
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
	Tx	Repeat frames 1 to 4 until PTT released….															
End	Tx	FS3	End Flag														

Table 7 dPMR Frame Format - Call set-up with ACK

Bit no.		24	48	72	96	120	144	168	192	216	240	264	288	312	336	360	384
		press PTT															
Header	Tx	Preamble			FS1		Header Info 0					CC	Header Info 1				
End	Tx	FS3	End Flag														
Ack	Rx	Preamble			FS1		Header Info 0					CC	Header Info 1				
Header	Tx	Preamble			FS1		Header Info 0					CC	Header Info 1				
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
	Tx	Repeat frames 1 to 4 until PTT released….															
End	Tx	FS3	End Flag														

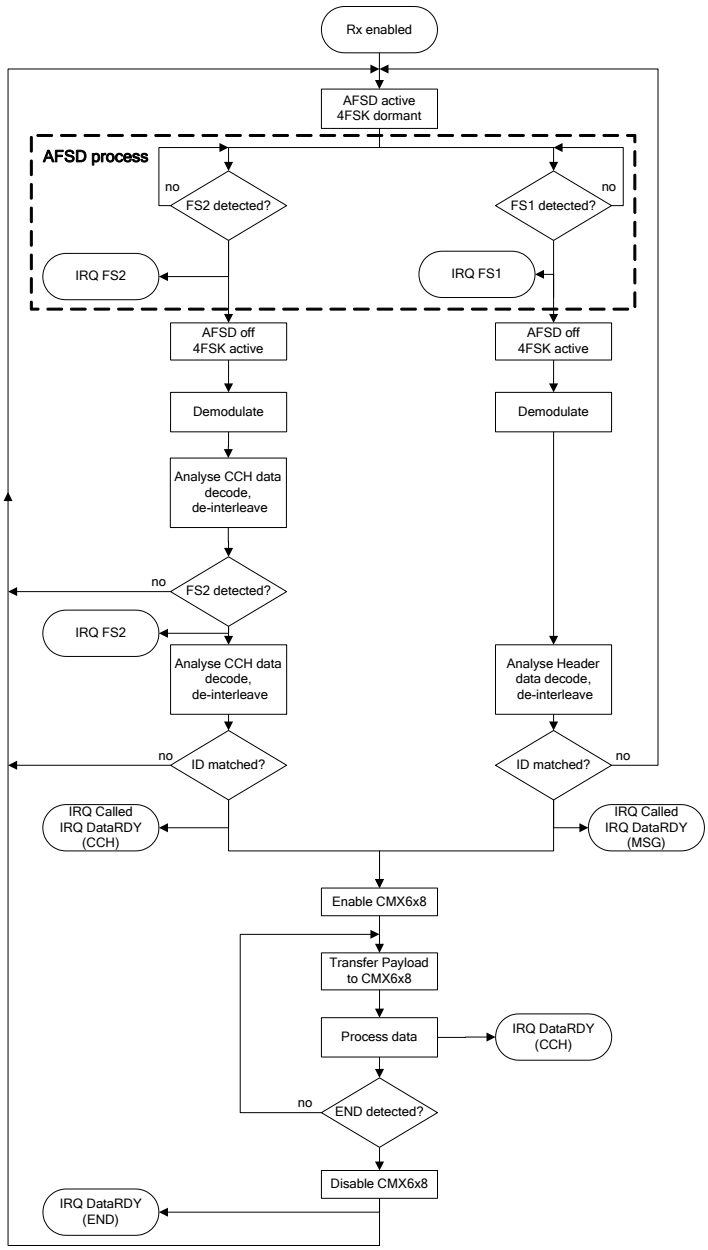


Figure 19 FS Detection

5.7.4 FEC and Coding

The CMX7241/7341 implements all CRCs, Hamming codes, interleaving and scrambling required by the dPMR standard. Any CRC failures in control channel fields or coded data blocks are indicated when transferring the decoded fields or data to the host. This relieves the host of a substantial processing load and has the added advantage of reducing the complexity and timing constraints of interfacing between the host, vocoder and CMX7241/7341.

The dPMR Message Frame format contains duplicate copies of all control channel fields (in the MI0 and MI1 Message Information blocks) but only one MI block is transferred to/from the host. On receiving a Message Frame the CMX7241/7341 decodes both MI blocks, checks both CRCs and can accept the call if either block is valid.

5.7.5 Voice Coding

A CML CMX618/CMX608 RALCWI or CMX7262 TWELP vocoder can be used under the control of the CMX7241/7341. The CMX7241/7341 provides an auxiliary SPI/C-BUS port (which may be shared with CMX994) which is used to issue control commands and transfer voice payload data directly to the vocoder, minimising the loading on the host controller during voice calls.
Alternatively, the CMX7241/7341 can support any third-party vocoder by routing voice payload data over the main C-BUS interface and through the host. In this mode, all vocoder control and data transfers must be managed by the host.
Voice data transferred to the vocoder in Rx mode always uses soft decision (4-bit log-likelihood ratio) format. This option is also available for voice payload data routed to the host, although it increases the required data transfer rate over C-BUS by a factor of four.

5.7.6 Radio Performance Requirements

For optimum performance, the signal should not be significantly degraded by filters that are excessively narrow and/or cause significant group delay distortion. Care should be taken in interfacing the device to the radio circuits to maintain the frequency and phase response (both low and high end), in order to achieve optimum performance. Test modes are provided to assist in both the initial design and production set-up procedures.
Further information and application notes can be found at http://www.cmlmicro.com .

5.8 Audio/Voice Functions

5.8.1 Microphone

A microphone may be directly connected to the MIC input, which is configured as an op amp with the positive input tied to VBIAS. This allows the gain and frequency response to be set by selecting appropriate values of C15, C16 and R9, R10. The device includes a programmable gain stage which can either be set by the host by writing to the Analogue Output Gain register ($B0) or can be left for the device to control as part of the Voice AGC functionality.

5.8.2 Speaker

A speaker amplifier may be connected to the AUDIO output. The signal level on this pin can be controlled using the Analogue Output Gain Register ($B0).

5.8.3 Modulation

Two separate modulation outputs are provided (MOD1, MOD2) with independent level controls to facilitate 2-point modulation systems. Alternatively, the same outputs may be configured to drive an I/Q modulator. In I/Q mode the Analogue FM modulation level is set to 2.5kHz in order to be compatible with 12.5kHz channel operation. I/Q Tx mode is not suitable for 25kHz channel operation.

5.8.4 Audio / Voice processing

All the necessary processing blocks to support analogue FM voice for 12.5 or 2 5kHz channel operation are provided to support ETSI 300 086 and TIA 603 compatible systems. This includes:

- 300 Hz HPF to reject sub-audible signalling
- Pre emphasis and de-emphasis
- Channel filtering for 12.5 or 25kHz channels
- Programmable Limiter (works in concert with the Voice AGC)

In addition, frequency inversion voice scrambler and a voice compander are also provided.
The analogue signal levels must be set so as not to overload the internal processing blocks. In particular, pre-emphasis and de-emphasis processing will boost signals by up to 10dB, depending on their frequency. Threshold levels for the Voice AGC and Tx Limiter functions are host programmable.

5.8.5 Sub-Audio Signalling

A 51-tone CTCSS and 83-code DCS encoder / decoder is provided which meets the requirements of TIA 603. Reverse tone burst and Squelch Tail Elimination are supported.

5.8.6 In-band Signalling

- A fully flexible Selcall Tone encoder/decoder with host programmable tones is provided. By default the CCIR tone set is enabled.
- A 1200/2400 bps FFSK modem that meets the requirements of MPT1327 is available. This provides simultaneous detection of up to four different sync sequences, all of which are host programmable..
- A standard DTMF generator/decoder is provided
- A general purpose audio tone generator is also available for generating “ring-tones”, confidence tones or key beeps etc.

Note that enabling more than one in-band signalling format simultaneously may lead to false detects on any one of them, and increase power consumption.

6 Detailed Descriptions

6.1 Xtal Frequency

The CMX7241/7341 is designed to work with an external frequency source of 19.2 MHz. For other values, contact CML Customer support.

Table 8 Xtal/Clock Frequency Settings for Program Block 3

Program Register			External Frequency Source (MHz)							
										19.2
P3.14	Idle	GP timer								**$0018**
P3.15		VCO output and AUX clk divide								**$0099**
P3.16	Rx or Tx	MainCLK Init								**$4F51**
P3.17		MainCLK Lock Time								**$0267**
P3.18		MainCLK0								**$43B1**
P3.19		MainCLK1								**$0019**
P3.20		MainCLK2								**$0040**
P3.21		VCO output and AUX clk divide								**$0140**
P3.22		Internal ADC/DAC clk divide								**$0008**

6.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7241/7341 and the host µC; this interface is compatible with microwire and SPI. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 6.6.2.

The CMX7241/7341 will monitor the state of the C-BUS registers that the host has written-to every 250 µs (the C-BUS latency period) hence it is not advisable for the host to make successive writes to the same C-BUS register within this period.

6.2.1 C-BUS Operation

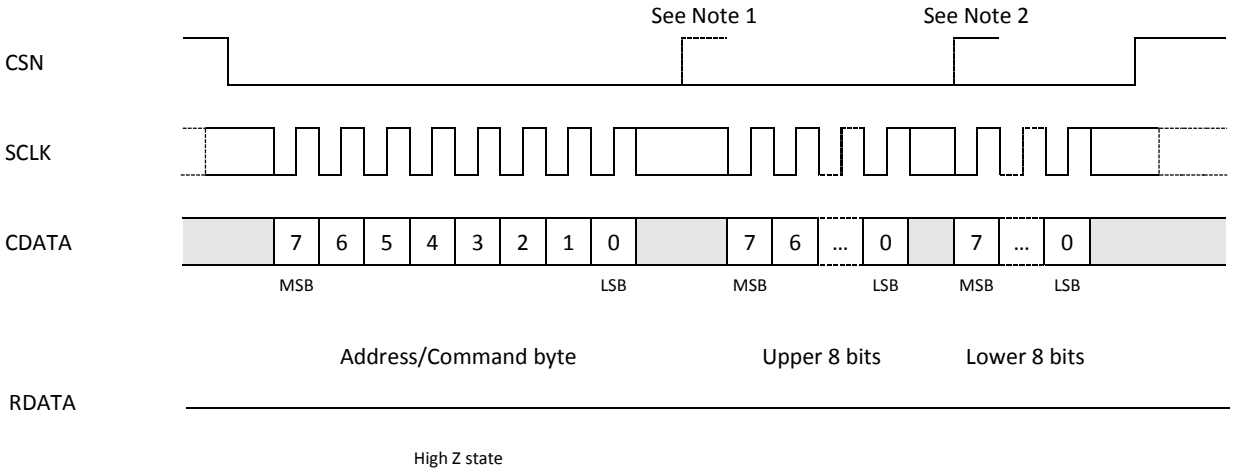
This block provides for the transfer of data and control or status information between the CMX7241/7341's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single address byte sent from the µC which may be followed by one or more data byte(s) sent from the µC to be written into one of the CMX7241/7341's Write Only Registers, or one or more data byte(s) read out from one of the CMX7241/7341's Read Only Registers, as shown in Figure 20.

Data sent from the µC on the CDATA (Command Data) line is clocked into the CMX7241/7341 on the rising edge of the SCLK (Serial Clock) input. RDATA (Reply Data) sent from the CMX7241/7341 to the µC is valid

when the SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an address byte is dependent on the value of the Address byte. The most significant bit of the address or data is sent first. For detailed timings see section 7.2. Note that, due to internal timing constraints, there may be a delay of up to 250 µs between the end of a C-BUS write operation and the device reading the data from its internal register.

C-BUS Write:



C-BUS Read:

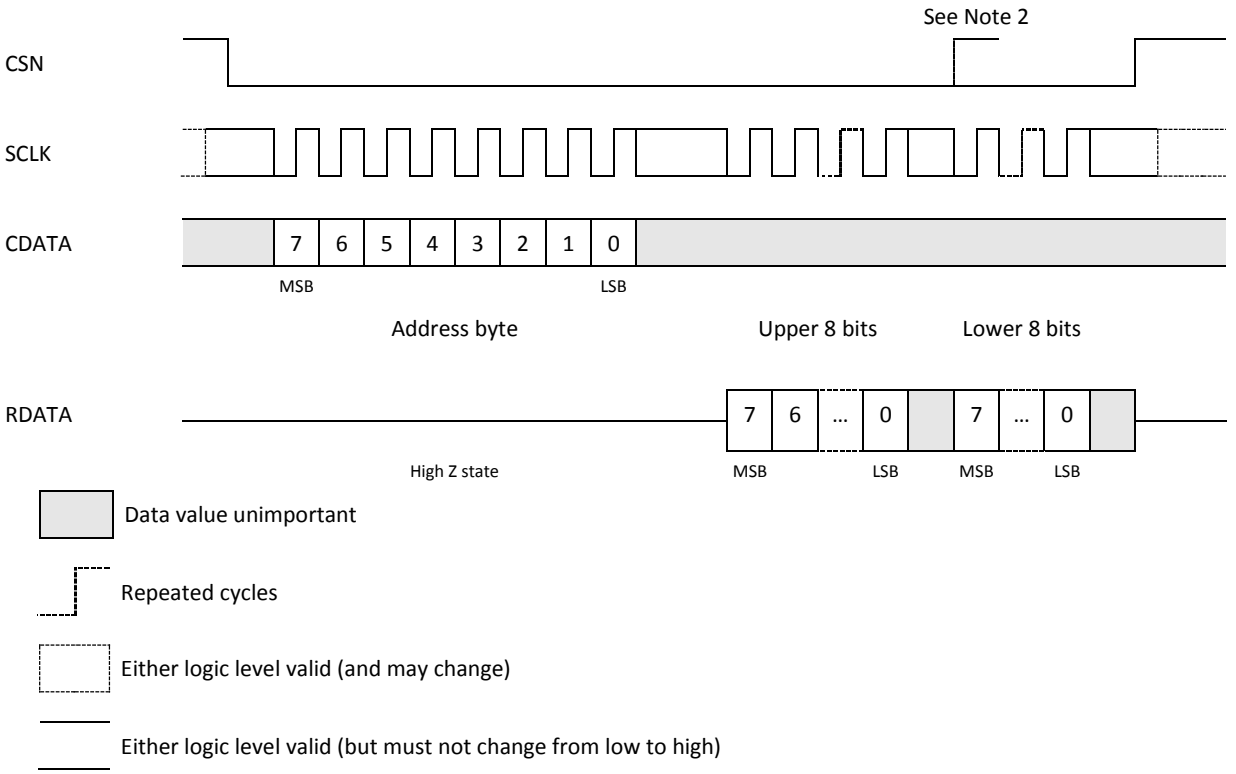


Figure 20 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

6.3 Function Image™ Loading

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which can be included into the host controller software. The maximum possible size of Function ImageTM is 96 kbytes, although a typical FI will be less than this. Note that the BOOTEN pins are only read at power-on or following a C-BUS General Reset or a reset via the RESET pin and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN pins are ignored by the CMX7241/7341 until the next power-up or C-BUS General Reset.

The BOOTEN pins are both fitted with internal low current pull-down devices.

For C-BUS load operation, both pins should be pulled high by connecting them to DVDD either directly or via a 220k resistor (see Figure 21).

Once the FI has been loaded, the CMX7241/7341 will report the following information:

- $C5 = Product Ident Code ($7241 or $7341)
- $C9 = FI version code (1xxx)
- $A9, $AA = Block 2 Checksum
- $B8, $B9 = Block 1 Checksum

The host should verify the checksum values with those published with the Function Image file downloaded from the CML Technical Portal.

The device waits for the host to load the 32-bit Device Activation Code through C-BUS register $C8. Once activated, the device initialises fully, enters idle mode and becomes ready for use, and the Programming flag (bit 0 of the Status register) will be set.

Once the FI has been activated, the checksum, product identification and version code registers are cleared and these values are no longer available. If an invalid activation code is loaded, the device will report the value $DEAD in register $A9 and must be reset via the dedicated RESET pin (if used) or power-cycled before an attempt is made to re-load the FI and re-activate.

Both the Device Activation Code and the checksum values are available from the CML Technical Portal.

Table 9 BOOTEN Pin States

	BOOTEN2	BOOTEN1	Notes:
C-BUS Host load	1	1	FIFO mode (or single word mode)
Multi-Serial Memory load	1	0	Flexible address mode
Serial Memory load	0	1	Compatible with CMX7141
No FI load	0	0	

Note: Following a reset, the contents of the device should be verified using the CRC check facility, and re-loaded if required.

6.3.1 FI Loading from Host Controller

The Function Image™ can be included with the host controller software for download into the CMX7241/7341 at power-up over the C-BUS interface. This is done by writing the FI data into the Tx FIFO Data register ($79) which supports streaming operation. The BOOTEN1/2 pins must first be set to the C-BUS load configuration and the device then powered up or Reset before the FI data is sent over C-BUS.

When using the recommended 19.2 MHz clock source for XTALIN, the device can accommodate the host continuously streaming data to the Tx FIFO at the maximum SCLK rate of 10 MHz, therefore it is not necessary to monitor the FIFO level registers during this operation. FI download time is limited only by the clock frequency of the C-BUS. With a 10 MHz SCLK it should take less than 250 ms to complete even when loading the largest possible Function Image™.

The CMX7241/7341 memory can be protected against brownout or other forms of corruption. This protection is applied automatically in the 7241/7341 FIs, however when using legacy 7131/7141 FIs, this should be applied during the process of FI loading. To apply protection, the host must write the value $007F to C-BUS register $A0 after the last data block is loaded and before sending the activation block which ends the loading of the FI.

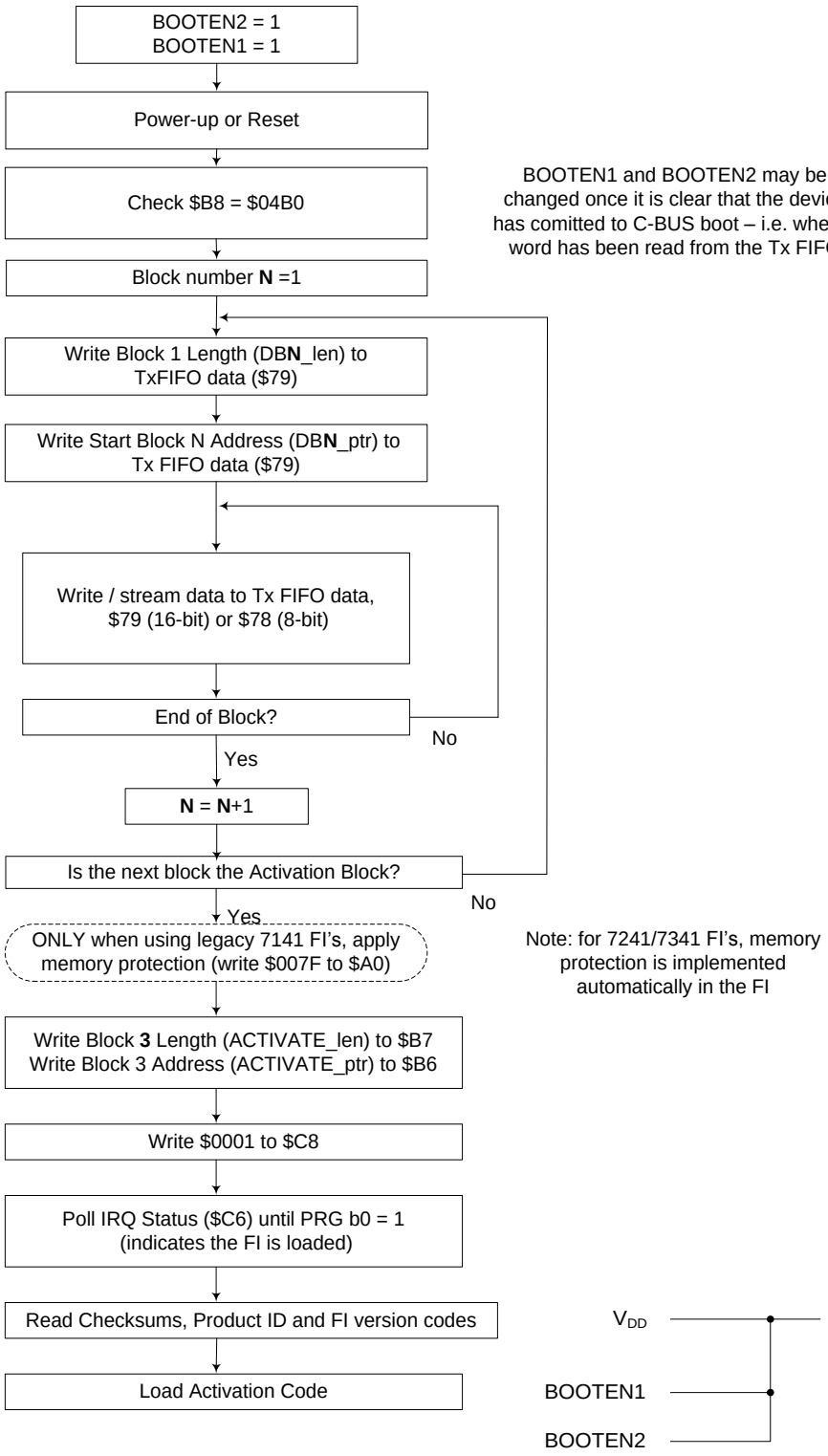


Figure 21 FI Loading from Host

If the main clock frequency (at the XTALIN pin) is slower than the C-BUS clock then the host will need to manually increase the internal MainCLK speed (contact CML Customer Support for details). The device does not take any action until BOTH length and address have been written to the FIFO, so writing the length and then polling for 'FIFO level = 0' will NOT work.

Support for the legacy mode, as used in the CMX7141 and CMX7041 series, is provided, but not recommended. Contact CML Customer Support for details.
Block 3 (Activate) may also be loaded using the Tx FIFO mechanism. However, in this case, the PRG flag will not be set when the operation has completed, so the host must implement a fixed delay or poll the $C5 register until the Device Ident Code appears, before the checksum values can be read.

6.3.2 FI Loading from Host with CMX7262

When using the CMX7262 under direct control of the device, it is necessary to also load the CMX7262 with its own FI. This can be accomplished by providing the CMX7262 with its own serial flash storage locally (see the CMX7262 Datasheet for details), or over the host C-BUS connection after completing the initial device FI load by making use of an additional download mode (note that this is not possible if the Auxiliary Serial Port is in the “split” / “alternate” mode – see Section 4.4). This is enabled by changing the Block 3 ACTIVATE_ptr from $4010 to $400E. In this mode any further data blocks received are transferred through the device to the connected CMX7262.

Following the download of the modified activation block pointer the boot checksums may be verified to confirm that the CMX7241/7341 Function Image™ was correctly transferred. Following this, the next blocks may be transferred across the C-BUS interface in a similar manner – these will be the sections from the CMX7262 Function Image™. Upon receiving the 2nd Activation Pointer (that of the CMX7262) the boot checksums will be available to be read. They will be read from the CMX7241/7341 registers $AA:$A9 and $B9:$B8 but will be the checksums of the CMX7262 Function Image™ blocks which were transferred.
Upon successful read-back of the checksums the host may proceed to load the CMX7241/7341 activation codes. Alternatively, a combined Function Image maybe supplied as a single .h file suitably pre-formatted for download – contact CML Application Support for details.

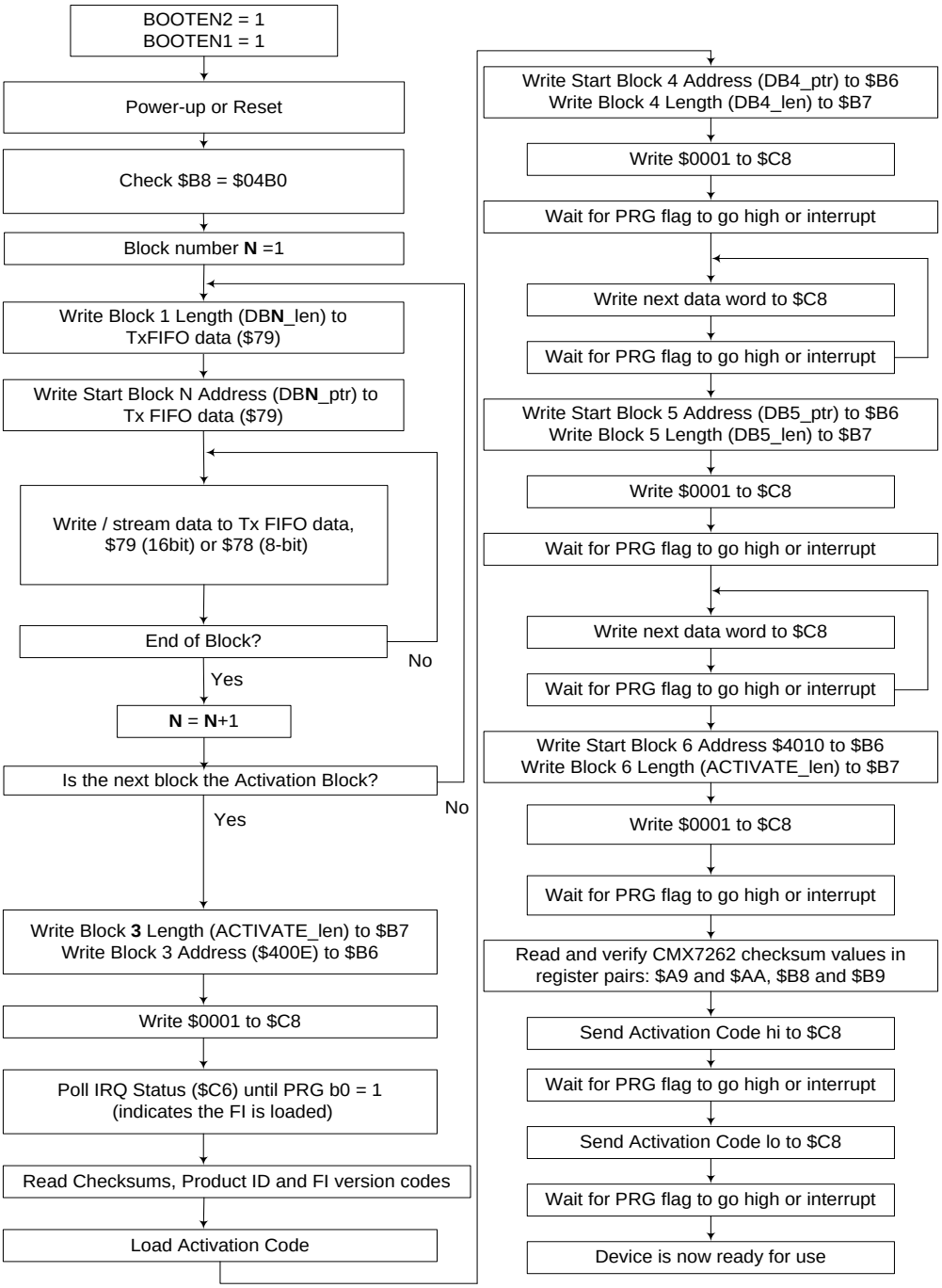


Figure 22 FI Loading (including CMX7262)

Blocks 1, 2 and 3 are provided from the 7241/7341FI-1.x file, but with Block 3 ACTIVATION_ptr set to $400E.
Blocks 4, 5 and 6 are provided from the 7262FI-1.x file with the Block 6 ACTIVATION_ptr set to $4010.

6.4 Direct Vocoder Control Interface

An auxiliary SPI/C-BUS interface is provided which allows the CMX6x8 or CMX7262 to be directly controlled by the CMX7241/7341 without the need for the host to intervene. This is accomplished by using an additional Chip Select pin (SSOUT).. The CMX7241/7341 Auxiliary SPI/C-BUS interface bus should be connected to the C-BUS interface on the vocoder using the SSOUT pin as the CSN signal for the CMX6x8/CMX7262 running in C-BUS mode. Selection of the auxiliary SPI/C-BUS port mode is made using Program register P2.0:b3-0.The initialisation and operational settings of the CMX6x8/CMX7262 should be programmed by the host into the CMX7241/7341 Program Block 1 on power-up. These values will be written to the defined registers in the Vocoder at:

- Initialisation
- Idle mode
- Rx mode
- Tx mode.

Mic Gain and Speaker Gain commands may be sent to the Vocoder whenever the CMX7241/7341 is in Rx or Tx mode. The DTX and VAD modes of the CMX6x8 are not supported in 7241/7341FI-1.x. DTMF Mode 1 (transparent) is supported. The default settings for the CMX6x8 are:

- 4-frame packet (80 ms) with FEC no STD, no DTMF
- 2.4k bps with FEC
- Internal sync
- Throttle = 1
- Internal codec
- IRQ disabled
- Soft-coded data bits.

The connections for the CMX6x8 Vocoder are shown Table 10. The alternate pin arrangement is enabled by setting P6.1:b15

Table 10 CMX6x8/CMX7262 Vocoder Connections

CMX7241 (P6.1:15 = 0)	CMX7241/7341 alt (P6.1:15 = 1)	CMX6x8/CMX7262 pin
SSOUT	SSOUT	CSN
EPSI	GPIOA	CDATA
EPSO	EPSO	RDATA
EPSCLK	GPIOB	CLK
No connection	No connection	IRQN (tied to V_{DD} via 100kΩ resistor).

Figure 23 shows one possible implementation of the CMX7241/7341 combined with a CMX618, a host microcontroller and suitable RF sections to provide a digital PMR radio. The bold lines show the active signal paths in Rx and Tx respectively.

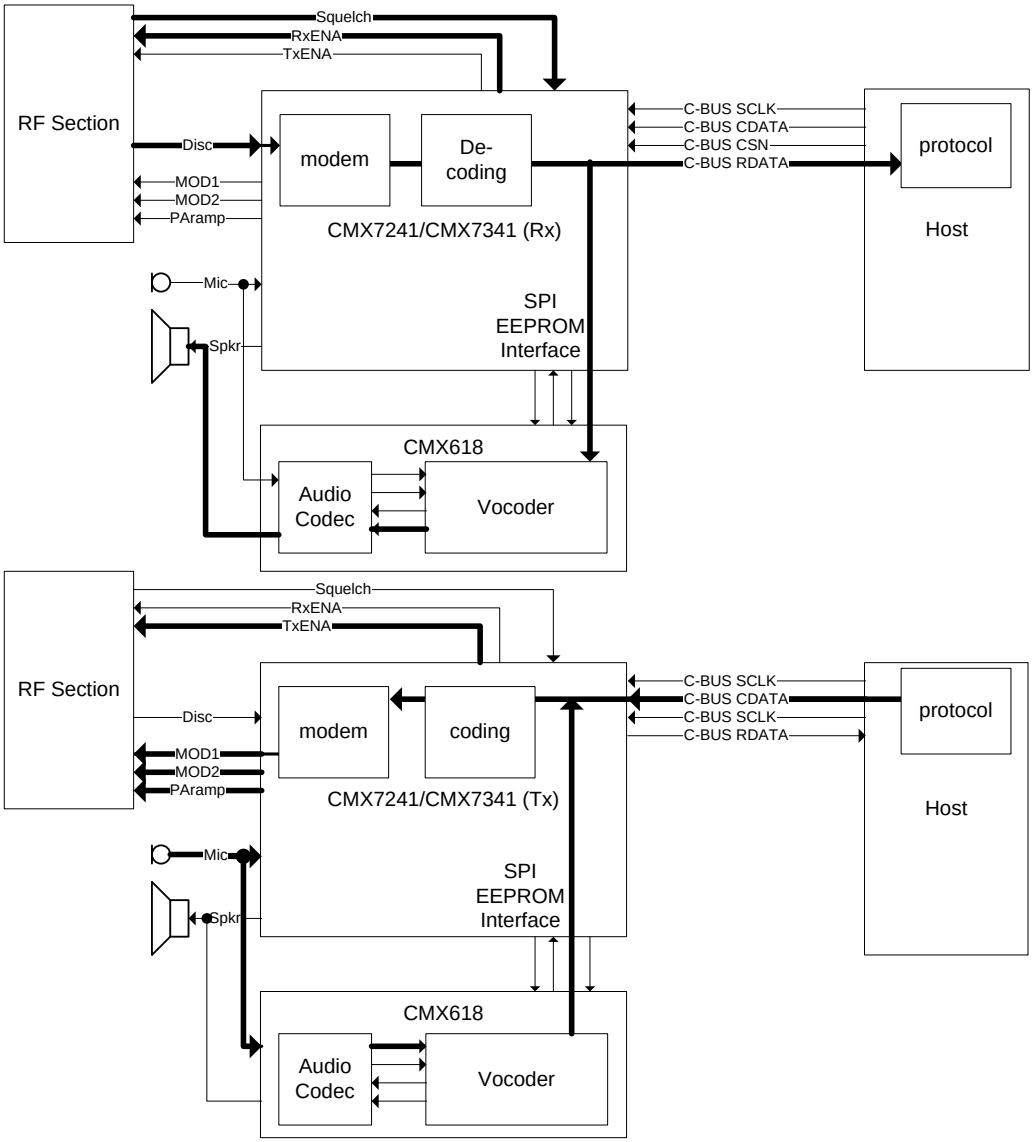


Figure 23 Digital Voice Rx and Tx Blocks

The paralleling of the microphone and speaker connections between the CMX618 and the CMX7241/7341 is only required if the CMX7241/7341 is also to provide analogue PMR functionality. Otherwise, the microphone and speaker should be connected to the CMX618 only. The CMX618 RALCWI Vocoder provides an on-chip audio and voice codec, but alternatively a CMX608 device could be used along with an external audio codec. Voice payload data is transferred directly from and to the CMX618 by the CMX7241/7341. Note that the CMX618 Audio output does not have a high impedance mode, therefore an external analogue switch is required to isolate it when the CMX7421/CMX7341 AUDIO output is in use.

6.5 External Codec Support

6.5.1 DVSI Vocoder Interface

If the DVSI vocoder (or other third-party vocoder) is used all radio channel data will need to be transferred over the main C-BUS through the host. In this case the Vocoder Enable Program registers (P6.1) must be set appropriately to respond correctly to the incoming data fields and the SPI-Codec ENA bit ($A0 bit 0) should be set to 1.

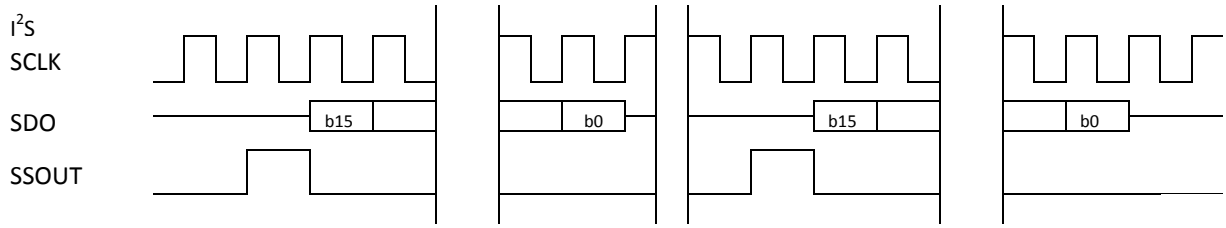
The connections for the AMBE3000 vocoder from DVSI to enable it to use the CMX7241/7341 as the PCM audio codec are shown in Table 11. The alternate configuration is enabled by setting P6.1:b15

Table 11 DVSI Vocoder Connections

CMX7241 (P6.1:b15 = 0)	CMX7341 (P6.1:b15 = 1)	AMBE3000 pin
SSOUT	SSOUT	SPI_STE
EPSI	GPIOA	SPI_RX_DATA
EPSO	EPSO	SPI_TX_DATA
EPSCLK	GPIOB	SPI_CLK and SPI_CLK_IN.

6.5.2 Support for I^2S Mode

The device can support I2S interfaces in mono, 16-bit mode only, for transmitting and receiving audio codec data using the SPI bus. This mode is selected in the programming register (see Section 8.3.7). The diagram below shows typical transmit waveforms.



6.6 Device Control

The CMX7241/7341 can be set into the relevant mode to suit its environment. These modes are described in the following sections and are programmed over the C-BUS: either directly to operational registers or, for parameters that are not likely to change during operation, via the Programming register ($C8).

For basic operation:

(1) Enable the relevant hardware sections via the Power Down Control register

(2) Set the appropriate mode registers to the desired state

(3) Select the required signal routing and gain

(4) Use the Mode Control register to place the device into Rx or Tx mode.

To conserve power when the device is not actively processing a signal, place the device into Idle mode. This will also command the CMX6x8 to enter powersaving mode as well. Additional powersaving can be achieved by disabling any unused hardware blocks, however, care must be taken not to disturb any sections that are automatically controlled. Note that the BIAS block must be enabled to allow any of the Input or output blocks to function.

See:

- Power Down Control - $C0 write
- Mode Control - $C1 write
- 4FSK Modem Configuration - $A1 write

6.6.1 General Notes

In normal operation, the most significant registers, in addition to the TxData and RxData blocks, are:

- Mode Control - $C1 write
- IRQ Status - $C6 read
- Analogue Output Gain - $B0 write
- Input Gain and Signal Routing - $B1 write
- Aux Data and Analogue Mode - $C2 write
- Analogue Control - $C3 write.

Setting the Mode register to either Rx or Tx will automatically increase the internal clock speed to its operational speed and bring the CMX6x8 out of its powersave mode. Setting the Mode register to Idle will automatically return the internal clock to a lower (powersaving) speed. To access the Program Blocks (through the Programming register, $C8) the device MUST be in Idle mode.

Under normal circumstances the CMX7241/7341 manages the Main Clock Control automatically, using the default values loaded in Program Block 3.

6.6.2 Interrupt Operation

The CMX7241/7341 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the IRQ Status register and the IRQ Mask bit (bit 15) are both set to 1. The IRQ bit is set when the state of the interrupt flag bits in the IRQ Status register change from 0 to 1 and the corresponding mask bit(s) in the Interrupt Mask register is(are) set. Enabling an interrupt by setting a mask bit (0→1) after the corresponding IRQ Status register bit has already been set to 1 will also cause the IRQ bit to be set.

All interrupt flag bits in the IRQ Status register, except the Programming Flag (bit 0), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the IRQ Status register. The Programming Flag bit is set to 1 only when it is permissible to write a new word to the Programming register.
See:

- IRQ Status - $C6 read
- Interrupt Mask - $CE write.

Continuous polling of the Status register ($C6) is not recommended due to both the increase in response time, host loading and potential digital noise generation due to bus activity. If the host cannot support a fully IRQ driven interface then it should route the IRQ signal to a host I/O pin and poll this pin instead.

6.6.3 Signal Routing

The CMX7241/7341 offers a flexible routing architecture, with three signal inputs, a choice of two modulator configurations (to suit two-point modulation or I/Q schemes) and a single audio output.
See:

- Input Gain and Signal Routing - $B1 write
- Mode Control - $C1 write

The analogue gain/attenuation of each input and output can be set individually, with additional Fine Attenuation control available via the Programming registers in the CMX7241/7341. The Mic. and Speaker gains are set by the CMX6x8, which is controlled through the Analogue Control - $C3 write of the CMX7241/7341.

See:

- Analogue Output Gain - $B0 write (MOD1 and 2)
- Input Gain and Signal Routing - $B1 write (DISC input, MOD1 and 2)
- Analogue Control - $C3 write (CMX6x8/CMX7262 Mic. and Speaker).

In common with other FIs developed for the CMX7241/7341, this device is equipped with two signal processing paths. Input 1 should be routed to any of the three input sources (ALT, DISC or MIC) which should be connected to the radio's discriminator output. The internal signals Output 1 and Output 2 are used to provide either two-point or I/Q signals and should be routed to the MOD1 and MOD2 pins as required

In dPMR Formatted modes the microphone and speaker paths are automatically re-routed to the Vocoder when appropriate. This routing is controlled by the data field in the Header Block which indicates whether the payload is speech data, and the Vocoder Disable bit in the 4FSK Modem Configuration register, $A1.

6.6.4 Mode Control

The CMX7241/7341 operates in one of these operational modes:

- Idle
- Rx
- Tx
- Rx with CMX994 I/Q Cal.
- Rx with CMX994 Powersave

At power-on or following a Reset, the device will automatically enter Idle mode, which allows maximum powersaving whilst still retaining the capability of monitoring the AuxADC inputs (if enabled). It is only possible to write to the Programming register whilst in Idle mode.

See:

- Mode Control - $C1 write.

GPIO1 and GPIO2 pins (RXENA and TXENA) reflect bits 0 and 1 of the Mode Control register, as shown in Table 12. These can be used to drive external hardware without the host having to intervene. There are also two additional GPIO pins that are programmable under host control.

Table 12 Device Mode Selection

Mode Control ($C1) b3-0	Modem Mode	R20,R21connected to DVdd		R20,R21connected to DVss	
		TXENA	RXENA	TXENA	RXENA
0000	Idle – Low Power Mode	1	1	0	0
0001	Rx	1	0	0	1
0010	Tx	0	1	1	0
0011	*reserved*	x	x	x	x
0100	*reserved*	1	1	0	0
0101	Rx with CMX994 I/Q Cal.(I/Q mode only)	1	0	0	1
1001	Rx with Powersave (I/Q mode only)	1	0	1	0
others	*reserved*	x	x	x	x

Table 13 dPMR Modem Control Selection

Mode Control ($C1) b7-4	Rx	Tx
0000	Rx Idle	Tx Idle
0001	Rx dPMR Formatted	Tx dPMR Formatted
0010	Rx Raw	*reserved*
0011	Rx 4FSK EYE	Tx 4FSK PRBS
0100	Rx Pass-through Mode	Tx 4FSK Preamble
0101	*reserved*	Tx 4FSK Mod Set-up
0110	Sync	Test
0111	Reset/Abort	Reset/Abort
1xxx	*reserved*	*reserved*

Table 14 Analogue Mode Selection

b15	b14	b13	b12	b11	b10	b9	b8
Voice	Tone	Sub-Audio	*res*	Scrambler	Selcall	DTMF	FFSK

In Rx, both analogue and Digital modes maybe selected at the same time, however, to achieve best performance and power consumption, once an activity in a particular mode has been detected (as indicated by the IRQ, Digital and Analogue status registers, $C6, $C9, $9B, and $CC), the others should be disabled.

In Tx, only one mode should be selected at any one time, with the exception of Sub-Audio, which may be enabled in conjunction with any other analogue mode.
The Modem Mode bits and the Mode Control bits should be set together in the same C-BUS write.

6.6.5 Tx Mode dPMR

In Tx dPMR mode operation ($C1, Mode Control = $0012), the host should write the initial Message Info data block to the C-BUS TxData registers and set the Modem Mode to dPMR Formatted and the Control bits to Tx. The preamble and frame sync are transmitted automatically followed by the coded Message frame contents. As soon as the Message Info data block has been read from the C-BUS TxData registers, the 'Data Ready' IRQ is asserted and the next block of control channel or payload data may be loaded. If the Message Info fields indicate that the burst is a voice call, and use of the CMX6x8/CMX7262 vocoder has been enabled, encoded voice data will be taken from it directly for transmission over-air.
At the end of the burst after the last bit has left the modulator a 'Tx Done' IRQ will be issued. At this point it is now safe for the host to change the Mode Control and Modem Mode to Idle ($C1, Mode Control = $0000) and turn the RF transmitter off.

6.6.6 Tx Mode PRBS

In PRBS mode ($C1, Mode Control = $0032) the preamble and frame sync are transmitted automatically followed by a PRBS pattern conforming to ITU-T O.153 (para. 2.1) giving a 511-bit repeating sequence.

6.6.7 Tx Mode Preamble

In Preamble mode ($C1, Mode Control = $0042) the preamble sequence [+3 +3 -3 -3] is sent continually. This can be used to set up and adjust the RF hardware.

6.6.8 Tx Mode Mod Set-up

In Mod Set-up mode ($C1 = $0052) the output depends on the selected Tx modulation type. In two-point mode, a repeating sequence of eight +3 symbols followed by eight -3 symbols is sent, and in I/Q mode a continuous sequence of +3 symbols is sent. This can be used to set up and adjust the RF hardware.

6.6.9 Tx Mode Test

In Test mode, simple test waveforms are generated (defined by the dPMR Association TWG). See section 8.1.22.

6.6.10 Tx Sequencer

The Tx Sequencer provides an automated way of executing a sequence of actions, thus reducing timing constraints placed on the host. It is controlled by setting b15 in the 4FSK Modem Configuration register ($A1) to 1. If enabled, it will automatically start executing its sequence of transmit actions when the CMX7241/7341 is placed in Tx mode. The timing values for each action can be set in P3.0 to P3.12 and are defined in increments of 250µs. The RAMDAC will ramp (up and down) over a period defined by the configuration in P3.13 (RAMDAC scan time configuration).

For digital Tx modes the CMX7241/7341 will be prevented from modulating data until the Modulation Start Delay has elapsed. For analogue Tx modes the signal will initially be muted for this period, at which point any buffered FFSK data will begin to modulate. Tone generation will not be possible during this start delay time therefore tone generation commands should be delayed until the Modulation Start Delay timer has expired. Expiry of the timer is indicated by the raising of the Sequencer Event IRQ ($C6:b2) and setting of the Sequencer Start event flag (b10) of the 4FSK Modem Status register ($C9).

The Tx Sequencer may also directly take control of the GPIOA and GPIOB signals if required – setting them high for the duration of the active mode. This is enabled by selecting the appropriate bit in P6.0:b13,12. The delay timers for controlling each GPIO signal transition are set individually.

In digital Tx modes the sequencer ends automatically with the detection of the end of data burst within the payload block. While in analogue Tx mode FFSK data will also automatically end the sequencer following detection of the last data to be transmitted. The Tx Sequencer can also be forced to execute the “end” actions by writing Tx Sequencer Release ($B000) to AuxFunction Control ($A8). This can be used to end the sequence when analogue Tx modes are used (without FFSK, for instance).

Following completion of the last sequencer action (TXENA inactive) the Sequencer Event IRQ is asserted with the Sequencer End event flag (b11) being set in the 4FSK Modem Status register ($C9) and the device is automatically returned to its previous mode.

It is important that the RAMDAC ramp down completes by the end of the sequencer event. This can be confirmed by also verifying that the Ramp flag (b12) of $C9 – 4FSK Modem Status is clear when the Sequencer (End) event IRQ is raised. This can be accomplished by either increasing the Tx ENA inactive delay timer or decreasing the RAMDAC scan time.

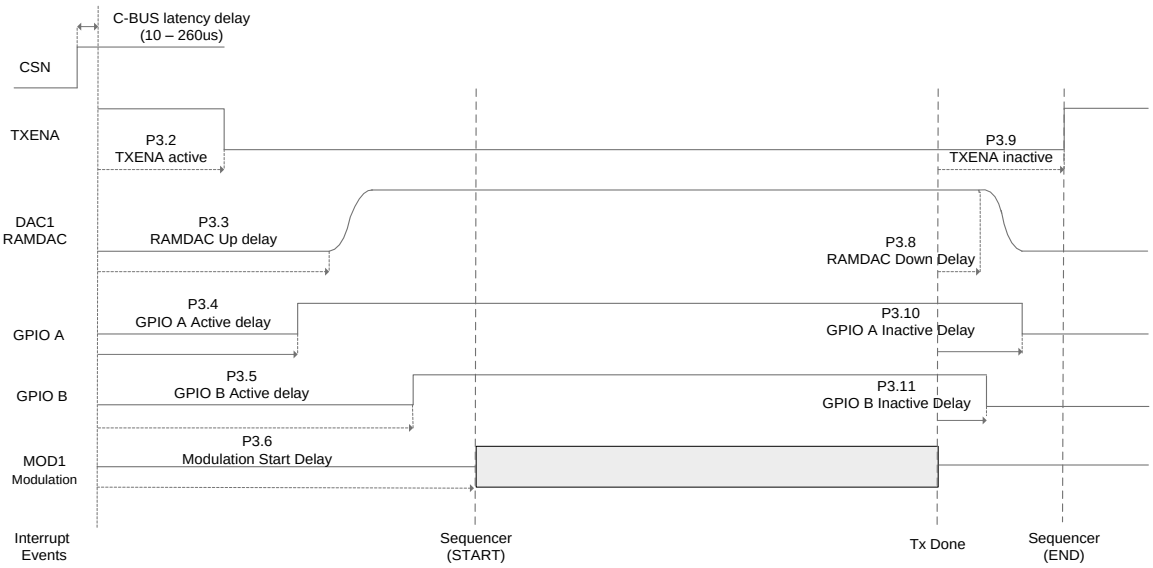


Figure 24 Tx Sequencer Delay Timers

6.6.11 Rx Mode dPMR

In Rx dPMR mode operation ($C1, Mode Control = $0011), the CMX7241/7341 will automatically start searching for frame synchronisation. When a valid frame sync sequence is detected, an 'FS detect' IRQ is asserted and the data demodulator is enabled. If the burst is then accepted a 'Called' IRQ is asserted and the first Message Info or CCH Info block is loaded into the C-BUS RxData registers with a 'Data Ready' IRQ. If the control channel fields indicate that the burst is a voice call, and use of the CMX6x8 vocoder has been enabled, received payload data will be sent to it directly for decoding. Otherwise payload data is loaded into the C-BUS RxData registers with a 'Data Ready' IRQ to indicate when each new block is available. If 'soft' data mode has been selected, the payload data is encoded in 4-bit log-likelihood-ratio format and the host must be able to service the 'Data Ready' IRQs and RxData registers at four times the normal rate to avoid overflow.

6.6.12 Rx Mode Raw

Rx Mode Raw is included in this FI to facilitate BER measurements. In this mode ($C1, Mode Control = $0021), once a valid Frame Sync has been detected, all following data received is loaded directly into the C-BUS RxData registers. This continues until the host exits Rx Raw mode, even if there is no valid signal at the input. On exiting Rx Mode Raw, there may be a DataRdy IRQ pending which should be cleared by the host. Note that Raw Mode operation always requires the incoming data to be preceded with a valid Preamble and Frame Sync pattern in order to derive timing information for the demodulator. The device will update the C-BUS RxData registers with Rx payload data as it becomes available. The host MUST respond to the DataRDY IRQ before the RxData registers are over-written by subsequent data from the modem.

6.6.13 Rx Mode Eye

In Rx 4FSK EYE mode ($C1 = $0031), the filtered received signal is output at the MOD1 pin as an 'eye' diagram for test and alignment purposes. A trigger pulse is output at the MOD2 pin to allow viewing on a suitable oscilloscope. The trigger pulse is generated directly from the receiver xtal source, not from the input signal.

6.6.14 Rx Pass-through Mode

Rx Pass-through mode ($C1 = $0041) is very similar to Rx Mode Eye as described in section 6.6.13. However the output at the MOD1 pin is the flat, unfiltered signal. A trigger pulse is output at the MOD2 pin to allow viewing on a suitable oscilloscope. The trigger pulse is generated directly from the receiver xtal source, not from the input signal.

Table 15 Frequency Response for Rx Pass-through Mode

300Hz	-0.6dB
1kHz	0dB (reference)
2kHz	-0.7dB
2.5kHz	-1.4dB
3kHz	-2.4dB
4kHz	-4.9dB
6kHz	-12.2dB

6.6.15 Rx Mode with CMX994 AGC (I/Q Mode only)

By default, when receiving in I/Q Mode the device will control its internal analogue gain and the gain of the CMX994 in order to keep the received I/Q signals within an acceptable dynamic range. This AGC feature may be disabled using Program Block P6.0 (I/Q AGC function), in which case any setup that the host has made of the CMX994 will determine its gain, with the input gain of the device being controlled using the Input Gain and Signal Routing - $B1 write register.
It is important to ensure that the dc offset on the I/Q signals is small, otherwise the AGC function will interpret the dc as a large received signal and never select maximum gain. This problem can be addressed by calibrating the CMX994 as described in Section 6.6.16.

6.6.16 Rx Mode with CMX994 I/Q Cal (I/Q Mode only)

When receiving, the device will estimate and remove the dc error present in the I/Q signals from a CMX994 receiver. However, it is necessary to calibrate the CMX994 so that the magnitude of the dc offsets present is as small as possible. Selecting Rx mode with CMX994 I/Q Cal ($C1, Mode Control b3-0 = $5) causes the device to measure the dc offset on the DISC and ALT input pins and to control the CMX994 receiver to minimise the dc offsets. The device will then begin to receive normally – correcting the remaining dc offset internally.

Important note: when calibrating I/Q it is important that the I/Q signals are not swapped when interfacing to the CMX994. This can be corrected by using bits 2 to 5 of the Input Gain and Routing register ($B1).

If the CMX994 is poorly calibrated, a loss of headroom when receiving signals will result. In extreme cases, when large dc offsets are amplified, the result can be big enough to prevent the AGC from reaching maximum gain as it interprets the dc offset itself as a large signal.

Selection of some CMX994 options such as low power, or phase correction in the case of a CMX994A/CMX994E, can change the I/Q dc position. For this reason the calibration should be executed with the desired CMX994 configuration already applied.

Having calibrated the CMX994, the value written to the CMX994 dc offset correction register is available to read using the Aux Data and Status ($A9, $AA) registers. This means that having calibrated the CMX994 on a receive channel the calibration result may be stored by the host microcontroller and restored at a later time.

The format of the DC offset correction register read back value differs slightly between a CMX994 and a CMX994A/CMX994E. When a CMX994A/CMX994E is connected (and configured as such) the calibration will be performed using the Extended Rx Offset Register ($17). This is a 16-bit register with a greater range of offset values than available in the CMX994. Because the Aux ADC Data and Status registers ($A9 and $AA)

only provide 12 available bits the field is compressed when read back during this mechanism. If the host microcontroller wishes to write the values to the CMX994A/CMX994E (via 994 pass-through mode) it must convert the format accordingly before writing to the CMX994A/CMX994E Extended Rx Offset Register ($17). For further details about the format of the I or Q correction values please refer to the CMX994/CMX994A/CMX994E Datasheet, available from the CML website.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Q Channel Correction Value						0	0	I Channel Correction Value					

Figure 25 - Format of CMX994A/E Extended Rx Offset register ($17)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	Q Channel Correction Value						I Channel Correction Value					

Figure 26 - Format of I/Q DC calibration reporting when CMX994A/CMX994E is selected

6.6.17 Rx Mode with CMX994 Powersave (I/Q mode only)

6.6.17.1 Overview

Significant power saving may be achieved by using the low-power features of the CMX994. These are controlled by the device automatically when powersave is enabled by selecting Rx mode with powersave ($C1, Mode Control b3-0 = $9). It will continue to powersave the CMX994 until a valid signal is detected. At this point a Powersave Exit IRQ will be raised and the power-saving state will be cleared. From this point the CMX994 will remain 'on', until the powersave mode is reapplied by rewriting to the Mode Control register again. The Mode Control register may also be re-written while the powersave is still active – this will have the effect of restarting the state machine from the beginning of the off time state. An overview of the powersave states can be seen in Figure 27.

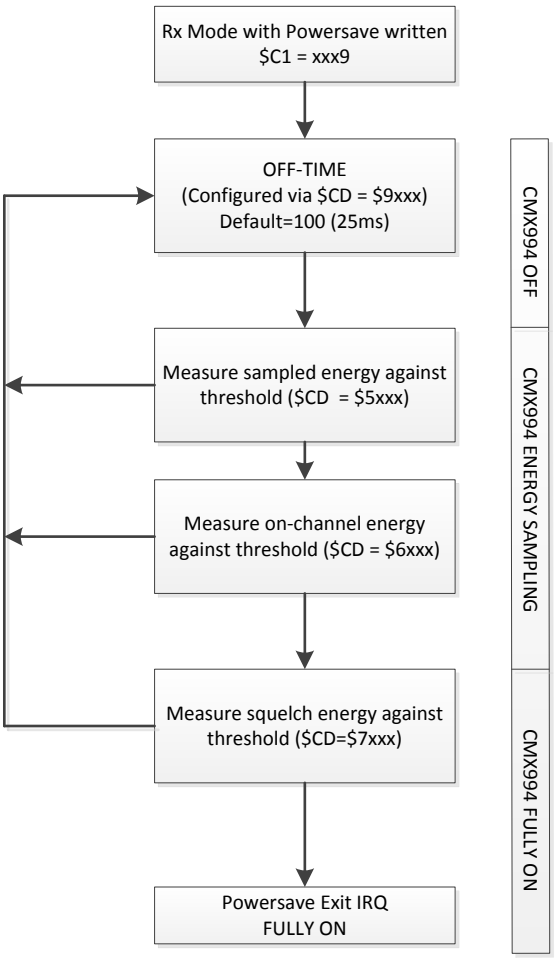


Figure 27 - Powersave States

There are three possible power states for the CMX994 under power saving mode.

- Max saving – the device is in this state during the OFF-TIME period and saves the maximum amount of power.
- Energy sampling – this state is used to sense energy present on the channel, using the minimum power required. It can be set to use less power than the normal 'on' state, depending on the type of CMX994 device connected, and configuration. For full details see section 6.6.17.2.
- Normal 'on' – this state is entered into once the energy threshold tests have been met and squelch calculations are required; it is the normal operating state for the CMX994 while receiving a signal and is based on the CMX994 register values written by the host via pass-through mode.

6.6.17.2 CMX994 Powersave Configuration and Options

The powersave functions are compatible with three variants of the CMX994: standard CMX994, CMX994A and CMX994E. The CMX994A and CMX994E contain additional hardware options which can be used to achieve improved powersaving. For full details consult the CMX994/CMX994A/CMX994E datasheet. The device in use should be selected by writing the appropriate value to Programming Register P6.2 (see section 8.3.7).

The CMX994 may be configured to further optimise the savings available. The controls are divided into three areas:

- Static mode selection of the CMX994/CMX994A/CMX994E via pass-through mode
- Threshold and Off-Time selection via the Aux Config ($CD) mechanism
- Configuration options in Program Block words 6.2 and 6.3

The static parameters which can affect current are listed below:

CMX994 Register / bit	Description	Notes
$11: b4	Low Power	Available on CMX994/CMX994A/CMX994E
$15: b1-0	Phase Correction Disable	Available on CMX994A/CMX994E only (for most applications these bits can be set to '11', saving approximately 15mA with no, or minimal, impact on system performance)
$15: b15-14	Enhanced Mode	Available on CMX994E only

With the static configuration in place, the powersave thresholds should be set to minimise the number of false triggers due to noise while maintaining good sensitivity. The default values provided should be good for most conditions. A larger saving can be made by adjusting the duty cycle via the Off-Time parameter, with a trade off being made against response time.

Dynamic switching of CMX994/CMX994A/CMX994E parameters can save further current during the energy sampling state of the powersave mode. The Low Power bit (and Enhanced Mode in the case of a CMX994E) can be automatically disabled during the energy sampling state and then restored to the host-configured value on exit. The CMX994A and CMX994E also allow for a single channel (I or Q) to be used in the energy sampling, reducing current further. Both of these options are configured in Programming Register P6.3 (see section 8.3.7).

6.6.17.3 Powersave Performance

The amount of current saved is shown in by Figure 28 which shows the variation in CMX994/A/E current with different "off" times. The two curves illustrate the difference in powersaving that can be achieved between the standard CMX994 and the CMX994A and CMX994E which allow the phase correction circuit to be disabled. The curves make use of the CMX994/CMX994A/CMX994E "LP" bit during powersave but it should be noted full RF performance is restored on exiting powersave.

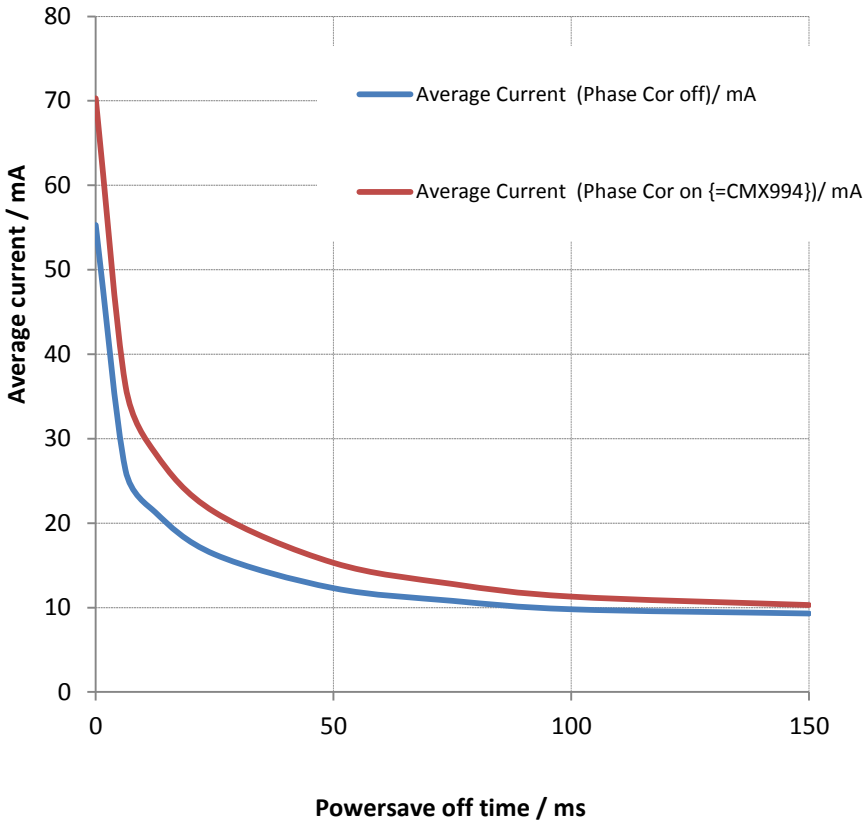


Figure 28 Effect of Powersave as a Function of "OFF" Time

The powersave operation has three states as described in section 6.6.17.1. The variation in powersave current is demonstrated by the currents shown in Table 16; each line in the table represents the powersave function deciding to continue in the powersaved state at each of the three possible decision points in the algorithm. The same effect is shown for "best case" and "worst case" scenarios as a function of "off" time in Figure 29.

Table 16 Variation in Average Current Consumption with Different Powersave States / Test Conditions

Test Condition	Average Current (typical, CMX994/CMX994A/CMX994E only) / mA
No signal	16.6
+65dB adjacent channel signal	18.1
Wideband signal (squelch closed)	38.3

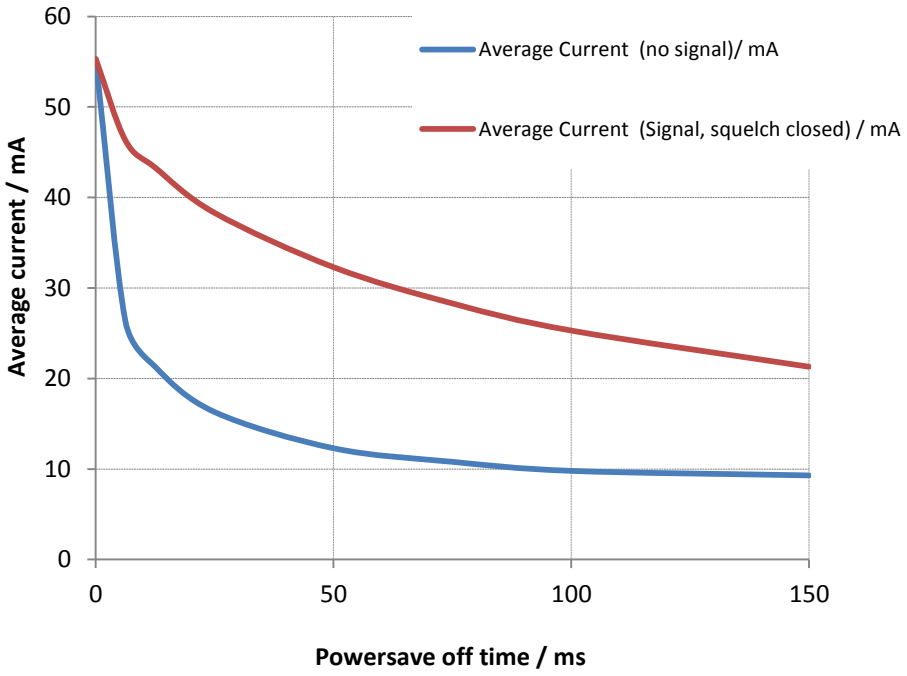


Figure 29 Effect of Powersave as a Function of "OFF" Time for Best Case and Worst Case Powesave State Evaluations

The user can decide which of the available powersave functions to use. The range of powersaving available is shown in Table 17. Each successive row in the table adds an extra powersave mode.

Table 17 Variation in Average Current Consumption with Different Powersave Configurations, "OFF" Time set at 25ms

Configuration	**Average Current (typical, CMX994/CMX994A/CMX994E only) / mA**
Standard CMX994 Powersave	27.3
Add "LP" bit	24.3
Add phase correction off (CMX994A/CMX994E only)	19.3
Add I or Q channel off (CMX994A/CMX994E only)	16.3

6.6.18 Data Transfer

Payload data is transferred from/to the host using blocks of five Rx and five Tx 16-bit C-BUS registers, allowing up to 72 bits (9 bytes) of data to be transferred in sequence. The lowest 8 bits of the register block are reserved for a Byte Counter, Block ID and a Transaction Counter. The byte count indicates how many bytes in the data block are valid and avoids the need to perform a full five word C-BUS read/write if only a smaller block of data need to be transferred.

Table 18 C-BUS Data Registers

C-BUS Address	Function	C-BUS Address	Function
$B5	Tx data 0-7 and info	$B8	Rx data 0-7 and info
$B6	Tx data 8-23	$B9	Rx data 8-23
$B7	Tx data 24-39	$BA	Rx data 24-39
$CA	Tx data 40-55	$BB	Rx data 40-55
$CB	Tx data 56-71	$C5	Rx data 56-71

Bits 7 and 6 hold the Transaction Counter, which is incremented modulo 4 on every read/write of the Data Block to allow detection of data underflow and overflow conditions. In Tx mode the host must increment the counter on every write to the TxData block, and if the CMX7241/7341 identifies that a block has been written out of sequence, the Event bit (C-BUS register $C6, b14) will be asserted and an IRQ raised, if enabled. The device detects that new data from the host is available by the change in the value of the Transaction Counter, therefore the host should ensure that all the data is available in the TxData block before updating this register (i.e. it should be the last register the host writes to in any block transfer). In Rx mode, the CMX7241/7341 will automatically increment the counter every time it writes to the RxData block. If the host identifies that a block has been written out of sequence, then it is likely that a data overrun condition has occurred and some data has been lost. If a CRC failure has been detected when decoding the data block, an 'Event' IRQ is issued concurrently with the 'Data Ready' IRQ along with a status code in the 4FSK Modem Status register ($C9).

6.6.19 Vocoder/CMX994 Pass-through

To allow the host to communicate directly with the CMX6x8/CMX7262/CMX994 for test and configuration purposes, a pass-through mode allows any CMX6x8/CMX7262/CMX994 C-BUS register to be read or written (as appropriate) accessed as Program Block $0F (see section 8.1.43). This mode uses the Programming ($C8), Program Block Address ($C7) and RxData0 ($B8) registers on the CMX7241/7341.

To write to the CMX6x8/CMX7262:

- Set the CMX7241/7341 to Idle mode ($C1=$0000)
- Wait for the Program Flag to be set ($C6 b0)
- Write the CMX6x8/CMX7262 C-BUS address to the Program Block Address register ($C7) with b15-8=$6F (write, 16 bit, Pass-through mode)
- Write the data value to the Programming register ($C8)
- Wait for the Program Flag to be set ($C6 b0).

To read from the CMX6x8/CMX7262:

- Set the CMX7241/7341 to Idle mode ($C1=$0000)
- Wait for the Program Flag to be set ($C6 b0)
- Write the CMX6x8/CMX7262 C-BUS address to the Program Block Address register ($C7) with b15-8 = $EF (read, 16 bit, Pass-through mode)
- Write a dummy value to the Programming register ($C8) to trigger the read operation
- Wait for the Program Flag to be set ($C6 b0)
- Read the CMX6x8/CMX7262 data value from the RxData0 register ($B8).

CMX6x8/CMX7262 C-BUS addresses are all 8 bits long and should be written to bits 0-7 of the Programming Register. Bit 15 is the read/write flag (0 = read, 1 = write) and bit 14 is the register-size flag (0 = 8-bit, 1 = 16-bit). Unused bits should be cleared to zero. When an 8-bit register is read or written, the data occupies the lower 8 bits of the appropriate register (Programming register or RxData0).

To write to the CMX994:

- Set the device to Idle mode ($C1=$0000)

- Wait for the Program Flag to be set ($C6 b0)
- Write the CMX994 C-BUS address to the Program Block Address register ($C7) with b15-8=$0F
- Write the CMX994 data value to the Programming register ($C8)
- Wait for the Program Flag to be set ($C6 b0).

Note that it is NOT possible to read data back from the CMX994 using this interface.

When using the CMX994A or CMX994E, the Extended Rx Offset Register ($17) is 16 bits wide. In order to access this register select 16-bit mode by setting b14 of the Program Block Address register ($C7) (all other registers are 8 bits wide so b14 must be left at zero for any other register).
For example, writing $4F17 to the Program Block Address register will access register $17 on the CMX994A in 16-bit mode. The full 16 bits to write should then be written to the Programming Register ($C8) in accordance with the register description.

6.7 dPMR Formatted Operation

The CMX7241/7341 performs all frame building/splitting and FEC coding/decoding functions, which relieves the host controller of a significant processing load. During voice calls the CMX7241/7341 can automatically enable and control the CMX6x8 or CMX7262, and transfer voice payload data from/to it without host intervention. In Rx mode, the CMX7241/7341 can monitor Colour Codes and address fields in incoming transmissions and only accept calls if the programmed address requirements are satisfied. This allows the host to remain in a power-down or 'sleep' state until it is really necessary to wake up, extending the battery life of the final product design. For Mode 3 (trunked) operation the host may need to monitor ALL traffic on the Beacon channel.

6.7.1 Colour Codes

The standard defines 64 Colour Codes, which are 24-bit sequences sent in Message and Payload frames for RF channel or system identification purposes. The CMX7241/7341 stores the full table internally and identifies Colour Codes using their 6-bit index in this table. In Tx mode the host should supply the index of the Colour Code to be sent in the Aux Data 2 register ($A2). In Rx mode the CMX7241/7341 reports the index of the detected Colour Code in the AuxData and Analogue Status register ($CC) and can optionally compare it against the Colour Code specified in the Aux Data 2 register ($A2) before accepting the burst. Colour Code checking is enabled using b9 of the 4FSK Modem Configuration register, $A1.

6.7.2 Addressing

The standard defines two addressing schemes: 24-bit binary or 7-digit BCD (binary-coded-decimal). Both addressing schemes are supported by the CMX7241/7341, selected by b11 in the 4FSK Modem Configuration register, $A1 (see User Manual Section 8.1.20). The standard does not mandate BCD addressing unless the host implements the Standard User Interface, but the advantages of BCD addressing are direct mapping of user keypad entries to destination addresses and the option of wildcard digits to implement group calls. BCD addresses can include wildcard digits in any of the lower four digits, and there are ten BCD 'All-Call' addresses with wildcards in all six lower digits.

The host can load two Own IDs into Program Block 1 for use in Rx mode address checking, which is enabled using b10 of the 4FSK Modem Configuration register, $A1. The CMX7241/7341 then compares the 'Called ID' field from incoming bursts against each of its Own IDs, and will reject the burst if a valid ID match is not found. If b11 of the 4FSK Modem Configuration register, $A1, is set the CMX7241/7341 will perform BCD translation of the Own IDs and the received 'Called ID' field before comparing them, allowing group call matching using wildcards.

TS 102 658 also specifies a system-wide All Call facility using the 'Communication Format' field in Header Frames (TS 102 658 section 5.5.6). The normal setting for this field is 'Peer-to-Peer', but when set to 'Call ALL' the CMX7241/7341 will always accept the call regardless of address settings. The host should take care not to transmit in All Call mode unless actually intended.

6.7.3 Data Formats

TS 102 658 defines the frame and data formats of the dPMR system for both Traffic and Beacon channels. Mode 1 and 2 systems only use Traffic channels. Mode 3 systems also use Beacon channels to manage the radio network, and terminals move onto a traffic channel when a call is actually made. Channel type is selected using b12 of the 4FSK Modem Configuration register, $A1.

The CMX7241/7341 uses the TxData and RxData registers to transfer data to and from the host. The Block ID field in the TxData0 register informs the CMX7241/7341 how to process each transfer. Payload may be Voice, Type 1, Type 2 or UDT Appended Data as defined in the initial Header frame but Packet (Type 3) Data is not currently supported. Payload data transfers are made in 9-byte blocks except for Type-2 data which is transferred in 5-byte blocks.

b5-4	Block ID	over-air bits	un-coded bits
00	MSG – Message Data	120	72
01	PLD – Payload or UDT (Traffic Channel) SYS – SYScast (Beacon Channel)	72 72	72 / 40 17
10	CCH – CCH data	72	41
11	END – End Data	36	17

Figure 30 Block ID

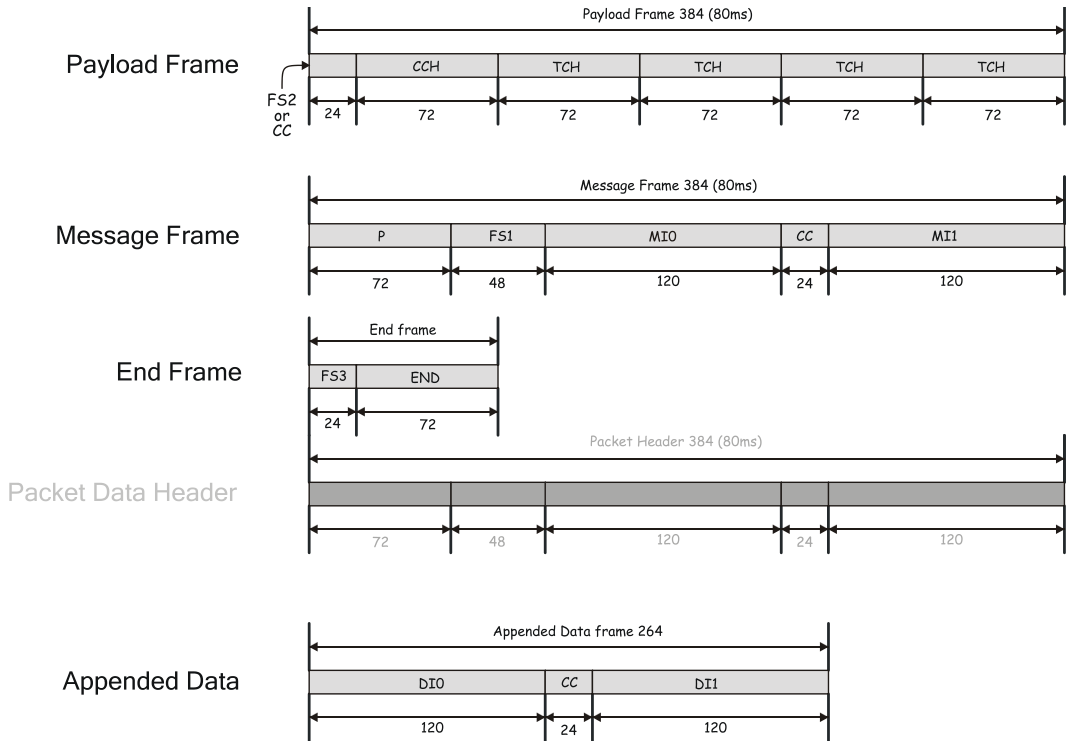


Figure 31 Traffic Channel Data Formats

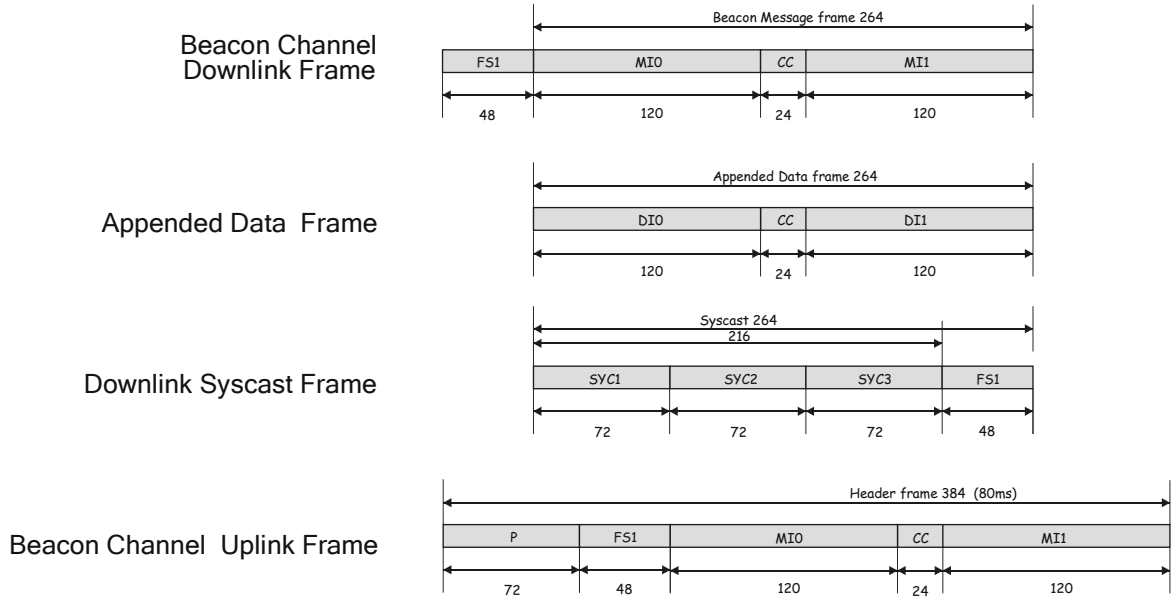


Figure 32 Beacon Channel Data Formats

Type-3 Message Data:

The occurrence of a Type-3 packet data burst is primarily signified by the presence of the FS4 sync pattern, rather than the FS1 used for all other bursts. It should be noted that FS4 is the logical inverse of FS1, so radio designs that inadvertently invert the demodulated waveform can erroneously report an FS4 when an FS1 would be expected – this should, however, be corrected in the design stage of the radio's development and should not occur in the field. The use of the FS4 enables the data contained in the Message/Header block to be formatted in a different manner, though, in practice, there a number of similarities. The subsequent burst format of the data is however, significantly different and requires a new handler for both Rx and Tx to be invoked.

Data Format:

The data formats of a Type-3 burst are shown in the following diagram as examples. It should be appreciated that ONLY the burst carrying the Type-3 data uses the FS4, any initial call-set-up or polling bursts to check for radio presence or routing utilise the standard FS1 style bursts that are already supported. The MI_detail field specifies the data length and the number of packets-per-burst. This is significantly different from the normal superframe format. In this implementation, as soon as an FS4 is detected, the burst which follows is assumed to be Type-3 data, irrespective of any other settings in the Message/Header block.

It should be noted that only two of the four possible values of pDs (data length) are supported – these being:

- pDs = 0 (288 bits)
- pDs = 3 (1440 bits)

See TS 102 658 section 9.4.

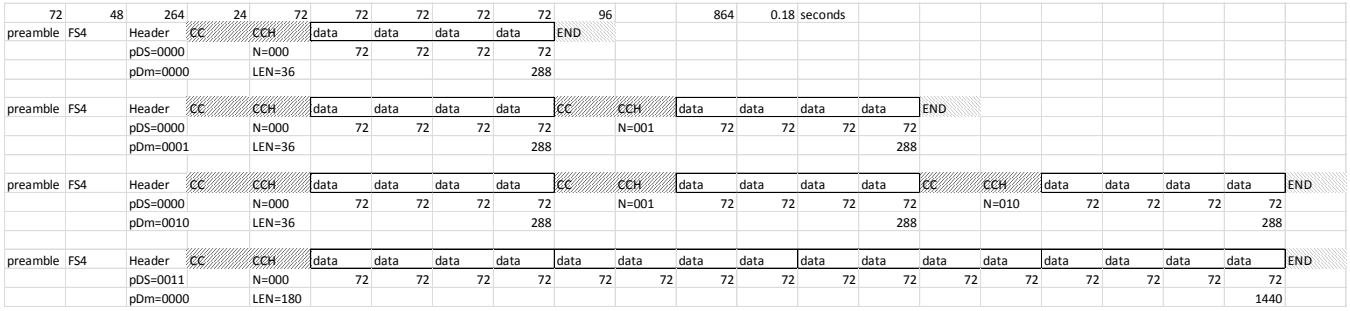


Figure 33 Type-3 Data Formats

Message Data:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	3	Message Type		0	23	Called ID		20	T-Count		Blk ID=00		Byte Count=1001			
1	19	Called ID						4								
2	3	Called ID		0	23	Calling ID				12						
3	11	Calling ID					0						2	M	0	V(b1)
4	V(b0)	1	F 0		EP	PM	2	MI_TYPE 0	7	MI_DET		0				
Aux (Rx)	ID Match			x	Group ID Match				x	x	Colour Code					
Aux (Tx)	Repeat Header Count				0	0	0	0	0	0	Colour Code					

For the Type-3 Message/Header Block, the contents are:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	3	MT = 0000		0	23	Called ID		20	0	0	0	0	1	0	0	1
1	19	Called ID						4								
2	3	Called ID		0	23	Calling ID				12						
3	11	Calling ID					0						2	M = 100	0	V(b1)
4	V(b0)	1	F 0		EP	PM	2	MI (011) 0	3	pDs (0000 - 0011)			3	pDm (0000 - 0111)		

which results in the following data being transferred by the host (in hex):

TxData0 $0009
TxData1 $0000
TxData2 $1000
TxData3 $0028
TxData4 $0330

The values for pDs and pDm should be set appropriately for the following data transfers. The value of the Communications Mode field should be set to 100b, and Message_Info_Type to 011b (See TS 102 658 5.5.7, 5.5.19.3 and Section 9).

Payload / UDT Data:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	data								T-Count		Blk ID=01		Count=0101 or 1001			
1	data								data							
2	data								data							
3	data								data							
4	data								data							

SYScast data:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	data								T-Count		Blk ID=01		Byte Count=0011			
1	data									x	x	x	x	x	x	x
2	not used															
3	not used															
4	not used															

CCH data:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	data								T-Count		Blk ID=10		Byte Count=0110			
1	data								data							
2	data								data							
3		x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
4	not used															
Aux	ID Match			x	Group ID Match				Colour Code							

Type-3 CCH Data:

For the embedded CCH block, the contents are:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	2	N	0	7	LEN	3			0	0	1	0	0	1	1	0
1	2	LEN	0	dummy = 0												
2	0	15	CRC for DATA field													1
3	0	dummy = 0														
4	not used															

which results in the following data being transferred to the host (in hex):

TxData0 $0426

TxData1	$8000	
TxData2	$091C	Note: an arbitrary CRC value is shown.
TxData3	$0000	
TxData4	not used	

The host MUST supply valid values for all fields in the CCH block as the transmission progresses. In particular, the values of N and the Data CRC field MUST be updated appropriately for each block. This is a significant difference from Type-1 and Type-2 formats (where the FI will do its best to auto-generate the contents of the CCH field, based on the information provided in the initial Message/Header block from the host). All the parameters provided by the host in the CCH block are passed directly "to air", they are not validated or used internally.

End Data:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	ET	0	1	ARQ	0	3	Tx_WAIT		0	T-Count		Blk ID=11		Byte Count=011	
1	4	STAT		0		*reserved*				x	x	x	x	x	x	x
2	not used															
3	not used															
4	not used															

6.7.4 Tx Mode (dPMR formatted)

In Tx dPMR™ Formatted mode ($C1, Mode Control = $0012), the CMX7241/7341 implements all FEC coding, interleaving and scrambling functions for Message Information, UDT Appended Data, Control Channel Information, Payload and End Information blocks, and inserts Frame Sync and Colour Code sequences to generate the required frame formats for transmission. During voice calls the CMX7241/7341 can automatically enable and control the CMX6x8/CMX7262 or SPI-Codec port, and transfer voice payload data from/to it without host intervention. The host should load Message Information, Control Channel Information and End Information blocks into the TxData registers with fields packed in their over-air format as shown in TS 102 658.

At the start of a transmission the host should preload the TxData registers with the initial Message Information data block before placing the CMX7241/7341 in Tx dPMR Formatted mode. The device will then send the Preamble, FS1 and Message Frame and will read the 'Message Type' field to determine the following burst type that will follow. If the 'Call Information' field indicates that extended wake-up Headers are to be sent, the CMX7241/7341 will do so automatically without reloading by the host. In payload bursts the Header fields are saved for re-use as Control Channel Information fields in the following Payload frames that follow, unless the host loads fresh Control Channel Information blocks during the call.

Unless the 'Message Type' field indicates the burst is a bare Message frame the CMX7241/7341 will now expect the host to load a series of Payload Data, UDT Appended Data and/or End Data blocks as appropriate. For Disconnect bursts which contain a repeated Message/End Frame pair the host should only load single blocks of Header and End Data, and the CMX7241/7341 will then resend the duplicate frames automatically. In Payload bursts the CMX7241/7341 will automatically save and re-use the initial Header fields to build Control Channel Information blocks which are then inserted automatically into each Payload frame. However if Slow Data is being sent (or any other changes to the CCH fields are required) then the host must re-load all four CCH blocks in each super-frame in correct sequence between payload data transfers.

If the CMX6x8/CMX7262 vocoder is enabled and the 'Communications Mode' field in the Header Frame indicates a voice call, the CMX7241/7341 will automatically enable the vocoder microphone input and route payload data from the vocoder for transmission. Note that the CMX6x8 or CMX7262 will take a finite time to encode the incoming voice data, during which the CMX7241/7341 will automatically insert 'silence' data into

the payload frames. Alternatively, if SPI-Codec mode has been enabled, the device will automatically enable the Audio Codec and deliver audio PCM samples to the SPI-Codec port. The host can load an End Frame at any point to terminate the call. At the end of all dPMR transmissions the CMX7241/7341 will issue a 'Tx Done' IRQ when it is safe for the host to place the device back into Idle mode ($C1, Mode Control = $0000).

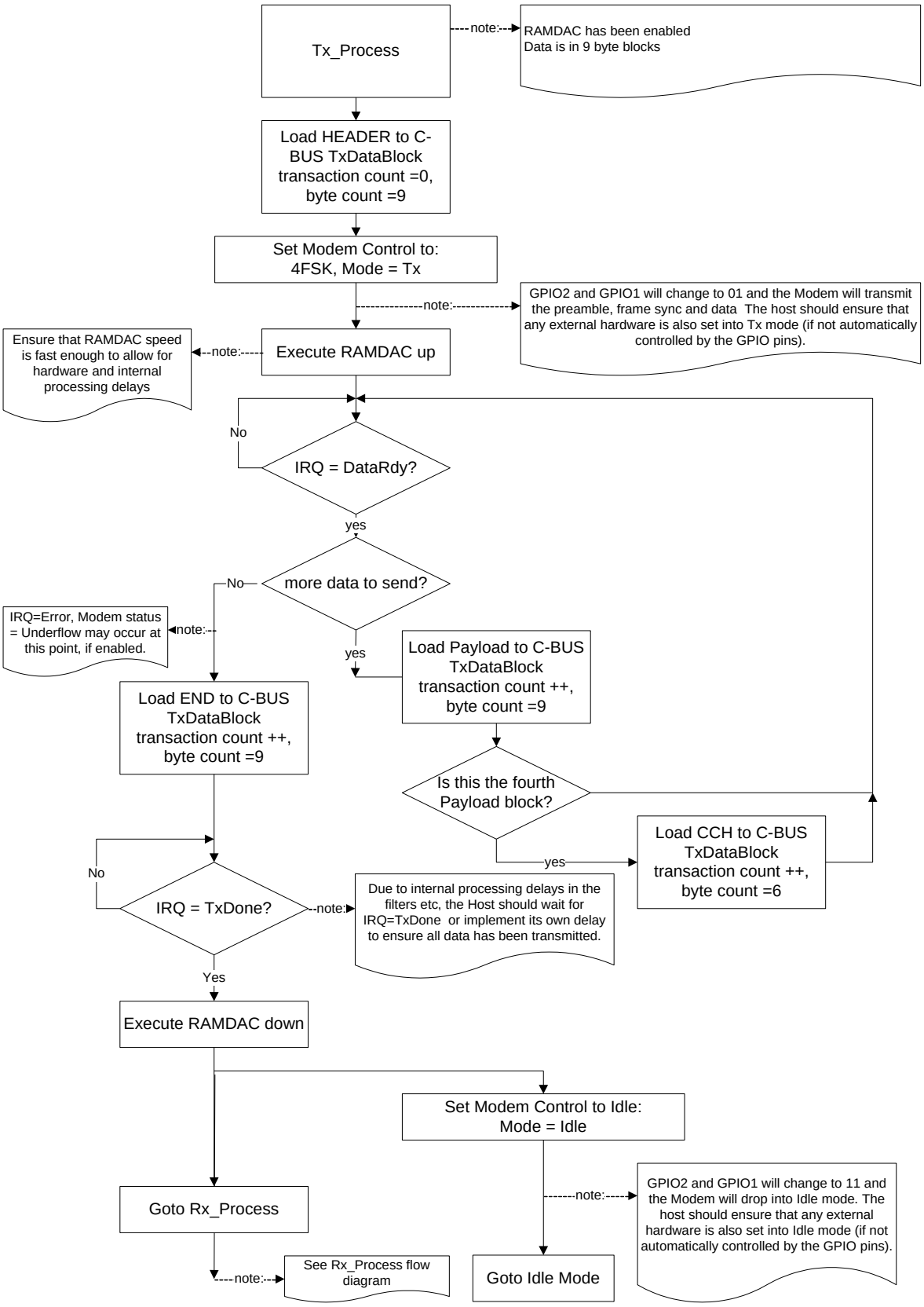


Figure 34 Tx Data Flow

6.7.5 Rx Mode (dPMR formatted)

In Rx dPMR Formatted mode ($C1, Mode Control = $0011) the CMX7241/7341 automatically splits incoming calls to extract Message Information, SYScast data, UDT Appended Data, Control Channel Information, Payload and End Information blocks and performs all the necessary de-scrambling, de-interleaving and FEC decoding functions. In voice calls the CMX7241/7341 can automatically enable the CMX6x8/CMX7262 vocoder or SPI-Codec port when required and transfer received speech data without host intervention.

The RxData registers are used to transfer Message, SYScast, UDT Appended Data, CCH and End Data fields in addition to payload data. The Block ID field in the RxData0 register informs the host what type of data block each transfer contains. The field layout in the RxData registers for the different transfer types is the same as for Tx dPMR Formatted mode (section 6.7.3).

To receive a Beacon channel the host should set the BEACON bit (b12) in the 4FSK Modem Configuration register ($A1) before placing the CMX7241/7341 in Rx dPMR Formatted mode. Otherwise if this bit is clear the CMX7241/7341 processes incoming transmissions as Traffic channel calls.

When placed in Rx dPMR Formatted mode the CMX7241/7341 begins scanning for frame sync sequences in the received signal. In addition to detecting the 48-bit FS1 frame sync at the start of a burst, the CMX7241/7341 can also perform 'late entry' into a voice call by detecting two successive copies of the 24-bit FS2 sequence at the correct two-frame spacing. When any valid frame sync sequence has been detected, an 'FS Detect' IRQ is issued and the data demodulator is enabled.

After detecting a frame sync the CMX7241/7341 decodes the contents of the following Message Frame (after an FS1 detect) or Control Channel Information blocks (after an FS2 detect). The Message Information or CCH Information CRCs are checked and processing continues only if valid fields have been received. Message Frames contain two duplicate Message Information blocks and the CMX7241/7341 checks both block CRCs, uses the first valid block and discards the other.

When repeated 'extended wake-up' Header Frames are received (see TS 102 658 section 11.1) the CMX7241/7341 will decode the first valid Header Frame and then ignore all following repeat Headers. This maximises the time the host can be kept in powersave.

After an FS2 detect, if address checking is enabled the CMX7241/7341 will wait to receive all four CCH blocks in a superframe and then repack the fields into the Message Information block format for transfer to the host. If address checking is not enabled the CMX7241/7341 only requires a single valid CCH block to determine the payload type and will immediately start transferring the following CCH and Payload blocks without waiting for a full superframe. The host should collect the remaining address fields from the following CCH blocks as they are transferred.

Address and Colour Code checking can be enabled with b9 and b10 of the Modem Configuration register; otherwise the CMX7241/7341 will accept all incoming calls. The Colour Code is checked first using the Colour Code index specified in the Tx AuxData register ($C2). If the received Colour Code does not match then the burst is rejected. Address checking now takes place depending on the addressing mode selected. Broadcast Messages and headers with the 'Communications Format' field set to 'Call ALL' are always accepted. Otherwise the 'Called ID' is checked against the device's Own IDs (programmed by the host into Program Block 1) and if a match is found the call is accepted. In any of these cases a 'Called' IRQ is issued to the host, otherwise the call is dropped with no further host notification and the CMX7241/7341 returns to frame sync search.

Depending on the burst type the CMX7241/7341 will decode the following Payload, SYScast, UDT Appended Data or End Frames and present their contents to the host or vocoder. If the CMX6x8/CMX7262 Vocoder is enabled and the 'Communication Mode' field in the Header Frame indicates a voice call, the CMX7241/7341

will automatically enable the vocoder speaker output and route payload data to the vocoder for decoding. In this mode, the data is transferred in 4-bit Log-Likelihood-Ratio format. Otherwise payload data is presented to the host in the RxData registers in soft or hard format as specified. When an End Frame is received the CMX7241/7341 will report its contents to the host, disable the vocoder (if necessary) and return to frame sync search.

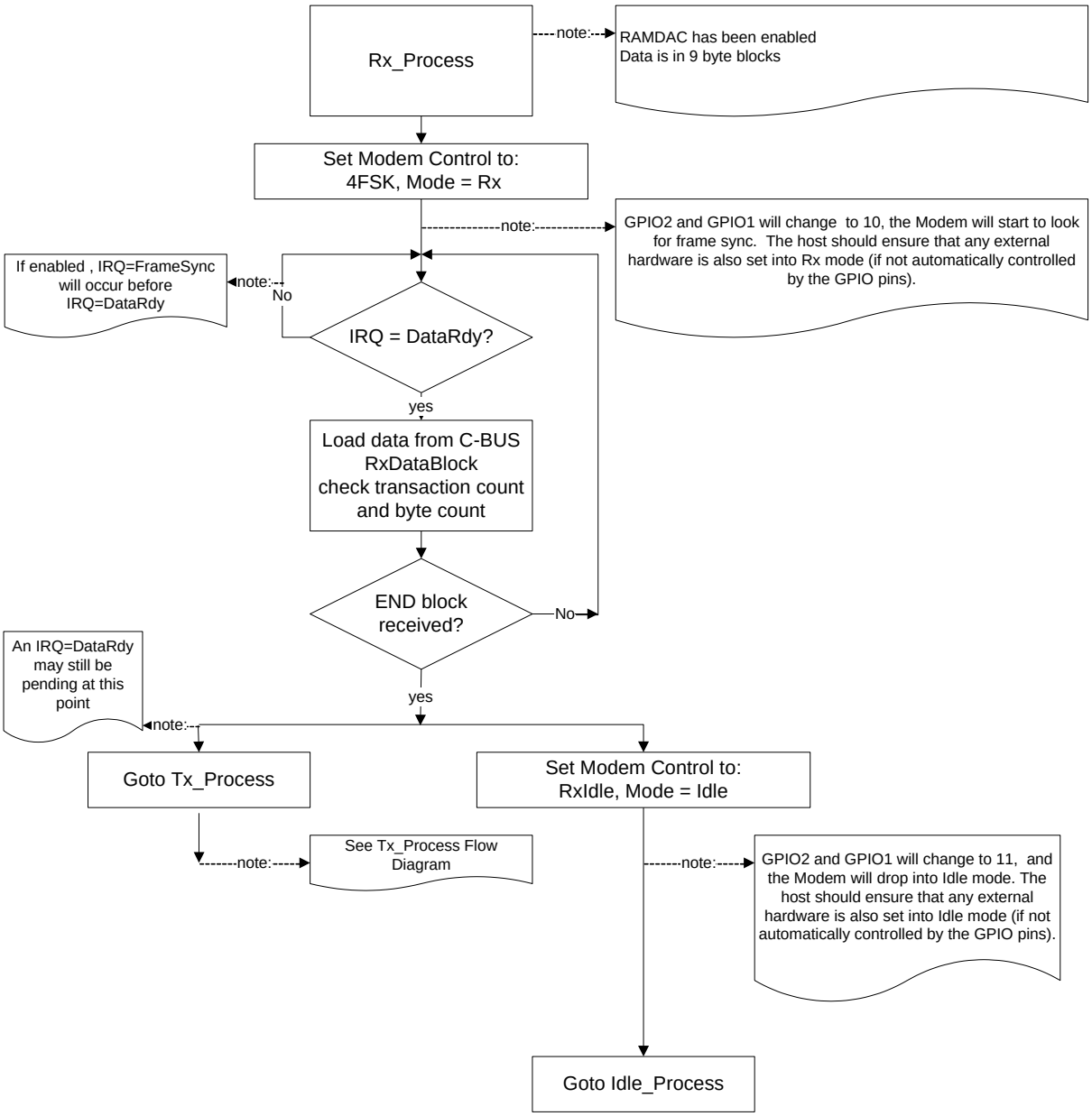


Figure 35 Rx Data Flow

All frame sync sequences, Colour Codes and CRCs contained in payload superframes are checked and an 'Event' IRQ is issued when any are received incorrectly. If all the frame sync sequences, Colour Codes and CRCs in a superframe are received incorrectly, the superframe is considered corrupt. The host can set a threshold for consecutive corrupt superframes (in Program Block 0) after which the CMX7241/7341 will issue an 'Event' IRQ, drop the call and return to frame sync search.

See:

- RxData 0 - $B8 read

6.7.6 Slow Data

The CCH Data block in each frame contains two 9-bit words of Slow Data which should be handled as necessary by the host. In Tx mode CCH Data block transfers are optional and if not reloaded the CMX7241/7341 will re-use the CCH fields from the preceding superframe or Message frame. When fresh CCH Data blocks are supplied then all four CCH Data blocks in the current superframe must be reloaded. In Rx mode the received CCH Data blocks are always transferred to the host.

6.8 Analogue PMR Description

6.8.1 Sub-Audio Processing

The filter used in the path can be set by the Program Register P2.0, either a 260Hz Chebyshev suitable for CTCSS or a 150Hz 4-pole Bessel for DCS.

An internal generator/detector is available for the 51 CTCSS tones shown in Table 20 and the 83 DCS codes shown in Table 19. Squelch-tail elimination is provided by inverting the MOD outputs or executing a phase change in CTCSS mode or a 134Hz “turn-off tone” in DCS mode. The tone/code to be generated is set by the value in the Analogue Mode register ($C2) in Tx mode and read from the AuxData and Analogue Status register ($CC) in Rx mode (see section 8.1.38).

Support for external sub-audio detection and generation is provided using the CTCSS and DCS filters. The Filter bandwidths are selectable for:

- 134Hz – LTR
- 150Hz – LTR / DCS
- 180Hz – LTR
- 260Hz - CTCSS

6.8.2 Voice Processing

A set of Audio Processing blocks are available for use in Analogue mode:

- 300Hz HPF
- 12.5kHz channel filter or 25kHz channel filter
- Hard limiter with anti-splatter filter
- Pre-emphasis and De-emphasis
- Compander
- Scrambler
- Voice AGC
- Level adjust
- In–band audio generator/s in both Rx and Tx paths

The 12.5kHz channel filter (narrow) will be selected by default, the 25kHz filter (wide) can be enabled by setting P2.0:b0. Note that selecting 25kHz mode operation in I/Q mode will automatically inhibit dPMR operation due to the difference in receiver bandwidths. Parallel analogue / digital mode is only available in 12.5kHz mode.

6.8.3 300Hz HPF

This is designed to reject signals below 300Hz from the voice path so that sub-audio signalling can be inserted (in Tx) or removed (in Rx) as appropriate. It should be enabled whenever sub-audio signalling is required.

6.8.4 12.5kHz/25kHz Channel Filters

These are designed to meet the requirements of ETSI 300 296 for Voice signal processing and feature an upper roll-off at 2.55kHz and 3.0kHz respectively.

6.8.5 Hard Limiter

This is provided to limit the peak deviation of the radio signal to meet the requirements of ETSI EN 300 296. An anti-splatter filter is included to reduce the effects of any harmonic signals generated in the process. The limiter threshold can be set using P2.3.

6.8.6 Compander

A syllabic compressor/expander is provided, similar to that used in the 7031/7041-FI-1.x to increase the dynamic range of the Voice signal. The unity gain points for Tx and Rx can be set independently using P2.9 and P2.10.

6.8.7 Scrambler

A frequency inversion scrambler is provided to enable a basic level of privacy. The default inversion frequency is 3300Hz, but can be programmed using $C3:1001b, however some loss of signal at the band edges may occur due to the channel filter roll-off.

6.8.8 Voice AGC

An automatic gain control system is provided in the MIC path, utilising the programmable gain settings of the Input 1 amplifier. When used in conjunction with the hard limiter function, this can compensate large variations in the MIC input signal without introducing significant distortion. The AGC threshold is programmable using P2.1. whilst the maximum gain setting and the decay time can be set using P2.2. When this feature is enabled, the host should not attempt to directly control the Input 1 gain setting.

6.8.9 Level Adjust

Independent level adjustments are provided using $C3 register for the voice, in-band and sub-audio signals as shown in Figure 36 Tx Level Adjustments and Figure 37 Rx Level Adjustments

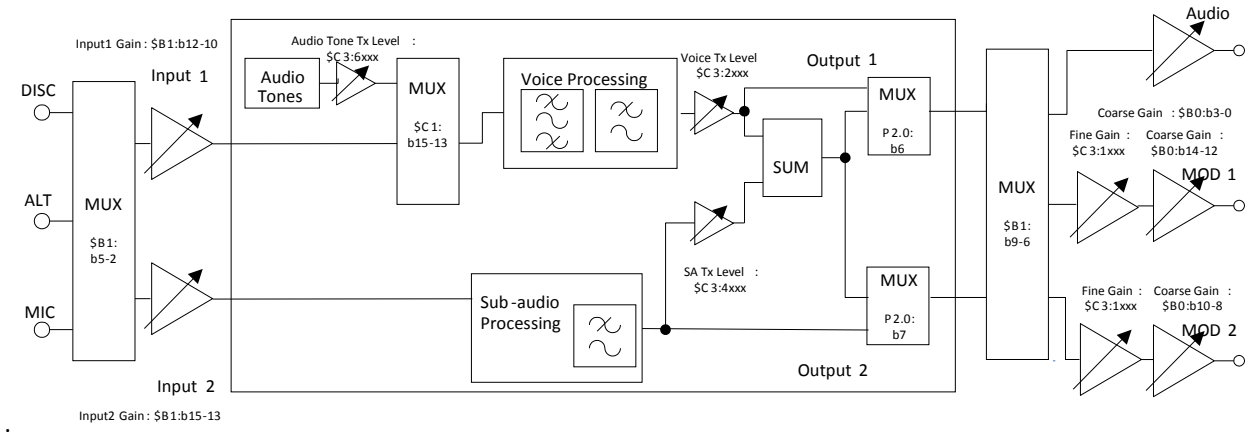


Figure 36 Tx Level Adjustments

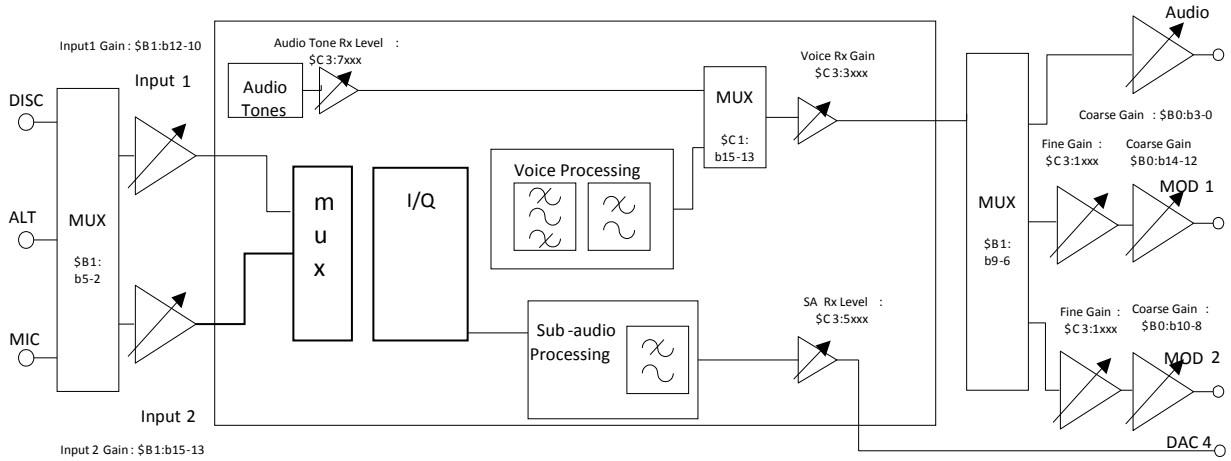


Figure 37 Rx Level Adjustments

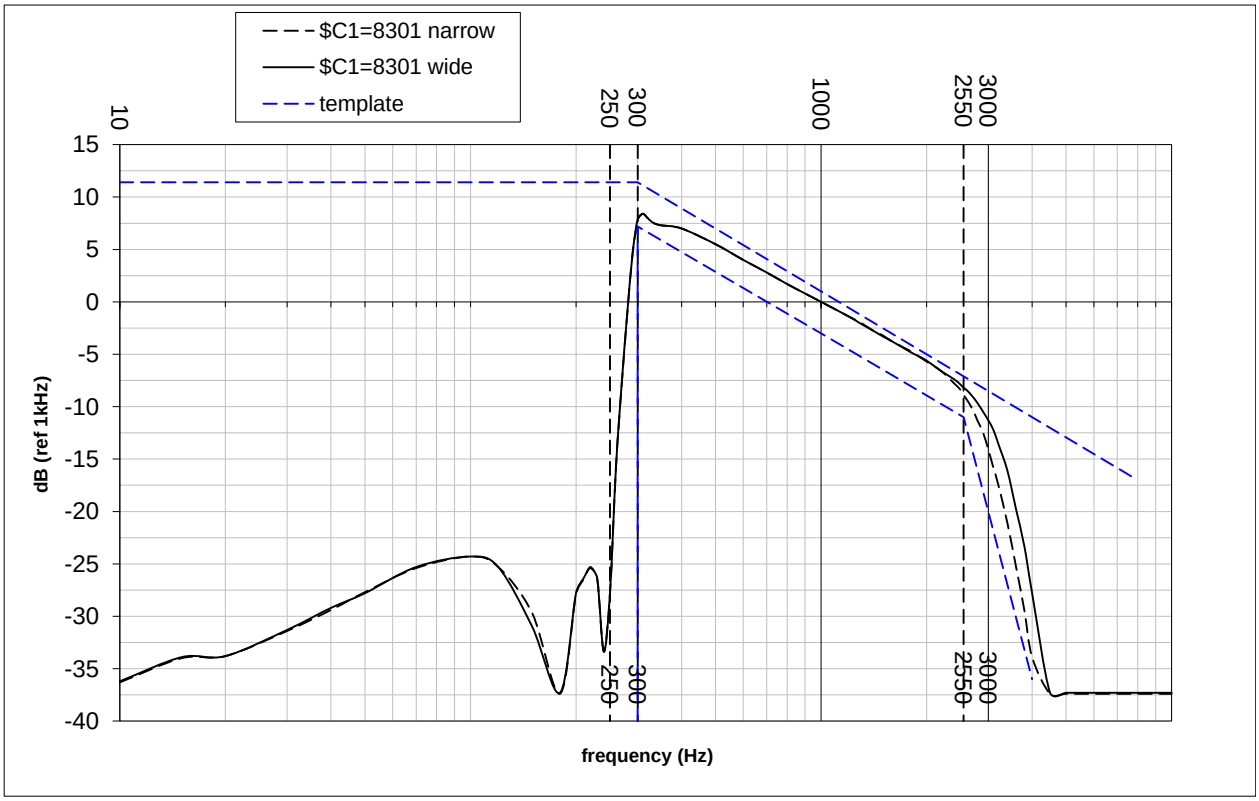


Figure 38 Rx Audio Response

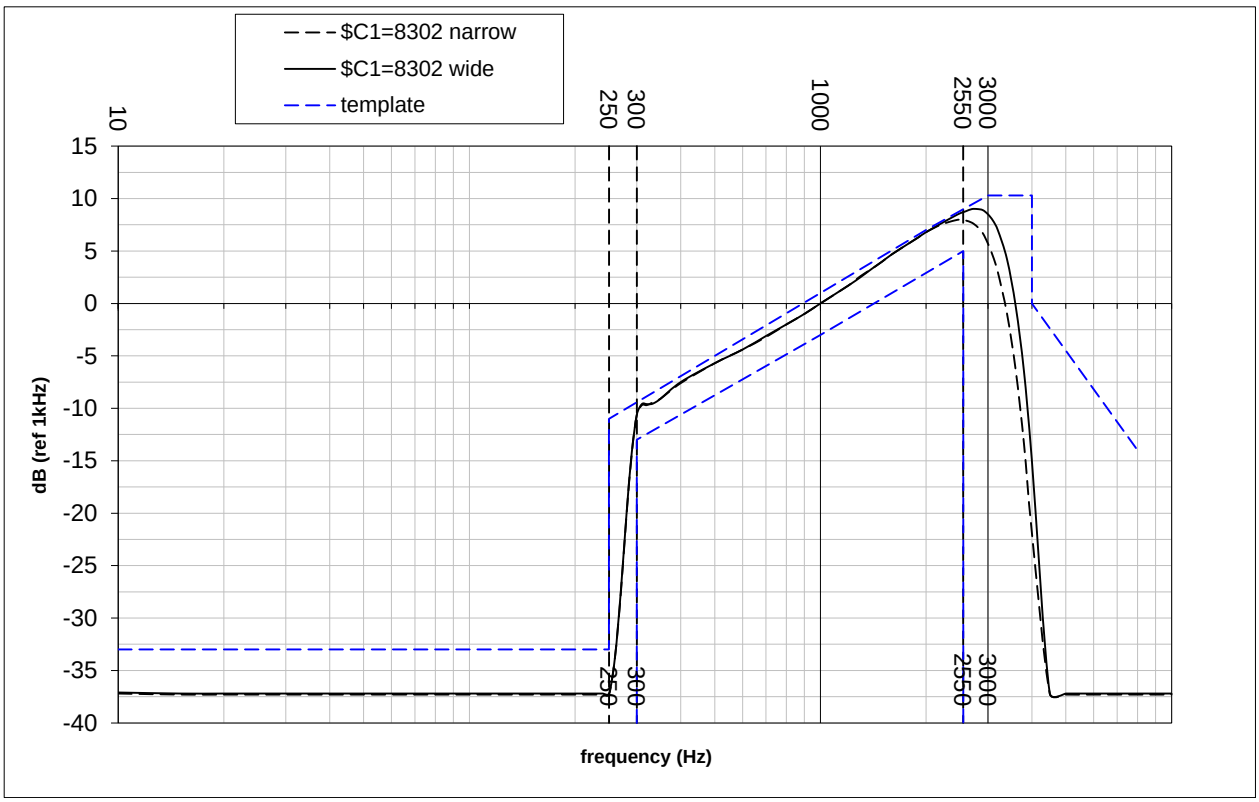


Figure 39 Tx Audio Response

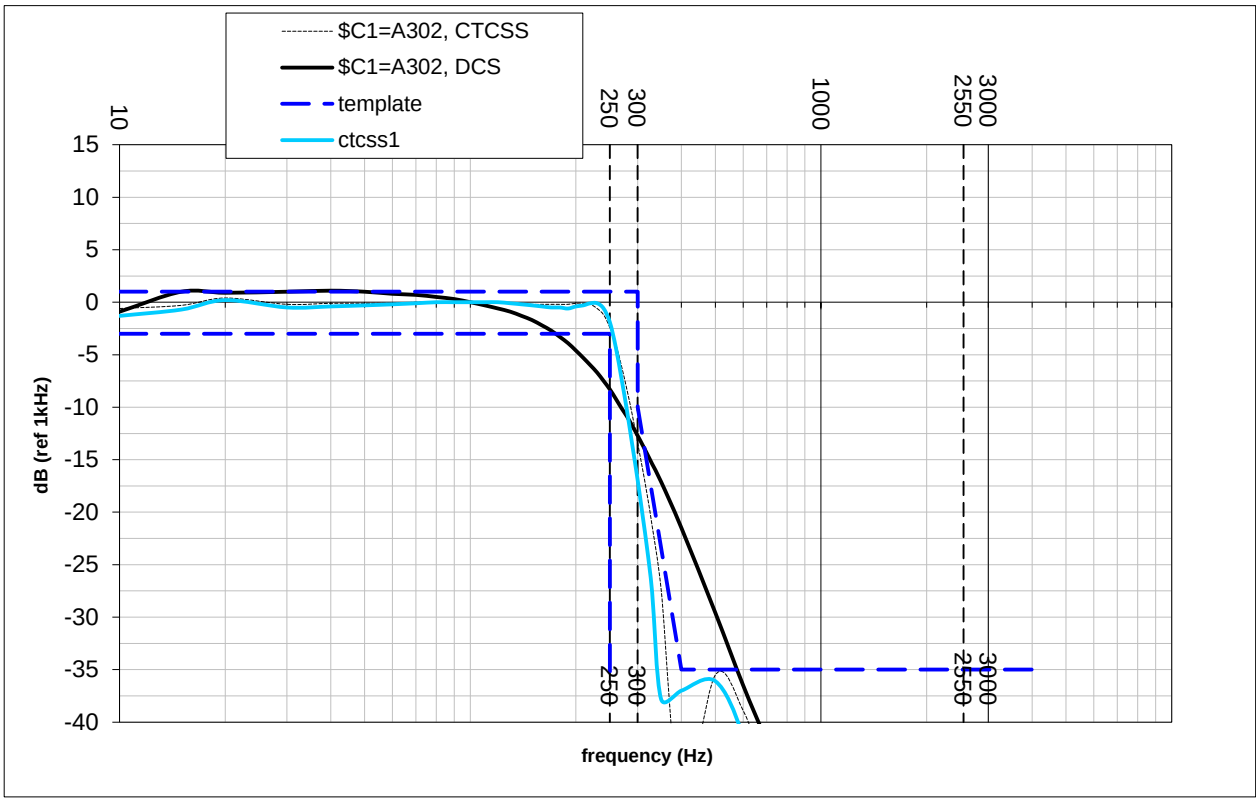


Figure 40 CTCSS and DCS filters

Table 19 DCS codes and values

	Register Value					Register Value			
DCS Code	**true**		**inverted**		**DCS Code**	**true**		**inverted**	
	Decimal	Hex	Decimal	Hex		Decimal	Hex	Decimal	Hex
no code	0	00	100	64	**311**	42	2A	142	8E
23	1	01	101	65	**315**	43	2B	143	8F
25	2	02	102	66	**331**	44	2C	144	90
26	3	03	103	67	**343**	45	2D	145	91
31	4	04	104	68	**346**	46	2E	146	92
32	5	05	105	69	**351**	47	2F	147	93
43	6	06	106	6A	**364**	48	30	148	94
47	7	07	107	6B	**365**	49	31	149	95
51	8	08	108	6C	**371**	50	32	150	96
54	9	09	109	6D	**411**	51	33	151	97
65	10	0A	110	6E	**412**	52	34	152	98

	Register Value					Register Value			
DCS Code	**true**		**inverted**		**DCS Code**	**true**		**inverted**	
	Decimal	Hex	Decimal	Hex		Decimal	Hex	Decimal	Hex
71	11	0B	111	6F	**413**	53	35	153	99
72	12	0C	112	70	**423**	54	36	154	9A
73	13	0D	113	71	**431**	55	37	155	9B
74	14	0E	114	72	**432**	56	38	156	9C
114	15	0F	115	73	**445**	57	39	157	9D
115	16	10	116	74	**464**	58	3A	158	9E
116	17	11	117	75	**465**	59	3B	159	9F
125	18	12	118	76	**466**	60	3C	160	A0
131	19	13	119	77	**503**	61	3D	161	A1
132	20	14	120	78	**506**	62	3E	162	A2
134	21	15	121	79	**516**	63	3F	163	A3
143	22	16	122	7A	**532**	64	40	164	A4
152	23	17	123	7B	**546**	65	41	165	A5
155	24	18	124	7C	**565**	66	42	166	A6
156	25	19	125	7D	**606**	67	43	167	A7
162	26	1A	126	7E	**612**	68	44	168	A8
165	27	1B	127	7F	**624**	69	45	169	A9
172	28	1C	128	80	**627**	70	46	170	AA
174	29	1D	129	81	**631**	71	47	171	AB
205	30	1E	130	82	**632**	72	48	172	AC
223	31	1F	131	83	**654**	73	49	173	AD
226	32	20	132	84	**662**	74	4A	174	AE
243	33	21	133	85	**664**	75	4B	175	AF
244	34	22	134	86	**703**	76	4C	176	B0
245	35	23	135	87	**712**	77	4D	177	B1
251	36	24	136	88	**723**	78	4E	178	B2
261	37	25	137	89	**731**	79	4F	179	B3
263	38	26	138	8A	**732**	80	50	180	B4
265	39	27	139	8B	**734**	81	51	181	B5
271	40	28	140	8C	**743**	82	52	182	B6
306	41	29	141	8D	**754**	83	53	183	B7
					user defined	84	54	184	B8

Table 20 CTCSS codes and values

Register Value		CTCSS tone		Register Value		CTCSS tone
Decimal	Hex	Frequency		Decimal	Hex	Frequency
200	C8	Tx: no tone Rx: Tone Clone		228	E4	173.8
201	C9	67.0		229	E5	179.9
202	CA	71.9		230	E6	186.2
203	CB	74.4		231	E7	192.8
204	CC	77.0		232	E8	203.5
205	CD	79.7		233	E9	210.7
206	CE	82.5		234	EA	218.1
207	CF	85.4		235	EB	225.7
208	D0	88.5		236	EC	233.6
209	D1	91.5		237	ED	241.8
210	D2	94.8		238	EE	250.3
211	D3	97.4		239	EF	69.3
212	D4	100.0		240	F0	62.5
213	D5	103.5		241	F1	159.8
214	D6	107.2		242	F2	165.5
215	D7	110.9		243	F3	171.3
216	D8	114.8		244	F4	177.3
217	D9	118.8		245	F5	183.5
218	DA	123.0		246	F6	189.9
219	DB	127.3		247	F7	196.6
220	DC	131.8		248	F8	199.5
221	DD	136.5		249	F9	206.5
222	DE	141.3		250	FA	229.1
223	DF	146.2		251	FB	254.1
224	E0	151.4		252	FC	user defined
225	E1	156.7		253	FD	Phase change
226	E2	162.2		254	FE	DCS turn-off
227	E3	167.9		255	FF	invalid tone

CTCSS detector thresholds and bandwidth are selectable using P2.4. Use of the “split tones” (239 to 251) will require a smaller bandwidth to be used, otherwise the adjacent tone frequency may be detected instead.

CTCSS phase changes (greater than +/- 90 degrees) are indicated by code $FD, and generated by writing to $C3 whilst the CTCSS generator is active. The phase change detector is enabled using P2.0:b2.

6.9 FFSK Data Modem

The device supports 1200 baud FFSK data mode suitable for use with MPT1327 or similar systems.
Selection of the FFSK mode is performed by bit 8 of the Mode register ($C1). Detection of the selected In-band signalling mode can be performed in parallel with voice reception.

See:

- Mode Control - $C1 write
- 4FSK Modem Configuration - $A1 write

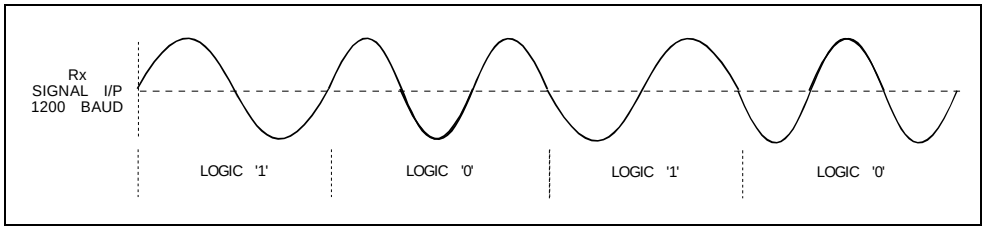


Figure 41 Modulating Waveforms for 1200 MSK/FFSK Signals

The table below shows the combinations of frequencies and number of cycles to represent each bit of data, for both baud rates.

Table 21 Data Frequencies for MPT1327 mode

Baud Rate	Data	Frequency	Number of Cycles
1200baud	1	1200Hz	one
	0	1800Hz	one and a half

Note: FFSK may be transmitted in conjunction with a CTCSS or DCS sub-audio component.

6.9.1 Receiving FFSK Signals

The device can decode incoming FFSK signals at 1200 and 2400 baud data rates. The desired rates can be configured by setting the Rx Mode in the FFSK Modem Format via the Analogue Control register ($C3). The form of FFSK signals is shown in Figure 41. An FFSK transmission begins with a preamble sequence followed by a 16-bit Sync sequence and then the user data.

The received signal is filtered and data is extracted with the aid of a PLL to recover the clock from the serial data stream. The recovered data is stored in a 2 byte buffer and an interrupt issued to indicate received data is ready. Data is transferred over the C-BUS under host µC control. If this data is not read before the next data is decoded it will be overwritten and it is up to the user to ensure that the data is transferred at an adequate rate following data ready being flagged. The FFSK bit clock is not output externally.

The extracted data is compared with the 16-bit programmed Frame Sync pattern (default is $CB23). An in-band IRQ will be flagged when the programmed Frame Sync pattern is detected. Once a valid Frame Sync pattern has been detected, the frame sync search algorithm is disabled; it may be re-started by the host disabling the FFSK bit of the Mode register ($C1:b8) and then re-enabling it (taking note of the C-BUS latency time).

Separate sync sequences are available, SynC, SynD, SynT and SynX. SynT is automatically derived as the inverse of the SynC sequence. All other sync sequences are user programmable. Sync detects are reported

with an in-band event IRQ and a code in the AuxData and Analogue Status register ($CC). The FFSK RxRate bit in this register can be read to determine whether the detection was at 1200 or 2400 baud.
After frame synchronisation has been achieved, the following user data is made available in the RxData1 register, along with a DataRdy IRQ indication. In an MPT1327 system, the preceding SYS and CCS codes will also be reported in RxData3 and RxData4 (however, this is dependent on the timing of the signalling, the host should confirm the validity of the data before relying on it).

FFSK may be transmitted in conjunction with a CTCSS or DCS sub-audio component. The device will handle the sub-audio signals as previously described. If a sub-audio signal turns off during reception of FFSK, it is up to the host µC to turn off the decoding as the device will continue receiving and processing the incoming signal until commanded otherwise by the host µC.

The host µC must keep track of the message length or otherwise determine the end of reception (e.g. by using sub-audio information to check for signal presence) and disable the demodulator at the appropriate time.

6.9.2 Transmitting FFSK Signals

When enabled, the modulator will begin transmitting the preamble data (defined in P1.0), followed by the selected sync sequence (defined in P1.0 and selected by b11-8 of the Analogue mode register ($C2). Therefore, these registers should be programmed to the required values before transmission is enabled.
The modulation rate will be determined by the setting of Tx Mode in the FFSK Modem Format field of the Analogue Control register ($C3). Changes to this setting will be not be applied until the next time the modem is enabled. The level of the FFSK signal generated can be controlled using the Audio Tone Tx Level field of the Analogue Control register ($C3).

The device will issue a DataRdy IRQ, which the host should respond to by loading the user data it wishes to transmit.

The device generates its own internal data clock and converts the binary data into the appropriately phased frequencies, as shown in Figure 41 and Table 21. The binary data is taken from Tx Data 1 register ($B6), most significant bit first. The following data words must be provided over the C-BUS in response to the DataRdy IRQ. The end of the FFSK transmission may be indicated to the device by setting the TxData 0 register to $0030, after which the device will indicate that the final data bit has left the chip by raising the TxDone IRQ, after which the host may power-down the RF circuitry and return the device to Idle mode as required.

6.10 Selcall Signalling

The device supports both Selcall and user-programmable in-band tones between 288 Hz and 3000 Hz. Note that if tones below 400 Hz are used, sub-audio signalling should be disabled and the 300 Hz HPF disabled.

By default, the device will load the CCIR Selcall tone set, however this may be over-written by the host with any valid set of tones within its operational range by use of the Programming register. This ensures that the device can remain compatible with all available tone systems in use. The device does not implement automatic repeat tone insertion or deletion: it is up to the host to correctly implement the appropriate Selcall protocol.

Selection of the Selcall mode is performed by bit 10 of the Mode register ($C1). Detection of the selected in-band signalling mode can be performed in parallel with voice reception.

See:

- Mode Control - $C1 write
- TxData 0 - $B5 write
- Aux Data and Analogue Status - $CC read

6.10.1 Receiving and Decoding Selcall Tones

Selcall tones can be used to flag the start of a call or to confirm the end of a call. If they occur during a call the tone may be audible at the receiver. When enabled, an interrupt will be issued when a signal matching a valid in-band tone changes state (i.e. on, off or a change to different tone).

The device implements the EEA tone set. Other addressing and data formats can be implemented by loading the Programming registers with the appropriate values. The frequency of each tone is defined in the Programming registers P4.0 to P4.15

In receive mode the device scans through the tone table sequentially. The code reported will be the first one that matches the incoming frequency and b3 of the IRQ Status register, $C6, will be asserted.
Adjustable decoder bandwidths and threshold levels are programmable via the Programming register. These allow certainty of detection to be traded against signal to noise performance when congestion or range limits the system performance.

Table 22 Selcall Tones

$CC:b15-13 (Rx)	$CC:b12 – 8 (Rx) $B6:b4-0 (Tx)			Freq. (Hz)	Program Register
Binary		Dec	Hex		
100	00000	0	0	1981	P4.0
100	00001	1	1	1124	P4.1
100	00010	2	2	1197	P4.2
100	00011	3	3	1275	P4.3
100	00100	4	4	1358	P4.4
100	00101	5	5	1446	P4.5
100	00110	6	6	1540	P4.6
100	00111	7	7	1640	P4.7
100	01000	8	8	1747	P4.8
100	01001	9	9	1860	P4.9
100	01010	10	A	2400	P4.10
100	01011	11	B	930	P4.11
100	01100	12	C	2247	P4.12
100	01101	13	D	991	P4.13
100	01110	14	E	2110	P4.14
100	01111	15	F	1055	P4.15
100	10000	16	10	Null tone	-
100	11111	31	1F	Unknown tone (Rx only)	-

Notes:
Normally, tone 14 is the repeat tone. This code must be used in transmit mode when the new code to be sent is the same as the previous one. e.g. to send '333' the sequence '3R3' should be sent, where 'R' is the repeat tone. When receiving Selcall tones, the device will indicate the repeat tone when it is received. It is up to the host to interpret and decode the tones accordingly.

6.10.2 Transmitting Selcall Tones

In Tx mode, only one in-band signalling mode may be selected at a time. The Selcall tone to be generated is loaded into the Tx Data 1 register ($B6) using bits 4-0 – see Table 22. The Selcall tone level is set using the Analogue Control register ($C3) b4-0, using the Audio Tone Tx Level field.

6.10.3 Alternative Selcall Tone Sets

These may be loaded via the Programming register to locations P4.0 to P4.15. See section 8.3.5.

Table 23 Alternative Selcall Tone Sets

	Frequency (Hz)				
Tone Number	**EIA**	**EEA**	**CCIR**	**ZVEI 1**	**ZVEI 2**
0	600	1981	1981	2400	2400
1	741	1124	1124	1060	1060
2	882	1197	1197	1160	1160
3	1023	1275	1275	1270	1270
4	1164	1358	1358	1400	1400
5	1305	1446	1446	1530	1530
6	1446	1540	1540	1670	1670
7	1587	1640	1640	1830	1830
8	1728	1747	1747	2000	2000
9	1869	1860	1860	2200	2200
A	2151	1055	2400	2800	885
B	2435	930	930	810	810
C	2010	2247	2247	970	740
D	2295	991	991	885	680
E	459	2110	2110	2600	970
F	NoTone	2400	1055	680	2600

6.11 DTMF Signalling

The device provides both DTMF encode and decode functions using the tone combinations shown in Table 24.

Selection of DTMF mode is performed by bit 9 of the Mode Control register ($C1). Detection of the selected in-band signalling mode can be performed in parallel with voice reception.

6.11.1 Reception and Decoding of DTMF

When a DTMF tone has been detected, b3 of the IRQ Status register ($C6) will be set and the tone code will be available in: Aux Data and Analogue Status - $CC read – see Table 24. This value will over-write any existing in-band tone value that may be present.

6.11.2 Transmission of DTMF

In Tx mode, only one in-band signalling mode may be selected at a time, DTMF is selected by setting b9 in the Mode Control register ($C1). The DTMF signals to be generated are loaded into the Tx Data 1 register ($B6) using bits 3-0 – see Table 24.

Single tone mode ($B6:b4) generates only a single tone of the DTMF pair. The underlined value in Table 24 indicates which of the tones will be generated when this bit is enabled.

The DTMF level is set using the Analogue Control register ($C3) (using the AudioTone Tx Level field) with optional twist set using $B6:b6,5 – see Table 25.

Setting $B6:b7 (No Tone) will mute the output of the DTMF generator. This can be used to generate a pause period between tones, thereby minimising the number of C-BUS writes required when generating a string of DTMF digits.

Table 24 DTMF Tone Pairs

$CC:b15-13 (Rx)	$CC:b12 – 8 (Rx) $B6:b4-0 (Tx)			Freq. Low (Hz)	Freq. High (Hz)
Binary		Key	Hex		
010	00000	D	0	941	1633
010	00001	1	1	697	1209
010	00010	2	2	697	1336
010	00011	3	3	697	1477
010	00100	4	4	770	1209
010	00101	5	5	770	1336
010	00110	6	6	770	1477
010	00111	7	7	852	1209
010	01000	8	8	852	1336
010	01001	9	9	852	1477
010	01010	0	A	941	1336
010	01011	*	B	941	1209
010	01100	#	C	941	1447
010	01101	A	D	697	1663
010	01110	B	E	770	1663
010	01111	C	F	852	1663
010	10000	x	x	Null tone (Rx only)	

Table 25 DTMF Twist

b6,5	Twist - dB
00	0
01	-2
10	-4
11	-6

6.12 Squelch Operation

Many limiter/discriminator chips provide a noise-quieting squelch circuit around an op-amp configured as a filter. This signal is conventionally passed to a comparator to provide a digital squelch signal, which can be

routed directly to one of the CMX7241/7341's GPIO pins or to the host. However with the CMX7241/7341, the comparator and threshold operations can be replaced by one of the AuxADCs with programmable thresholds and hysteresis functions.
See:

- IRQ Status - $C6 read
- 4FSK Modem Configuration - $A1 write

Note: This functionality is not necessary in I/Q mode as squelch detection is executed within the CMX7241/7341 signal processing chain, however the AuxADC functionality remains available.

6.13 GPIO Pin Operation

The CMX7241/7341 provides four GPIO pins: RXENA, TXENA, GPIOA and GPIOB.
RXENA and TXENA are configured to reflect the Tx/Rx state of the Mode register under control of the Tx Sequencer. These lines should be pulled to their inactive state by 47k resistors. This will ensure that the signals are in an inactive state whilst the FI loads, and also allows the FI to determine if they should be driven active high (CMX994 compatible) or active low (for backwards compatibility with the 7141 series).

Note that RXENA and TXENA will not change state until the relevant mode change has been executed by the CMX7241/7341. This is to allow the host sufficient time to load the relevant data buffers and the CMX7241/7341 time to encode the data required prior to its transmission. There is thus a fixed time delay between the GPIO pins changing state and the data signal appearing at the MOD output pins. During the power-on sequence (until the FI has completed its load sequence) these pins have only a weak pull-up applied to them, so care should be taken to ensure that any loading during this period does not adversely affect the operation of the unit.

GPIOA and GPIOB can either be used as serial clock and data signals when separate serial ports are required (see Section 4.4 Serial Port Interfaces), can be host programmable for input or output, or can be assigned as part of the Tx sequencer operation (CMX7241 only). The mode for each pin is set in Program block 6.0.

The default state is input, high level. When set for input, the values can be read back using the Modem Status register, $C9. In output mode the value for the GPIO pin is written via the Aux Function Control register, $A8.
The GPIOA and GPIOB functions can also be relocated to use the SYSCLK1 and SYSCLK2 pins. This allows the GPIOA or GPIOB functionality to still be used while the alternate SPI configuration is selected.

6.14 Auxiliary ADC Operation

The inputs to the two auxiliary ADCs can be independently routed from any of the signal input pins under control of the AuxADC Control register, $93. Conversions will be performed as long as a valid input source is selected. To stop the ADCs, the input source should be set to 'off'. Register $C0, b6, BIAS, must be enabled for auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the AuxADC Control register, $93, the length of the averaging is determined by the value in the AuxADC Control register, $93, and defaults to a value of 0. This is a rolling average system such that a proportion of the current data will be added to the last average value.

For an average value of:

0 = 50% of the current value will be added to 50% of the last average value
1 = 25% of the current value will be added to 75% of the last average value
= 12.5% etc.
7 = 0.78125% of input sample + 99.21875% of saved average

The maximum useful value of this field is 7.

High and Low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated the first time a rising edge passes the High threshold or a falling edge passes the Low threshold, see Figure 42. A high threshold IRQ re-arms the low threshold interrupt and vice-versa. The thresholds are programmed using $94-$97. See Figure 42.

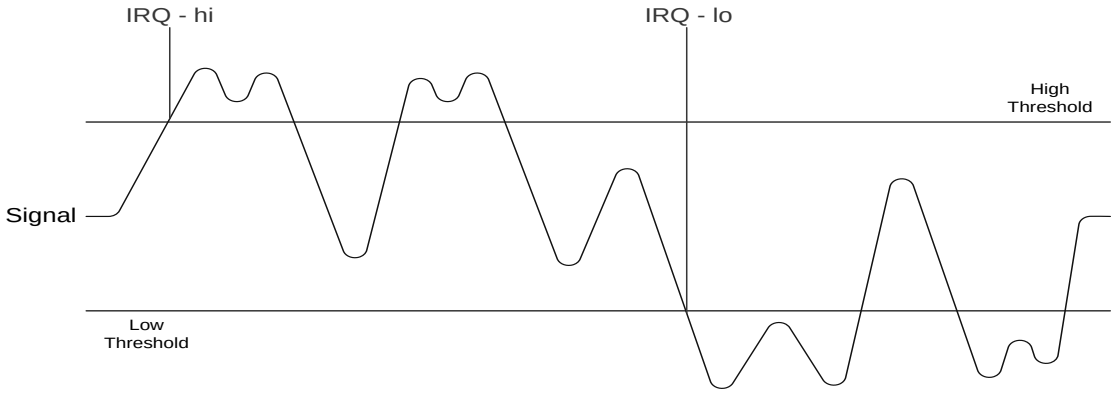


Figure 42 AuxADC IRQ Operation

Auxiliary ADC data is read back in the Aux 1 Data registers ($A9 and $AA) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

See:

- Aux Config - $CD write
- AuxADC1 and 2 Data - $D6 and $D7 read

6.15 Auxiliary DAC/RAMDAC Operation

The three auxiliary DAC channels are programmed via the AuxDAC Data registers, $30 to $33. (Note that AuxDAC channel 1 is allocated to the RAMDAC which will automatically output a pre-programmed profile at a programmed rate under control of the Tx Sequencer. The default profile is a raised cosine (see Table 31, but this may be over-written with a user-defined profile by writing to Programming register P7.0-63. The gain of the profile may be adjusted by writing to the RAMDAC Attenuator ($84) and a fixed offset may be applied using the RAMDAC Offset ($85).

The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to Idle or Rx mode whilst the RAMDAC is still ramping. An external R-C network may be required to remove any “step” noise from the output.

The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero. Updating an AuxDAC is performed by writing to the relevant AuxDAC register ($30-$33), however care should be taken to ensure that the AuxDAC is not currently in use by other functions (e.g RAMDAC, tone gen) as access will not be possible until the function is disabled. Any writes during this time will be discarded. On disabling RAMDAC or tone generator mode the previous enable state and level will be automatically restored by the AuxDAC.

See:

- Aux Function Control - $A8 write.
- AuxDAC1-4 Data - $30 to $33 write

6.16 Digital System Clock Generators

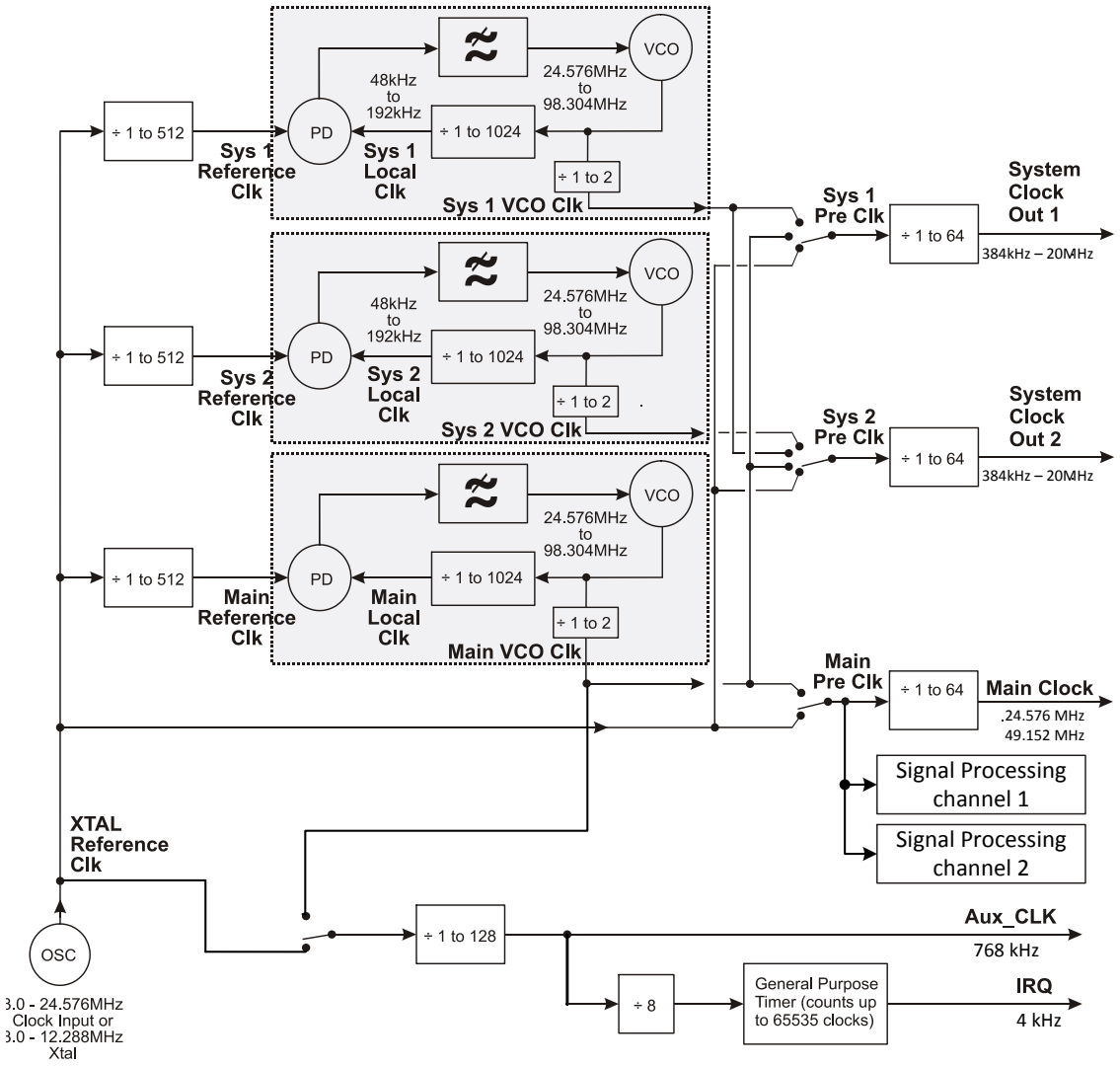


Figure 43 Digital Clock Generation Schemes

The CMX7241/7341 includes a two-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in Section 4.1 or the XTAL input can be driven by an externally generated clock. The crystal (Xtal) source frequency can go up to 12.288MHz (clock source frequency up to 24.576MHz), but a 19.2MHz oscillator is assumed by default for the functionality provided in the CMX7241/7341.

6.16.1 Main Clock Operation

A digital PLL is used to create the Main Clock (nominally 24.576MHz in Tx, 49.152MHz in Rx) for the internal sections of the CMX7241/7341. At the same time, other internal clocks are generated by division of either the XTAL Reference Clock or the Main Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters, running a General Purpose (GP) Timer and the signal

processing block. In particular, it should be noted that in Idle mode the setting of the GP Timer divider directly affects the C-BUS latency (with the default values this is nominally 250µs).

The CMX7241/7341 defaults to the settings appropriate for a 19.2MHz oscillator, however if other frequencies are to be used then the Program Block registers P3.13 to P3.21 will need to be programmed appropriately at power-on. This flexibility allows the device to re-use an external clock source, so reducing total cost and potential noise sources. A table of common values is provided in Table 8.

See:

- Block 3: Tx Sequencer and Clock Settings
- System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. These are digital phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a reference frequency of 96kHz. If not required, these clocks can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 43. Note that at power-on, SYSCLK1 will be active, directly coupled to the XTALIN signal..

See:

- SYSCLK 1 and SYSCLK 2 PLL Data - $AB, $AD write
- SYSCLK 1 and SYSCLK 2 REF - $AC, $AE write.

6.17 Signal Level Optimisation

The internal signal processing of the CMX7241/7341 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) - (2 x 0.3V)] Volts pk-pk = 838mV rms, assuming a sine wave signal. This should not be exceeded at any stage.

6.17.1 Transmit Path Levels

For the maximum signal out of the MOD1 and MOD2 attenuators, the signal level at the output of the Modem block is set to be 0dB, The MOD1 and MOD2 Fine Level Control ($801) has a maximum attenuation of 1.8dB and no gain, whereas the Analogue Output Gain ($B0) has a variable attenuation of up to +40.0dB and no gain.

[1] Note that C-BUS register $80 is an 8-bit register.

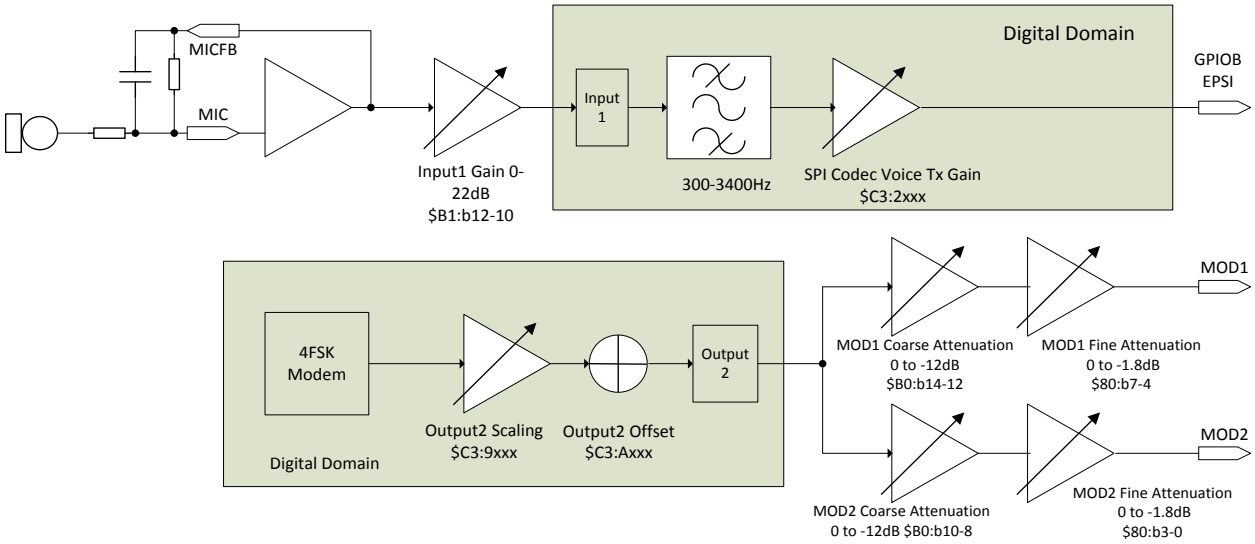


Figure 44 Tx Levels

6.17.2 Receive Path Levels

The Coarse Input adjustment ($B1) has a variable gain of up to +22.4dB and no attenuation. In LD mode with the lowest gain setting (0dB), the maximum allowable input signal level at the DISCFB pin would be 838mV rms. This signal level is an absolute maximum, which should not be exceeded.

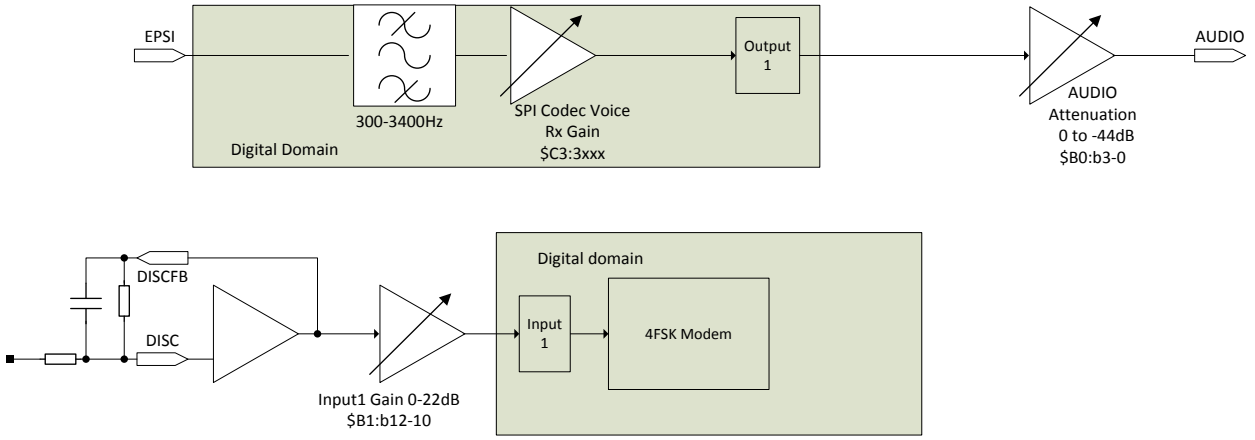
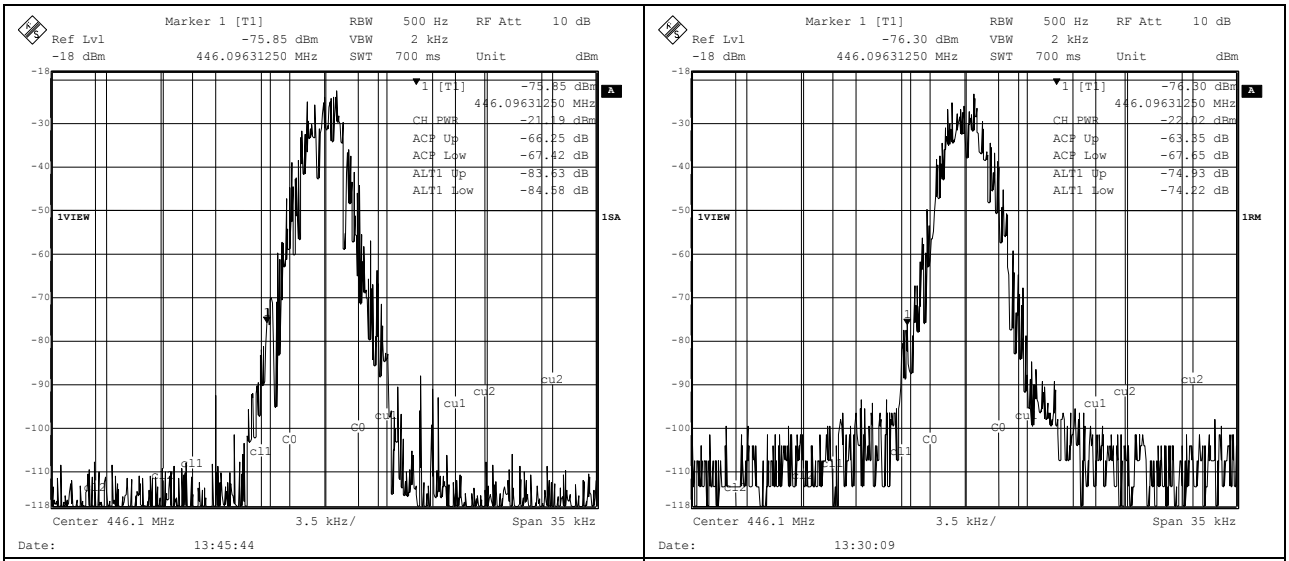


Figure 45 Rx Levels (LD mode)

In I/Q mode CMX7241/7341 automatically manages the gain control settings to optimise signal levels.

6.18 Tx Spectrum Plots

The following figure shows the Tx spectrum when using a suitable signal generator as measured on a spectrum analyser using the CMX7241/7341 internal PRBS generator. Note that the I/Q mode is sensitive to variations in dc offset in the modulation path and these must be minimised.



Two-point Modulation Spectrum	I/Q Modulation Spectrum

Figure 46 Tx Modulation Spectra – 4.8kbps

7 Performance Characteristics

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD}- DV_{SS}	−0.3	4.0	V
AV_{DD}- AV_{SS}	−0.3	4.0	V
Voltage on any pin to DV_{SS}	−0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	−0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding BIAS) (i.e. VDEC, AVDD, AVSS, DVDD, DVSS)	−30	+30	mA
Current into or out of any other pin	−20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD}	0	0.3	V
DV_{SS} and AV_{SS}	0	50	mV

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1600	mW
... Derating	–	16	mW/°C
Storage Temperature	−55	+125	°C
Operating Temperature	−40	+85	°C

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at T_{AMB} = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	−55	+125	°C
Operating Temperature	−40	+85	°C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
$DV_{DD} – DV_{SS}$		3.0	3.6	V
$AV_{DD} – AV_{SS}$		3.0	3.6	V
$V_{DEC} – DV_{SS}$	2	1.70	1.90	V
Operating Temperature		–40	+85	°C
XTAL/CLK Frequency (using an Xtal)	1	3.0	12.288	MHz
XTAL/CLK Frequency (using an external clock)	1	3.0	24.576	MHz

Notes: 1 Figures here represent the capability of the device. For use with this FI, however, an external CLK of 19.2MHz is required.

2 The V_{DEC} supply is automatically derived from DV_{DD} by the on-chip voltage regulator.

7.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2 and Figure 3. Maximum load on digital outputs = 30pF.

Oscillator Frequency = 19.2MHz ±0.01% (100ppm); T_{AMB} = −40°C to +85°C

$AV_{DD} = DV_{DD}$ = 3.0V to 3.6V

V_{DEC} = 1.8V

Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V

Signal levels track with supply voltage, so scale accordingly

Signal to Noise Ratio (SNR) in bit rate bandwidth

Input stage gain = 0dB. Output stage attenuation = 0dB

Current consumption figures quoted in this section apply to the device when loaded with 7241/7341FI-1.x only. The use of other CMX7241/7341 Function Images can modify the current consumption of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD}		–	8	100	µA
AI_{DD}		–	4	20	µA
Idle Mode	22				
DI_{DD}		–	1.4	–	mA
AI_{DD}	23	–	1.6	–	mA
Rx Mode (LD Mode)	22				
DI_{DD} (4.8kbps – search for FS)		–	4.7	–	mA
DI_{DD} (4.8kbps – FS found)		–	2.8	–	mA
AI_{DD}		–	1.6	–	mA
Rx Mode (I/Q Mode)	22				
DI_{DD} (4.8kbps – search for FS)		–	10.2	–	mA
DI_{DD} (4.8kbps – FS found)		–	7.4	–	mA
AI_{DD}		–	6.9	–	mA
Tx Mode	22				
DI_{DD} (4.8kbps – two-point)		–	4.3	–	mA
DI_{DD} (4.8kbps – I/Q)		–	5.4	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	1.5	–	mA

Additional Current for each Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 1.8V)		–	250	–	µA
Additional Current for each Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 1.8V)		–	50	–	µA
Additional Current for each Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA

Notes:

21 T_{AMB} = 25°C: not including any current drawn from the device pins by external circuitry.

22 System Clocks: auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled.

23 May be further reduced by power-saving unused sections

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input	24				
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		−40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Leakage Current (Logic 1 or 0)		−1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic 1 (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic 0 (I_{OL} = -5mA)		–	–	10%	DV_{DD}
'Off' State Leakage Current		–	–	10	µA
IRQN (Vout = DV_{DD})		−1.0	–	+1.0	µA
REPLY_DATA (output HiZ)		−1.0	–	+1.0	µA
V_{BIAS}	25				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	22	–	kΩ

Notes:

24 Characteristics when driving the XTAL/CLK pin with an external clock source.

25 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.

AC Parameters			Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input							
'High' Pulse Width			31	15	–	–	ns
'Low' Pulse Width			31	15	–	–	ns
Input Impedance (at 6.144MHz)							
	Powered-up	Resistance		–	150	–	kΩ
		Capacitance		–	20	–	pF
	Powered-down	Resistance		–	300	–	kΩ
		Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)				–	20	–	ms
System Clk 1/2 Outputs							
XTAL/CLK input to CLOCK_OUT timing:							
	(in high to out high)		32	–	15	–	ns
	(in low to out low)		32	–	15	–	ns
'High' Pulse Width			33	76	81.38	87	ns
'Low' Pulse Width			33	76	81.38	87	ns
V_{BIAS}							
Start-up Time (from powersave)				–	30	–	ms
Microphone, Alternate and Discriminator Inputs (MIC, ALT, DISC)							
Input Impedance			34	–	>10	–	MΩ
Maximum Input Level (pk-pk)			35	–	–	80%	AV_{DD}
Load Resistance (feedback pins)				80	–	–	kΩ
Amplifier Open Loop Voltage Gain		⎫					
(I/P = 1mVrms at 100Hz)		⎭		–	80	–	dB
Unity Gain Bandwidth				–	1.0	–	MHz
Programmable Input Gain Stage			36				
Gain (at 0dB)			37	−0.5	0	+0.5	dB
Cumulative Gain Error		⎫					
(wrt attenuation at 0dB)		⎭	37	−1.0	0	+1.0	dB

Notes:

31 Timing for an external input to the XTAL/CLK pin.

32 XTAL/CLK input driven by an external source.

33 6.144MHz XTAL fitted and 6.144MHz output selected (scale for 19.2MHz).

34 With no external components connected, measured at DC.

35 Centred about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: DISCFB, ALTFB or MICFB.

37 Design Value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1/2 and Audio Output (MOD 1, MOD 2, AUDIO)					
Power-up to Output Stable	41	–	50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error ⎫					
(wrt attenuation at 0dB) ⎭		−0.6	0	+0.6	dB
Output Impedance ⎫ Enabled	42	–	600	–	Ω
⎭ Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ
Audio Attenuator					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error ⎫					
(wrt attenuation at 0dB) ⎭		−1.0	0	+1.0	dB
Output Impedance ⎫ Enabled	42	–	600	–	Ω
⎭ Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3V and T_{AMB} = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centred about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (Aux ADC 1 to 4)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10 Bit ADCs					
Resolution		–	10	–	Bits
Maximum Input Level (pk-pk)	54	–	–	80%	AV_{DD}
Conversion Time	52	–	250	–	µs
Input Impedance					
Resistance	57	–	>10	–	MΩ
Capacitance		–	5	–	pF
Zero Error	55	0	–	TBA	mV
Integral Non-linearity		–	–	TBA	LSBs
Differential Non-linearity	53	–	–	TBA	LSBs
Auxiliary 10 Bit DACs					
Resolution		–	10	–	Bits
Maximum Output Level (pk-pk), no load	54	80%	–	–	AV_{DD}
Zero Error	56	0	–	TBA	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	TBA	LSBs
Differential Non-linearity	53	–	–	TBA	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure <1 bit additional error under nominal conditions.

52 With an auxiliary clock frequency of 6.144MHz.

53 Guaranteed monotonic with no missing codes.

54 Centred about $AV_{DD}/2$.

55 Input offset from a nominal V_{BIAS} input, which produces a $0200 ADC output.

56 Output offset from a $0200 DAC input, measured with respect to nominal V_{BIAS} output.

57 Measured at dc.

7.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in Figure 2. Maximum load on digital outputs = 30pF.

Oscillator Frequency = 19.2MHz ±0.01% (100ppm); T_{AMB} = −40°C to +85°C.

AV_{DD} = DV_{DD} = 3.0V to 3.6V. Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.

Signal levels track with supply voltage, so scale accordingly.

Signal-to-Noise Ratio (SNR) in bit rate bandwidth.

Input stage gain = 0dB, Output stage attenuation = 0dB.

All figures quoted in this section apply to the device when loaded with FI-1.0.x only. The use of other CMX7241/7341 Function Images can modify the parametric performance of the device.

dPMR **Modem**	**Notes**	**Min.**	**Typ.**	**Max.**	**Unit**
Modem Symbol Rate		–	2400	–	symbols /s
Modulation			4FSK		
Filter (RC) Alpha		–	0.2	–	
Tx Output Level (MOD1, MOD2, two-point)	60	–	2.88	–	Vpk-pk
Tx Output Level (MOD1, MOD2, I/Q)	60	–	2.20	–	Vpk-pk
Tx Adjacent Channel Power (MOD1, MOD2, prbs)	61, 63	-60	–	–	dB
Rx Co-channel Rejection	61, 63	15	12	–	dB
Rx Input Level		–	–	838	mVrms
Rx Input DC Offset		0.5	–	AV_{DD} - 0.5	V

Notes:

60 Transmitting continuous default preamble.

61 See user manual section 6.18.

62 Measured at baseband – radio design will affect ultimate product performance.

63 For a 6.25kHz/4.8kbps channel.

7.2 C-BUS Timing

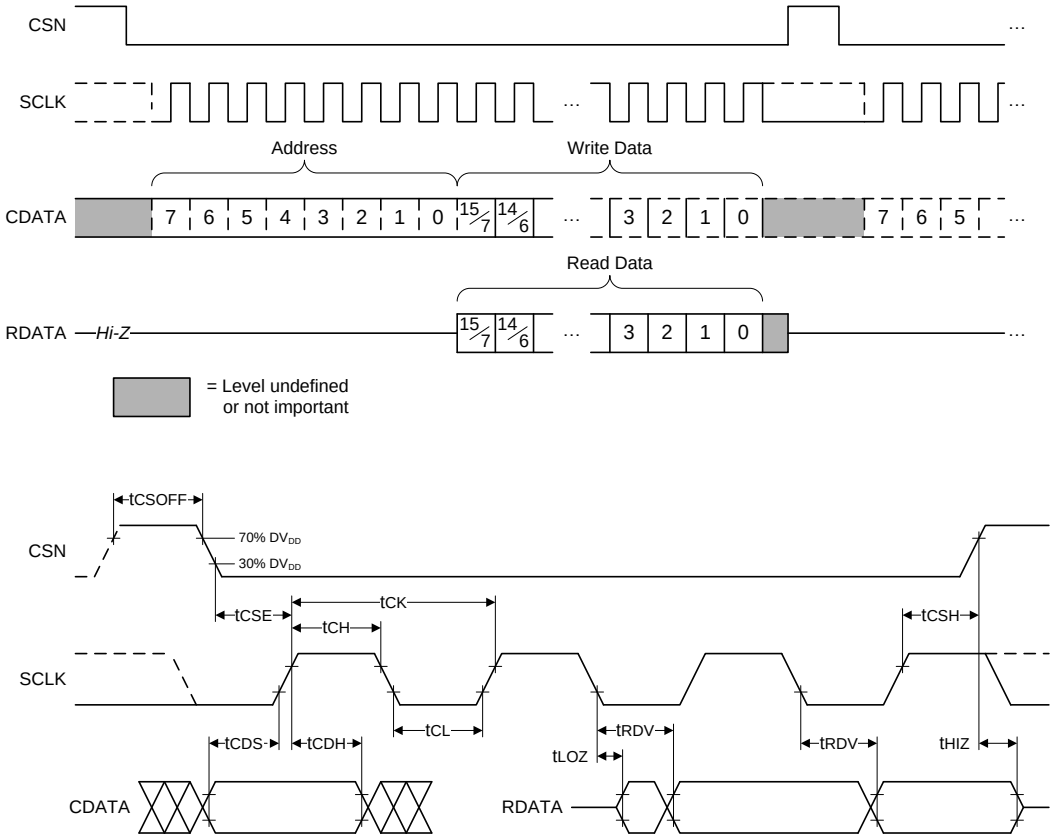


Figure 47 C-BUS Timing

AC Parameters		Notes	Min.	Typ.	Max.	Unit
C-BUS Timing						
Input pin rise/fall time (10% - 90% of DV_{DD})			–	–	3	ns
Capacitive load on RDATA and IRQN			–	–	30	pF
t_{CSE}	CSN enable to SCLK high time		40	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		40	–	–	ns
t_{LOZ}	SCLK low to RDATA output enable time		0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	30	ns
t_{CSOFF}	CSN high time between transactions		40	–	–	ns
t_{CK}	SCLK cycle time		100	–	–	ns
t_{CH}	SCLK high time		40	–	–	ns
t_{CL}	SCLK low time		40	–	–	ns

t_{CDS}	CDATA setup time		25	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDV}	SCLK low to RDATA valid time		0	–	35	ns

Notes: 1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.

2. Data is clocked into the peripheral on the rising SCLK edge.

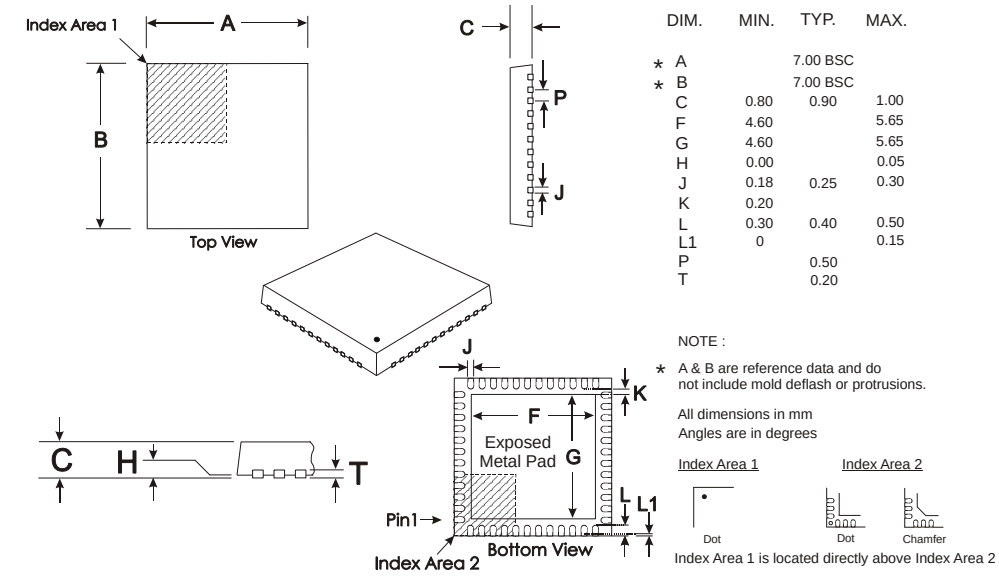
3. Commands are acted upon at the end of each command (rising edge of CSN).

4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.

5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than earlier C-BUS timing specification. The CMX7241/7341 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

7.3 Packaging.



DIM.	MIN.	TYP.	MAX.
* A		7.00 BSC	
* B		7.00 BSC	
C	0.80	0.90	1.00
F	4.60		5.65
G	4.60		5.65
H	0.00		0.05
J	0.18	0.25	0.30
K	0.20		
L	0.30	0.40	0.50
L1	0		0.15
P		0.50	
T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

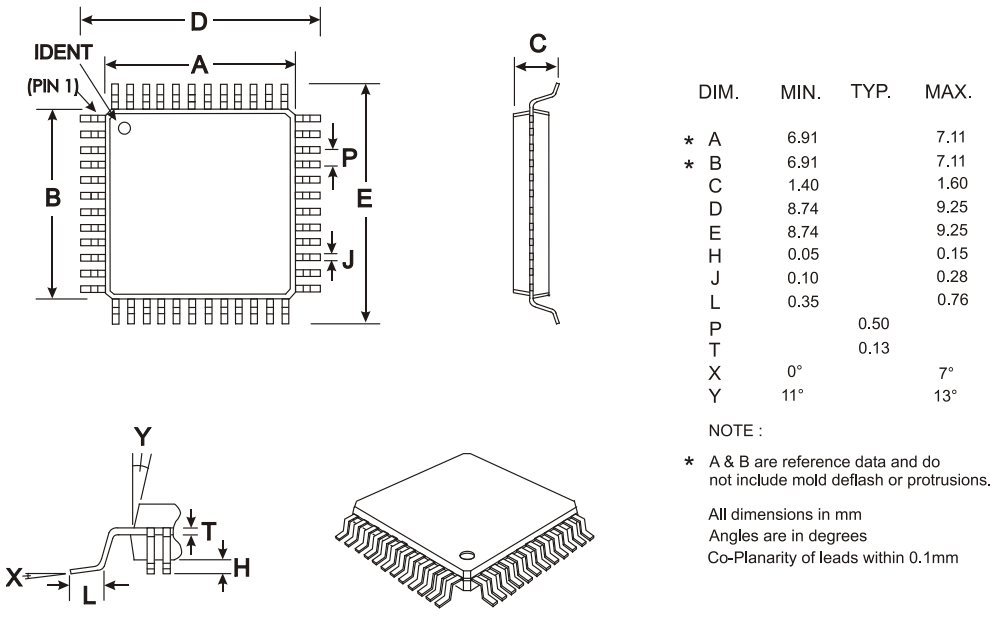
All dimensions in mm
Angles are in degrees

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 48 Mechanical Outline of 48-lead VQFN (Q3)

Order as part no. CMX7241Q3 or CMX7341Q3



DIM.	MIN.	TYP.	MAX.
* A	6.91		7.11
* B	6.91		7.11
C	1.40		1.60
D	8.74		9.25
E	8.74		9.25
H	0.05		0.15
J	0.10		0.28
L	0.35		0.76
P		0.50	
T		0.13	
X	0°		7°
Y	11°		13°

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 49 Mechanical Outline of 48-pin LQFP (L4)

Order as part no. CMX7241L4

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Design Support/Package Information page of the CML website: [www.cmlmicro.com].

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