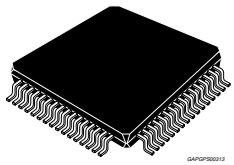
TDA7706

Highly integrated tuner for AM/FM car-radio

Data brief – production data

Features

- FM, AM and weather band reception
- Fully integrated VCO for world tuning
- High performance PLL for fast RDS system
- Integrated AM-LNA and PIN diodes
- Automatic self alignment for FM front-end pre-selection filter and image rejection
- Integrated IF filters with high selectivity, dynamic range and adaptive bandwidth control
- Drift-free Digital-IF signal processing with high performance
- RDS demodulation with group and block synchronization
- High performance stereo decoder with noise-blanker
- Digital interface for HD Radio™ reception with digital audio blending
- Fully programmable DSP core
- I^2C bus-controlled
- I^2S input/output digital audio interfaces
- Single 5 V supply
- LQFP64 package



LQFP64

Description

The TDA7706 highly integrated tuner is a high/performance AM/FM tuner IC for car-radio applications, suitable for HD Radio™ reception.

It contains mixers and IF amplifiers for AM, FM and WX, fully integrated VCO and PLL synthesizer, IF- processing including adaptive bandwidth control, stereo-decoder, RDS decoder, and digital interfaces for external HD Radio™ decoding on a single IC.

AM/FM IBOC or DRM base band filtering is available in parallel to standard analog reception.

The utilization of digital signal processing results in numerous advantages against today's tuners: very low number of external components, very small space occupation and easy application, very high selectivity due to digital filters, high customization possibility through software control, automatic alignment and a powerful DSP for custom processing.

Table 1. Device summary

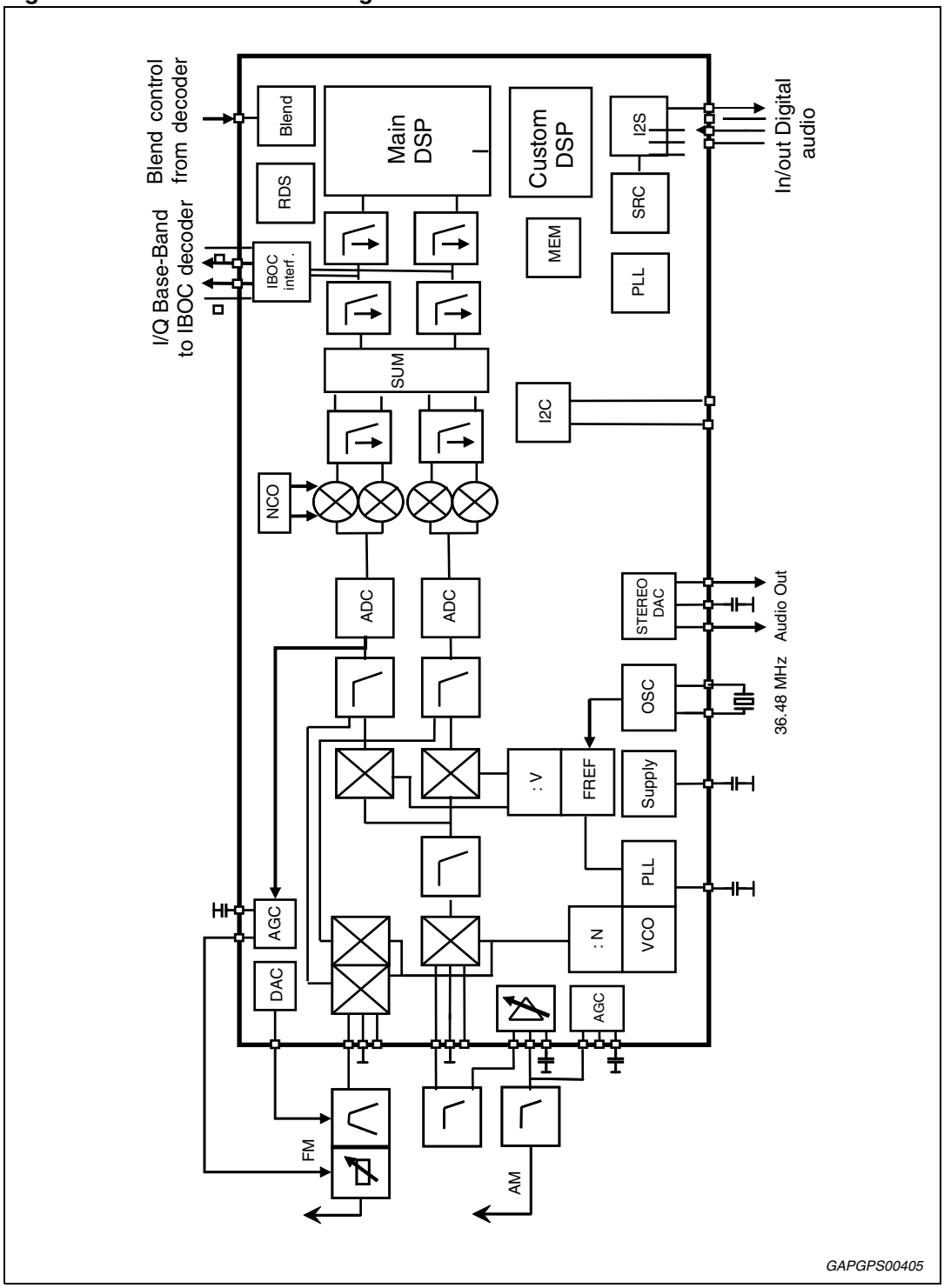
Order code	Package	Packing
TDA7706CB	LQFP64 (10x10x1.4mm)	Tray

Contents

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Functional block diagram



1.2 Pin description

Figure 2. Pin connection (top view)

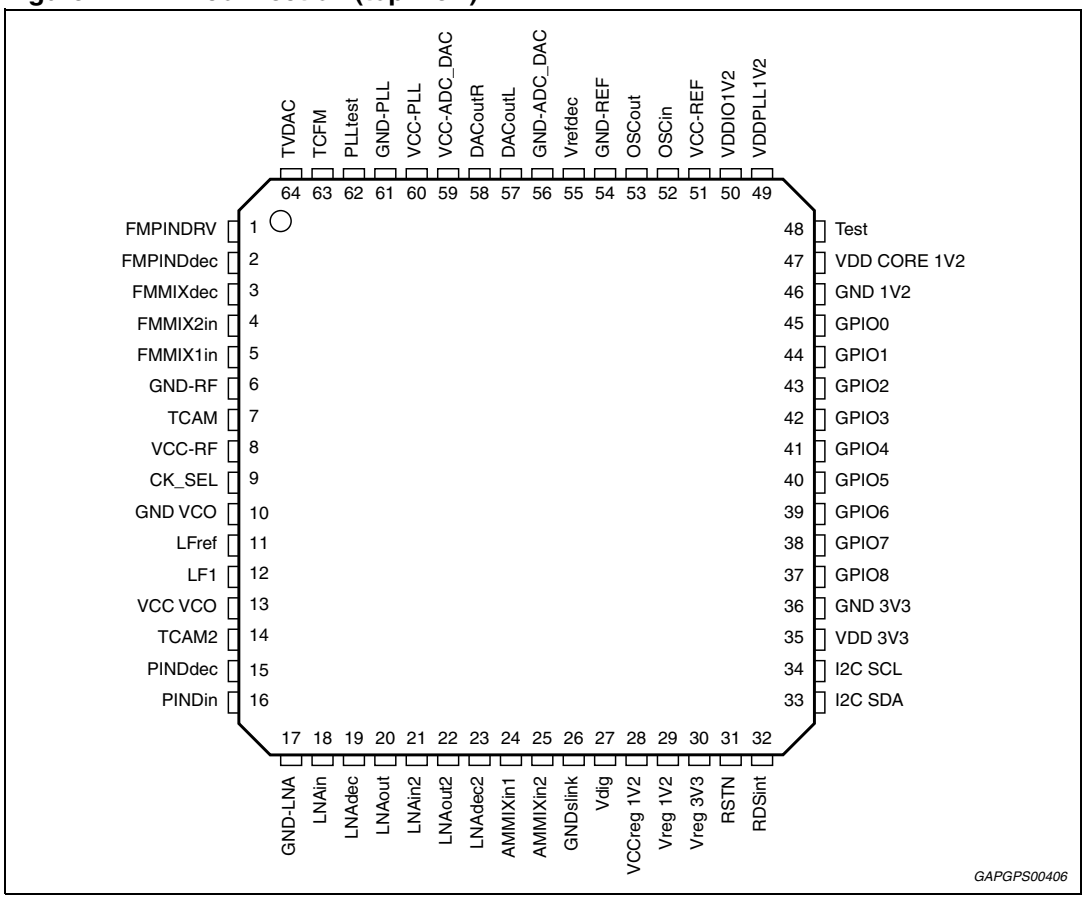


Table 2. Pin description

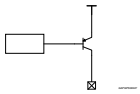
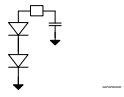
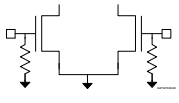
Pin	Pin name	I/O	Function	Description	Equivalent circuit
1	FMPINDRV	Out	FM	FM PIN diode driver output	
2	FMPINDdec	In		Integrated FM PINdiode decoupling	
3	FMMIXdec	-		FM RF signal ground	
4	FMMIXin2	In		FM mixer input 2	
5	FMMIXin1	In		FM mixer input 1	
6	GNDRF	-	-	RF power ground	-

Table 2. Pin description (continued)

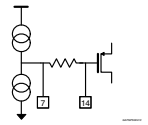
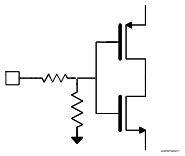
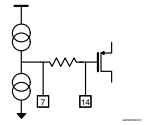
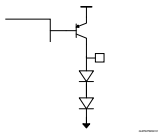
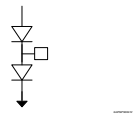
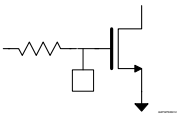
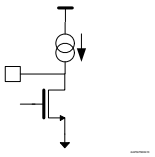
Pin	Pin name	I/O	Function	Description	Equivalent circuit
7	TCAM	-	-	AM AGC time constant	
8	VCCRF	In	-	RF 5V supply	-
9	CK_SEL	In	-	Master/Slave clock operation select	
10	GNDVCO	-	VCO	VCO ground	-
11	LFref	-		Loop filter reference	-
12	LF1	-		Loop filter output	-
13	VCCVCO	In		VCO 5V supply	-
14	TCAM2	-		AM AGC 2nd order time constant	
15	PINDdec	-	AM pin diode	AM AGC internal PIN diode decoupling	
16	PINDin	-		AM AGC internal PIN diode input	
17	GNDLNA	-	AM LNA	AM LNA ground	-
18	LNAin	In		AM LNA input	
19	LNAdec	-		AM LNA decoupling	
20	LNAout	Out		AM LNA output	-
21	LNAin2	-		AM LNA input 2nd stage	-

Table 2. Pin description (continued)

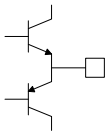
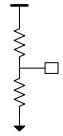
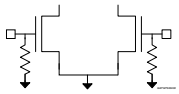
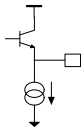
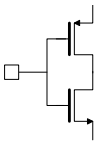
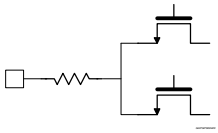
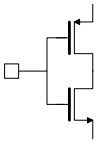
Pin	Pin name	I/O	Function	Description	Equivalent circuit
22	LNAout2	-	AM LNA	AM LNA output 2nd stage	
23	LNAdec2	-		AM LNA decoupling 2nd stage	
24	AMMIXin1	In	AM mixer inputs	AM mixer input 1	
25	AMMIXin2	In		AM mixer input 2	
26	GNDSLINK	-	Supply, ground and reset	Internal inter-IC communication bus ground	-
27	Vdig	In		Front-end digital 5 V supply	-
28	VCCreg1V2	In		Internal 1.2 V regulator 5 V supply	-
29	REG1V2	Out		Internal 1.2 V regulator output	
30	Vreg3v3	Out		Internal 3.3 V regulator output	
31	RSTN	In		Reset (low active) Pull-up 50 kΩ to 3.3 V IO supply	
32	RDSint	Out		RDS interrupt output Pull-down 50 kΩ to ground	-
33	I2CSDA	In/Out	I2C interface	I2C bus data Pull-up 50 kΩ to 3.3 V IO supply	
34	I2CSCL	In		I2C bus clock Pull-up 50 kΩ to 3.3 V IO supply	
35	VDD3V3	In	-	IO ring (3.3V) supply	-
36	GND3V3	-	-	IO ring (3.3V) supply	-

Table 2. Pin description (continued)

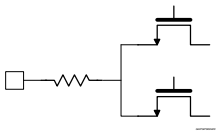
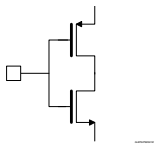
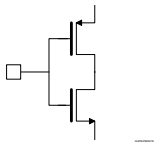
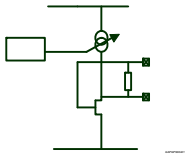
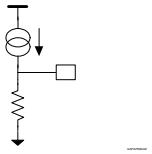
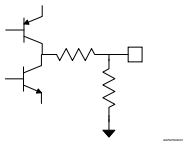
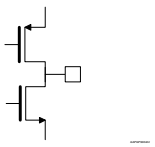
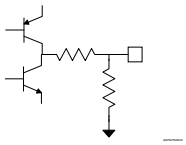
Pin	Pin name	I/O	Function	Description	Equivalent circuit
37	GPIO8	In/Out	HD Radio connectivity/ Audio output I2S interface	SAI clk Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
38	GPIO7	In/Out		Audio SAI word-select Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
39	GPIO6	In/Out		Audio SAI data-output Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
40	GPIO5	In/Out		Audio SAI data-input Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
41	GPIO4	In/Out		SAI Base-Band clock Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
42	GPIO3	In/Out		SAI Base-Band word-select Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
43	GPIO2	Out		SAI Base-Band I data Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
44	GPIO1	Out		SAI Base-Band Q data Pull-down 50 kΩ to ground, SINE_3V3_LIN pad	
45	GPIO0	In		HD blend Pull-down 50 kΩ to ground	
46	GND1V2	-	-	DSP core ground	-
47	VDD core 1V2	In	-	DSP core 1.2V supply	-
48	Test	In	-	Test Mode Pull-down 50 kΩ to ground	
49	VDDPLL1V2	In	-	Digital PLL 1.2 V supply	-
50	VDDIO1V2	In	-	Internal inter-IC communication 1.2V supply	-
51	VCC-REF	In	-	Front-end reference frequency and regulator 5 V supply	-

Table 2. Pin description (continued)

Pin	Pin name	I/O	Function	Description	Equivalent circuit
52	OSCin	In	Oscillator	Crystal oscilllator input	-
53	OSCout	Out		Crsystal oscillator output	
54	GND-REF	-	-	Front-end reference frequency and regulator ground	-
55	Vrefdec	-	-	3.3 V Bias generation decoupling	
56	GND-ADC_DAC	-	DAC	IFADC and audio DAC ground	-
57	DACoutL	Out		Audio output left	
58	DACoutR	Out		Audio output right	
59	VCC-ADC_DAC	In		IFADC and audio DAC 5V supply	-
60	VCC-PLL	In	PLL	Tuning PLL 5V supply	-
61	GND-PLL	-		Tuning PLL ground	-
62	PLLtest	Out		PLL Test output	
63	TCFM	-	-	FM AGC time constant	
64	TVDAC	Out	-	Tuning voltage output	-

2 Function description

2.1 FM - mixers

The FM Image Rejection mixer has two single ended inputs, selectable through software. They are designed for achieving best performance both in case of a passive tuned preselection and for a passive fixed band-pass preselection without tuning for lower cost applications.

The input frequency is down-converted to very low IF with high image rejection.

The tuned application is supported by an 8-bit tuning DAC. The alignment of the DAC is performed automatically on-chip.

2.2 FM - AGC

The programmable RFAGC senses the mixer input to avoid overload.

When the RFAGC threshold is reached, the PIN diode output is activated in order to attenuate the incoming RF signal

The PIN diode driver is able to drive external PIN diodes with up to 15 mA current.

The time constant of the FM AGC is defined by the combination of an external capacitor and internal currents. There are two programmable attack and decay time constants.

2.3 AM - LNA

The integrated AM LNA feature is integrated with low-noise and high IIP2 and IIP3. The gain of the LNA is controlled by the AGC. The maximum gain is set with an external resistor, typically 26 dB with 470 ohm.

2.4 AM - AGC

The programmable AM RFAGC senses the mixer inputs and controls the internal PIN diodes and LNA gains.

Firstly the LNA gain is reduced by about 10d B, and then the PIN diodes are activated to further attenuate the signal.

The time constant of the 2^{nd} order AM AGC LPF is defined by both external components and programmable internal currents.

2.5 AM - Mixers

The image rejection mixer has two AM inputs selectable via software. It easily supports low-cost applications for extended frequency bands like short-waves.

The input frequency is converted to low IF with high image rejection.

2.6 IF A/D converters

A high performance IQ-IFADC converts the IF signal to the digital domain for subsequent digital signal processing.

Two fully differential, continuous-time Sigma-Delta ($\Sigma\Delta$) IF-ADCs are used for both the'I' path and the 'Q' path. For each IFADC, two fully differential input nodes are fed with an input signal having a bandwidth up to 325 kHz. This fully differential design provides good suppression of even-order harmonics. For complex filtering, the input signals of the 'I' path and the 'Q' path have a 90 degree phase shift. The IFADC sampling frequency is 36.48 MHz.

2.7 Audio D/A converters

A CD-quality (>100dB DR) stereo DAC provides the left/right audio signals after IF processing and stereo-decoding by the DSP. In presence of an external HD Radio decoder the DAC outputs the high quality audio resulting from the decoding of the HD Radio transmissions.

2.8 VCO

The VCO is fully integrated without any external tuning component. It covers all the FM frequency bands including EU, US, Japan, East-Europe, Weather-Band and the AM-bands including LW, MW and SW. Its center frequency is approximately 2.7 GHz.

2.9 PLL

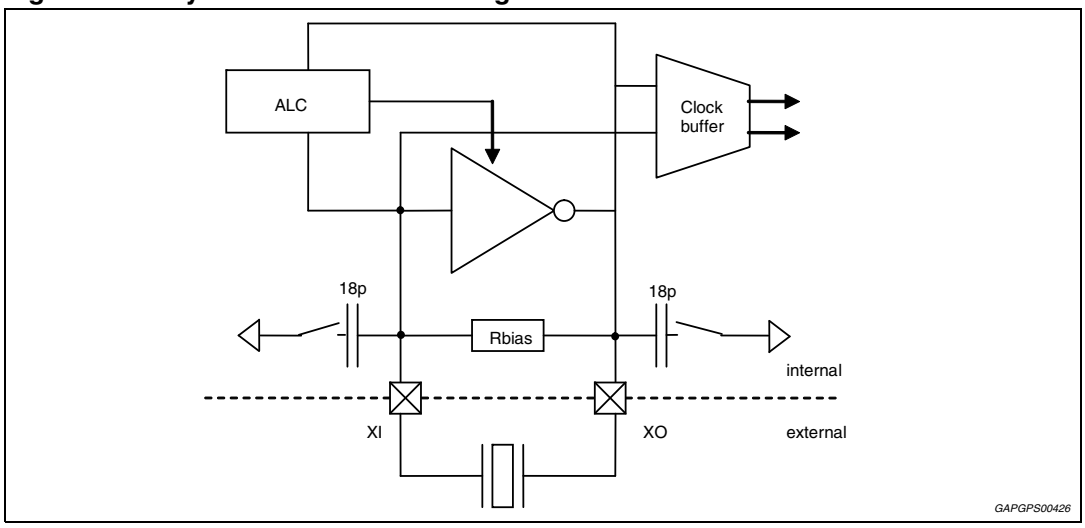
2.9.1 Tuner PLL

The very high-speed tuning PLL is able to settle within about 100 µs for fast RDS applications. The frequency step can be as low as 5 kHz in FM and 500 Hz in AM.

2.10 Crystal oscillator

The device works with a 36.48 MHz fundamental tone crystal. The oscillator block diagram is shown in *Figure 3*. On the PCB the crystal must be connected as close as possible to the chip oscillator input and output pins of the chip. The internal load capacitance together with pin and pad capacitance is optimized for fundamental tone crystal units at 36.48MHz. It is not recommended to put any additional external load capacitors. By suitably configuring pin #9 (CK_SEL), the device can be operated as either a clock master or a clock slave. If pin 9 is left open or tied to GND, the device is configured as clock master (typical operation mode). In case the device is configured as clock slave, pin 9 needs to be connected to 5V. Then the crystal oscillator is switched off and the device expects a crystal equivalent signal on the OSCout/OSCin pins.

Figure 3. Crystal oscillator block diagram



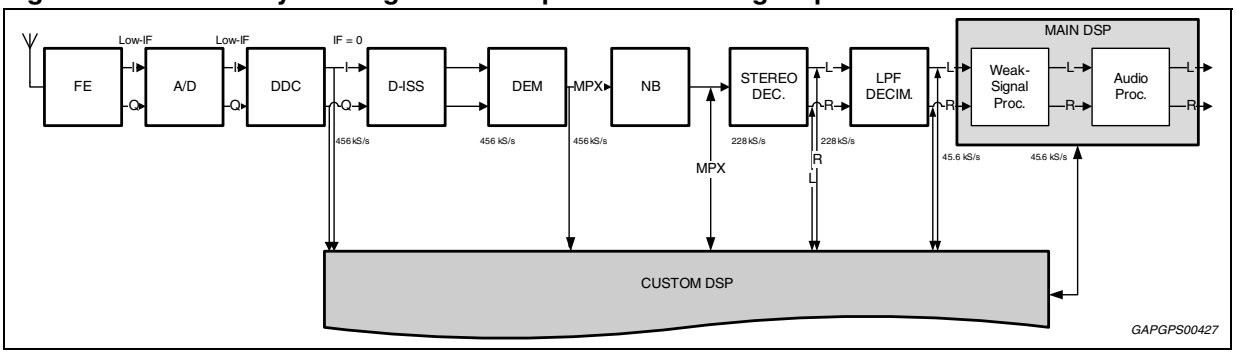
2.11 DSP

The TDA7706 embeds two DSP cores for high computational power and achievable customization. The first DSP and its hardware accelerators take care of all the tuner digital signal processing. The main program is fixed in ROM. Control parameters are copied to RAM and they are accessible and modifiable there, thus allowing a parametric performance optimization. The first DSP core performs:

- digital down-conversion of IF
- bandwidth selection with variable controlled bandwidth
- FM and AM noise blanking
- FM/AM demodulation with soft-mute, high-cut, weak signal processing and quality detection
- FM stereo decoding with stereo-blend
- RDS demodulation including error correction and block synchronization with generation of an RDS interrupt for the main µP
- Autonomous control of RDS-AF tests
- Self-alignment of pre-selection tuning

The second DSP is totally free for custom processing implementation. The second (customizable DSP) can interact with the main DSP by tapping the signal at the access points as shown in the *Figure 4* below.

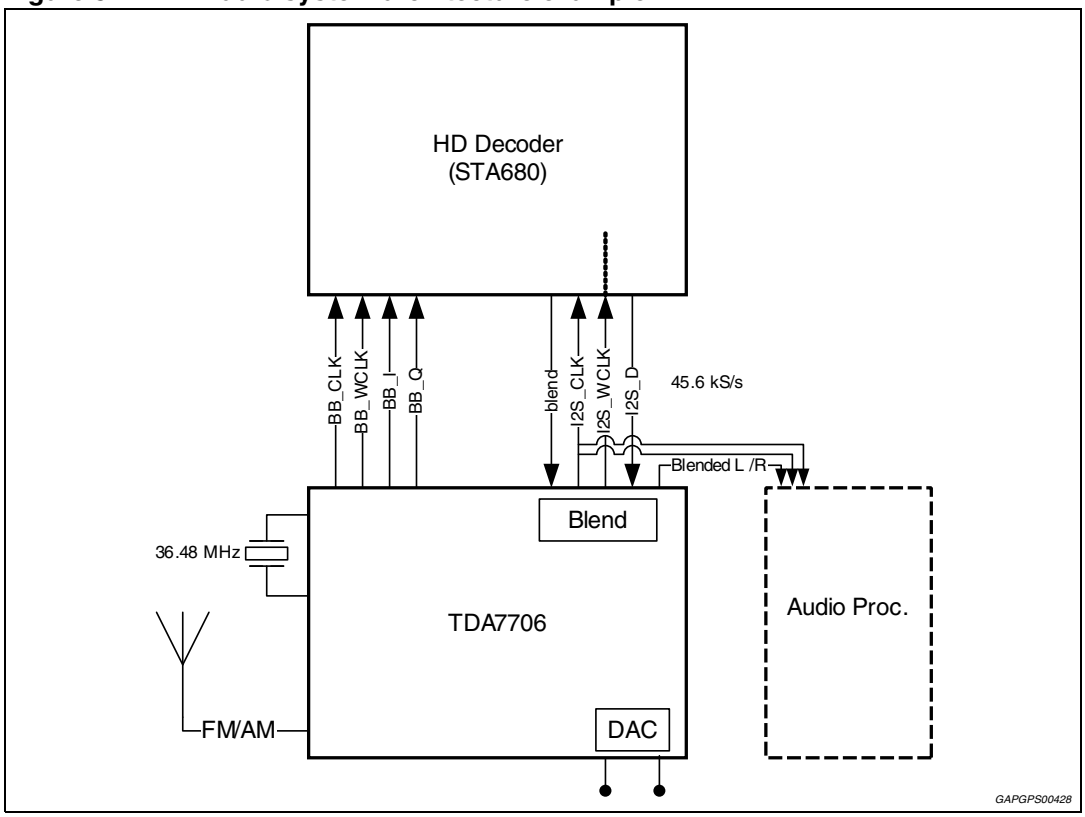
Figure 4. Secondary DSP signal access points in main signal path



2.12 HD Radio connectivity

The HIT2 complies with HD Radio interface specifications as per Ibiquity's "RX_SSS_1108 HD Radio power efficient RF-IF and peripheral processing (power RIPP) specification", thus providing an external HD Radio decoder with I/Q base-band signals and receiving the decoded digital audio from it, as shown in *Figure 5*.

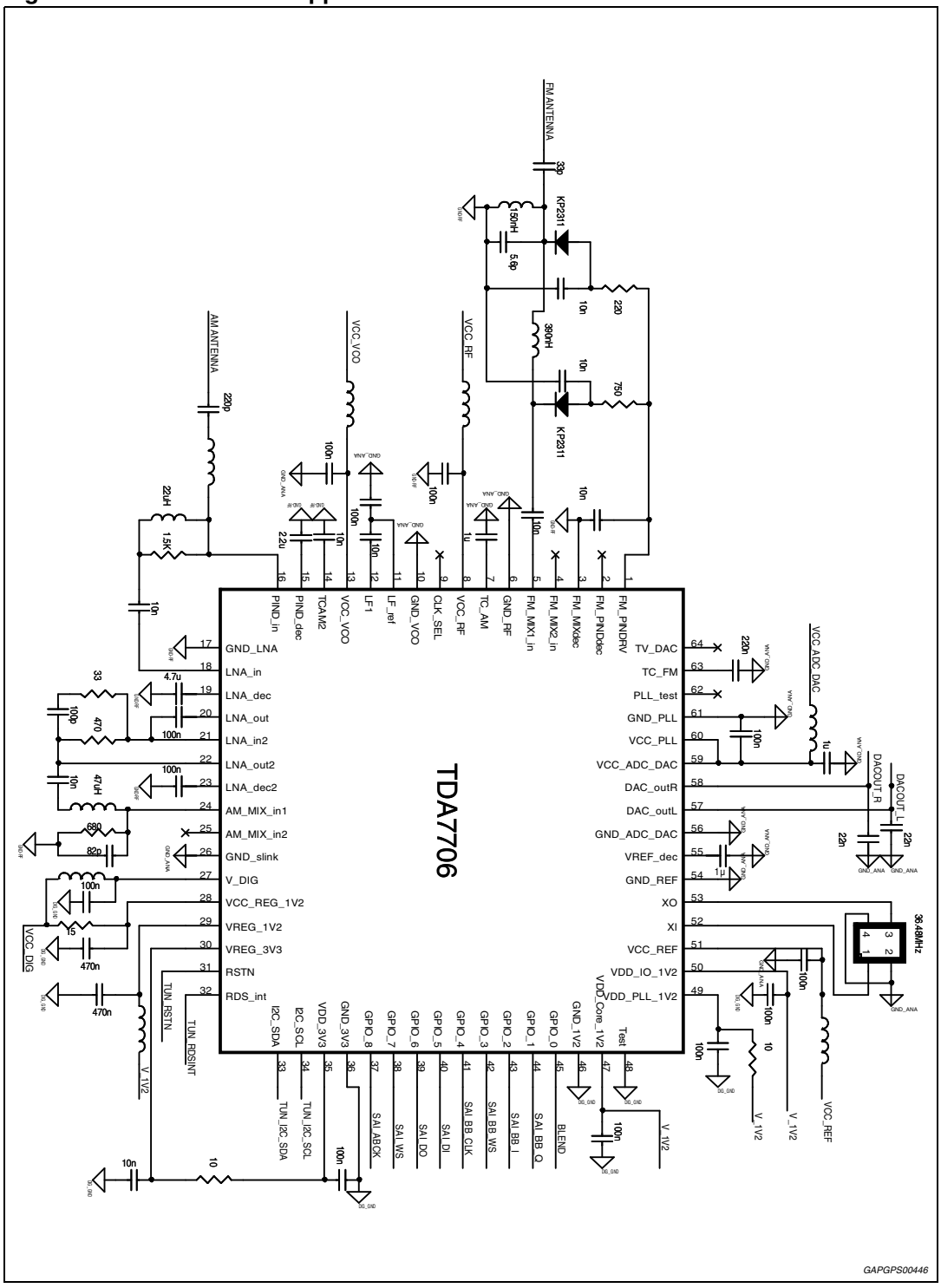
Figure 5. HD Radio system architecture example



3 Application schematics

3.1 Basic application schematic

Figure 6. FM wide-band application



4 Package information

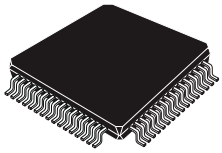
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

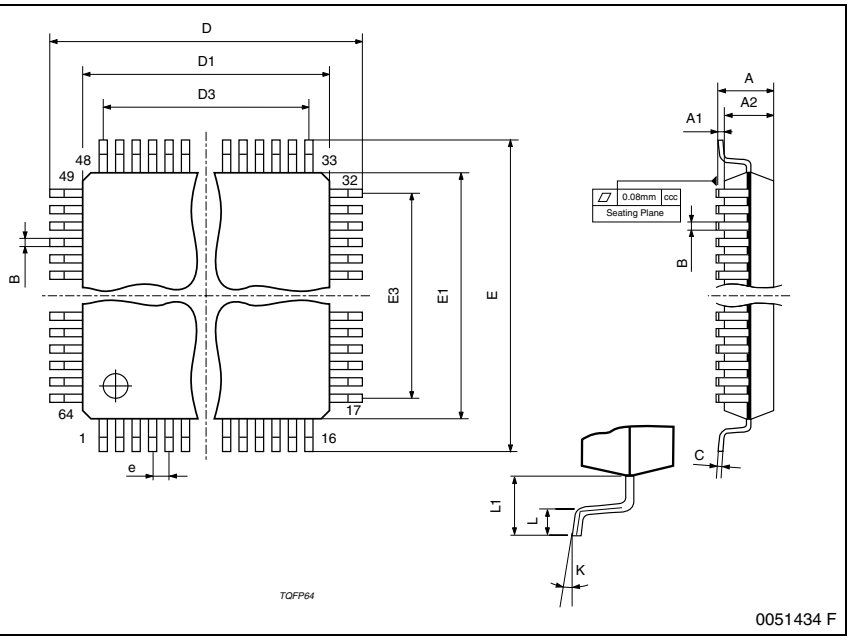
Figure 7. LQFP64 (10x10x1.4mm) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.0066	0.0086	0.0106
C	0.09		0.20	0.0035		0.0079
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		7.50			0.295	
e		0.50			0.0197	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		7.50			0.295	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
K	0° (min.), 3.5° (min.), 7°(max.)					
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



LQFP64 (10 x 10 x 1.4mm)



GAPGPS00365

5 Revision history

Table 3. Document revision history

Date	Revision	Changes
07-Mar-2012	1	Initial release.
25-Jun-2012	2	Updated *Table 1: Device summary on page 1*.
16-Sept-2013	3	Updated Disclaimer

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com