HMC960LP4E

v01.1212

DC - 100 MHz DUAL DIGITAL VARIABLE GAIN AMPLIFIER with DRIVER

Typical Applications

The HMC960LP4E is suitable for:

- Baseband I/Q Transceivers
- Direct Conversion & Low IF Transceivers
- Diversity Receivers
- ADC Drivers
- Adaptive Gain Control

Features

Low Noise: 6 dB NF

High Linearity: Output IP3 +30 dBm

Variable Gain: 0 to 40 dB

High Bandwidth: DC to 100 MHz

Precise Gain Accuracy: 0.5 dB Gain Step

Excellent Magnitude and Phase Response

Externally Controlled Common Mode Output Level

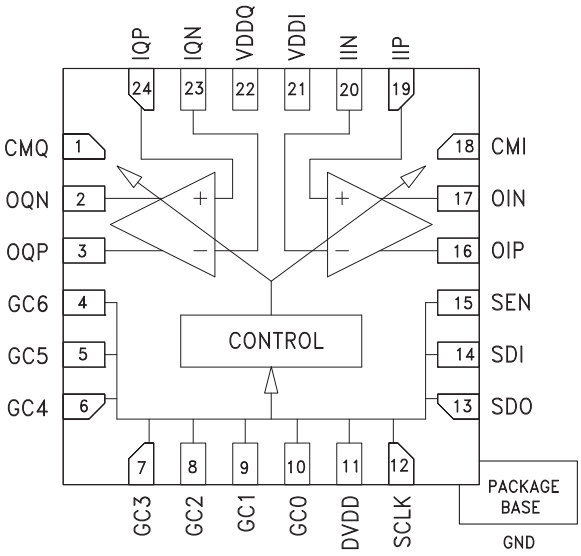
Parallel or Serial Gain Control

Read/Write Serial Port Interface (SPI)

24 Lead 4x4 mm SMT Package 16 mm^2

Programmable Input Impedance
(400 Ω Differential or 100 Ω Differential)

Functional Diagram



General Description

The HMC960LP4E is a digitally programmable dual channel variable gain amplifier. It supports discrete gain steps from 0 to 40 dB in precise 0.5 dB steps. It features a glitch free architecture to provide exceptionally smooth gain transitions. The device has matched gain paths which provide excellent quadrature balance over a wide signal bandwidth.

The HMC960LP4E provides an SPI programmable input impedance of 100 Ω differential or 400 Ω differential (default).

Externally controlled common mode output feature enables the HMC960LP4E to provide a flexible output interface to other parts in the signal path.

Gain can be controlled via either a parallel interface (GC[6:0]) or via the read/write serial port (SPI).

Housed in a compact 4x4mm (LP4) SMT QFN package, the HMC960LP4E requires minimal external components and provides a low cost alternative to more complicated switched amplifier architectures.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

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Table 1. Electrical Specifications

T_A = +25°C, VDDI, VDDQ, DVDD = 5V +/-10%, GND = 0V, 400 Ω differential load unless otherwise stated.

Parameter	Conditions	Min.	Typ.	Max.	Units
Analog Performance					
Gain Range		0		40	dB
Gain Step Size			0.5		dB
Gain Step Error	f = 40 MHz		0.05	±0.2	dB
Gain Absolute Error	f = 40 MHz		0.1	±0.2	dB
DC Offset [4]	measured over all gain settings		0	±50	mV
Signal Bandwidth 0.5 dB bandwidth 3 dB bandwidth	over all gain settings	 50 100	 90 180		 MHz MHz
Noise Figure 100 Ω Input Impedance (100 Ohm source) 400 Ω Input Impedance (400 Ohm source)	Gain: 0 dB (min gain) 10 dB 20 dB 30 dB 40 dB (max gain) 0 dB (min gain) 10 dB 20 dB 30 dB 40 dB (max gain)		 23 14 7.5 6.5 6 17.5 11 6.7 6.3 6.1		 dB dB dB dB dB dB dB dB dB dB
Output noise 0 dB gain 40 dB gain	measured at f = 1 MHz 100 Ω matched input load		 9 125		 nV/rtHz nV/rtHz
Output IP3 0 dB gain 40 dB gain	using two tones near 20 MHz at 2 Vppd output		 32 33		 dBm dBm
IM3 0 dB gain 40 dB gain	using two tones near 20 MHz at 2 Vppd output		 -75 -80		 dBc dBc
Output IP2 0 dB gain 40 dB gain	using two tones near 20 MHz at 2 Vppd output		 73 73		 dBm dBm
IM2 0 dB gain 40 dB gain	using two tones near 20 MHz at 2 Vppd output		 -80 -80		 dBc dBc
Sideband Suppression (Uncalibrated)[1]	tested at 20 MHz over all gains	40	55		dB
I/Q Channel Balance[1] Gain Phase	tested at 20 MHz		 0.02 0.15		 dB degrees
I/Q Channel Isolation		60	70		dB
Analog I/O					
Differential input impedance	100 Ω Mode 400 Ω Mode	80 320	100 400	120 480	Ω Ω
Full Scale Differential Input 400 Ω Differential Load 100 Ω Differential Load	 min / max gain setting min / max gain setting			 2/0.02 1/0.02	 Vppd Vppd
Input Common Mode Voltage Range		1		4	V

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Table 1. Electrical Specifications, T_A = +25°C (Continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
Full Scale Differential Output 400 Ω Differential Load 100 Ω Differential Load				 2 1	 Vppd Vppd
Output Voltage Range		0.5		Vdd - 0.5	V
Output Common Mode Voltage Range [2]		1	Vdd/2	3	V
Digital I/O	Tested at 30 MHz Operation				
Logic Levels					
Digital Input Low Level (VIL)				0.4	V
Digital Input High Level (VIH)		1.5			V
Digital Output Low Level (VOL)				0.4	V
Digital Output High Level (VOH)		Vdd - 0.4			V
Supply Related					
Digital I/O					
Power Supply	Analog & Digital Supplies	4.5	5	5.5	V
Supply Current [3]	Both I/Q channels		70		mA

[1] Sideband Rejection is only measured in dB, but relates to phase/magnitude channel imbalance as follows, for a mismatch of 1 degree phase and 0.1 dB magnitude:
SBR = -10Log[(1+A^2-2Acosx)/(1+A^2+2Acosx)]
where A = 10^(0.1/20) (linear magnitude) and x = 1*pi/180 (radians)
[2] Output common mode voltage range is specified for worst case temperature, supply voltage, and bias settings with 2 Vppd signal amplitude. For 5 V supply and recommended biasing (op-amp bias =1 and driver bias=2), over 3.5 V is typical. See "Output IP3 vs. Common Mode Voltage vs. Driver Bias Setting[1]" in Figure 12
[3] Recommend bias setting (op-amp bias =1 and driver bias=2)
[4] Standard deviation = 15 mV

Table 2. Test Conditions

Unless otherwise specified, the following test conditions were used

Parameter	Condition
Temperature	+27 °C
Gain Setting	0 dB
Output Signal Level	2 Vppd
Input/Output Common Mode Level	2.5 V
Programmed Impedance	200 Ω per input (400 Ω differential)
Output Load	200 Ω per output (400 Ω differential)
Supplies	Analog: +5 V, Digital +5 V
Driver Bias Setting	'10'
Op-Amp Bias Setting	'01' (Standard Setting)

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Figure 1. Gain vs. Temperature (40 MHz)

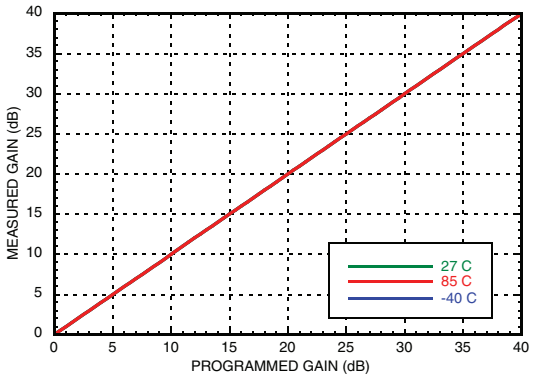


Figure 2. Gain Error, Absolute & Step (40 MHz)

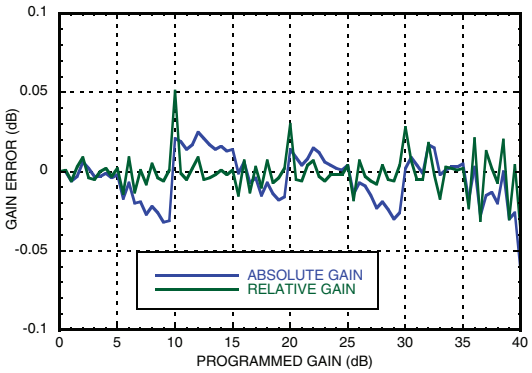


Figure 3. Gain vs. Temperature (100 MHz)

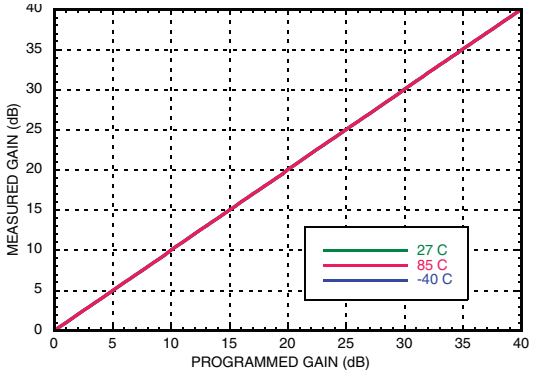


Figure 4. Gain Error, Absolute & Step (100 MHz)

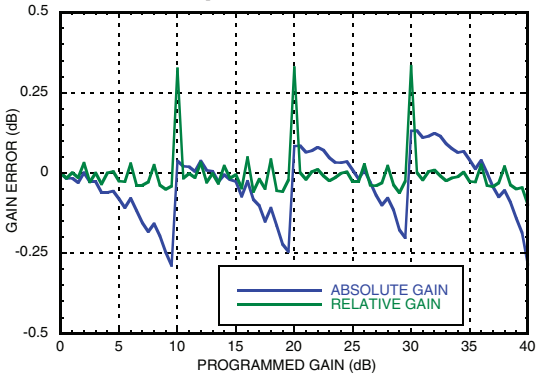


Figure 5. Frequency Response vs. Gain [1]

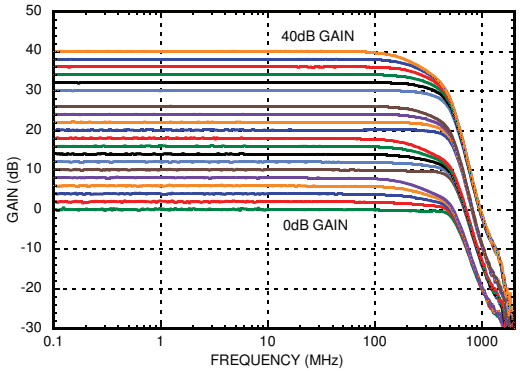
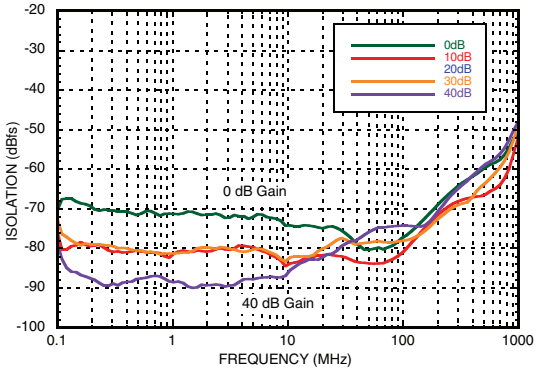


Figure 6. Channel Isolation vs. Gain [2]



[1] 2 dB Gain step increments
[2] 10 dB Gain step increments

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Figure 7. IM2 vs. Frequency & Gain [4]

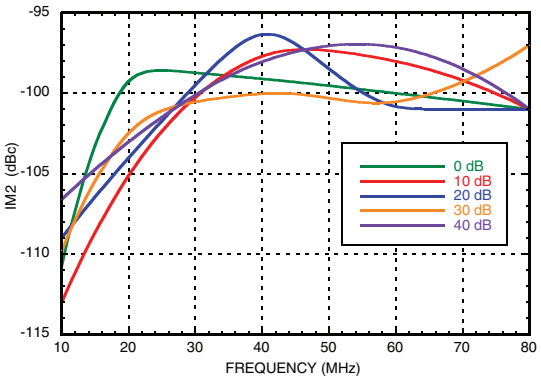


Figure 8. Output IP2 vs. Frequency & Gain [4]

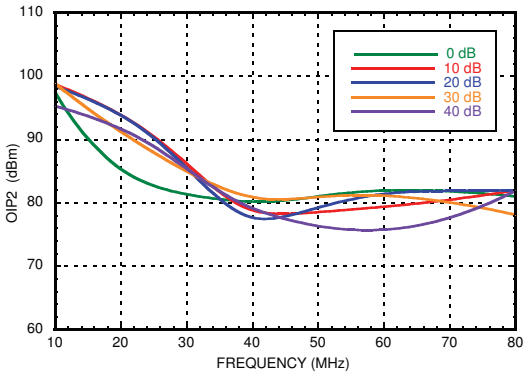


Figure 9. IM3 vs. Frequency and Gain, Standard Bias Setting [5][7]

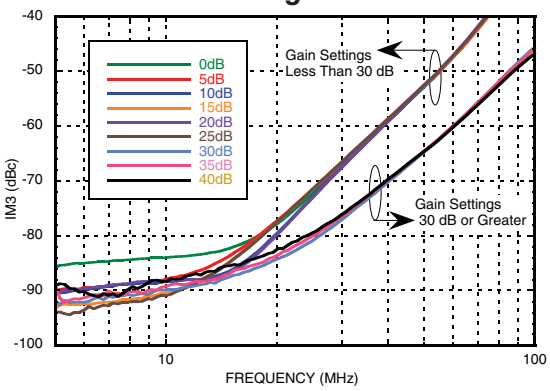


Figure 10. IM3 vs. Frequency & Gain, High Linearity Bias Setting [6][7]

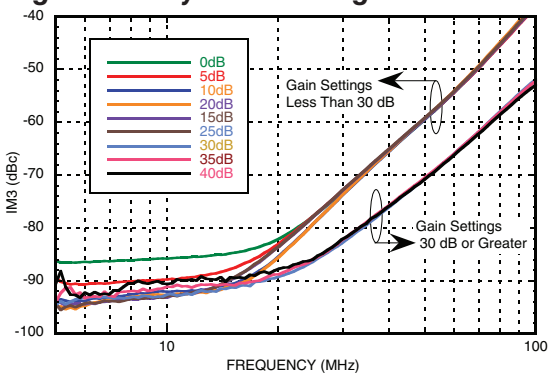


Figure 11. Output IP3 vs. Frequency & Gain, Standard Bias Setting [5] [7]

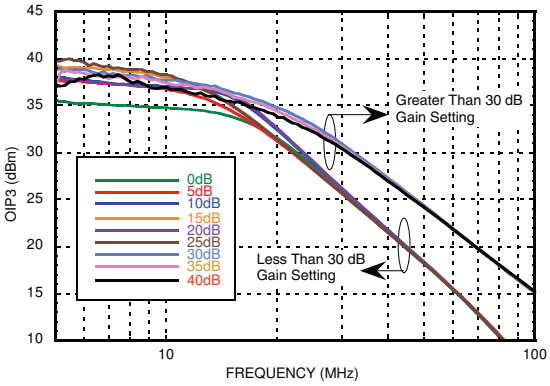
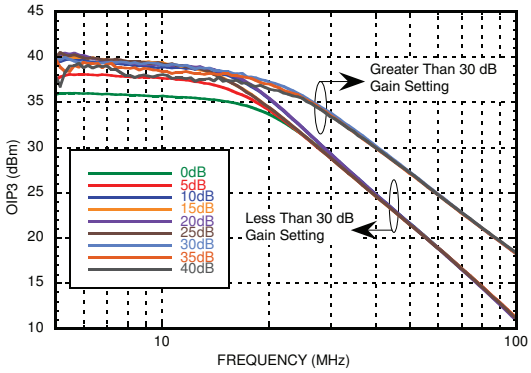


Figure 12. Output IP3 vs. Frequency & Gain, High Linearity Bias Setting [6] [7]



[3] VGA Gain = 0 dB, 2 Vpp differential output
[4] 300 mVppd output, load impedance = 400 Ω differential
[5] Amplifier bias setting = '01' (Standard Setting)
[6] Amplifier bias setting = '10' (High Linearity Setting)

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Figure 13. Output IP3 vs. Frequency & Bias, Gain = 10 dB [5][6] [7] [9]

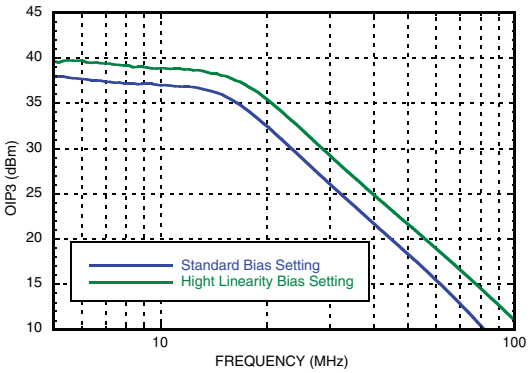


Figure 14. Output IP3 vs. Frequency & Bias, Gain = 30 dB [5][6] [7] [9]

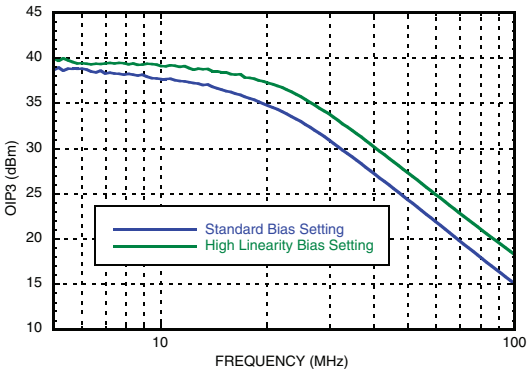


Figure 15. Output IP3 vs. Output Common Mode, Standard Bias Setting [3][5]

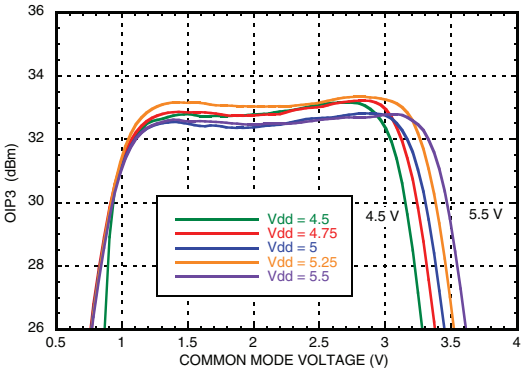


Figure 16. Output IP3 vs. Output Common Mode, High Linearity Bias Settings [3][6]

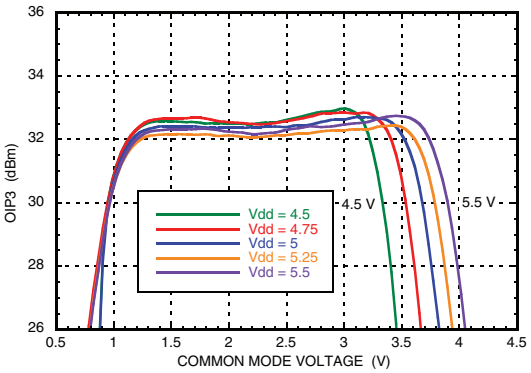


Figure 17. Output Voltage vs. Input Voltage for Various Gains

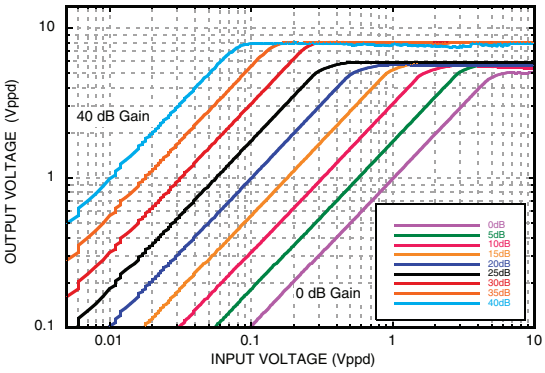
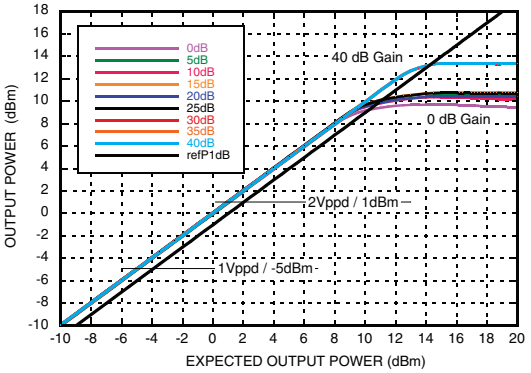


Figure 18. Output vs. Expected Output Over Gain [8]



[7] Load Impedance = 400 Ω differential, 2 Vppd output

[8] Output Power (dBm) is measured into 400 Ω output load

[9] Use the following formulas conversion between dBm, dBV_{rms}, and V_{ppd}, using a 400 Ω differential load: $dBV_{rms} = 20\log(Vppd/2.8284)$, $dBm = 10\log((Vppd/2.8284)^2/400x10^{-3})$, $dBm = dBV_{rms} - 10\log(400x10^{-3})$

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Figure 19. Output Noise vs. Low Frequency, 100 Ω Rin [10]

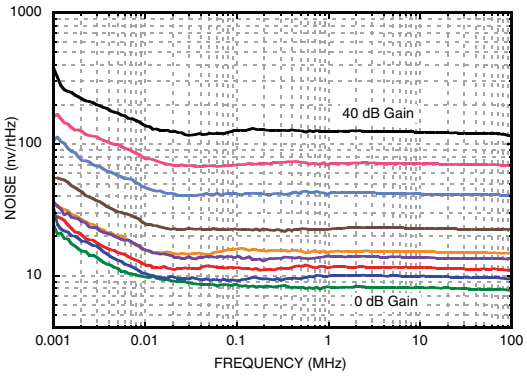


Figure 20. Noise Figure vs. Gain & Input Impedance at 1 MHz

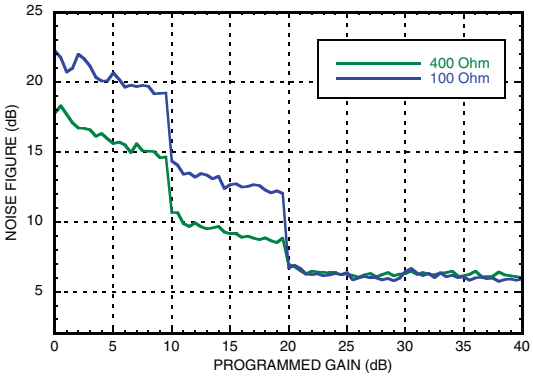


Figure 21. Sideband Rejection vs. Gain

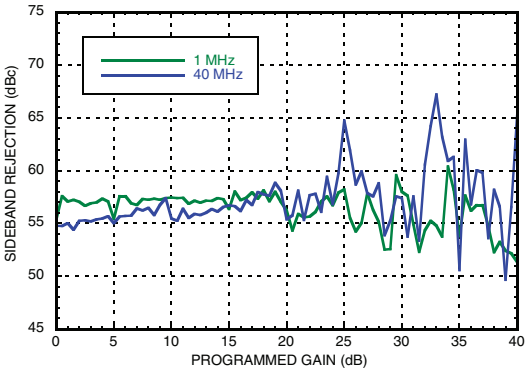
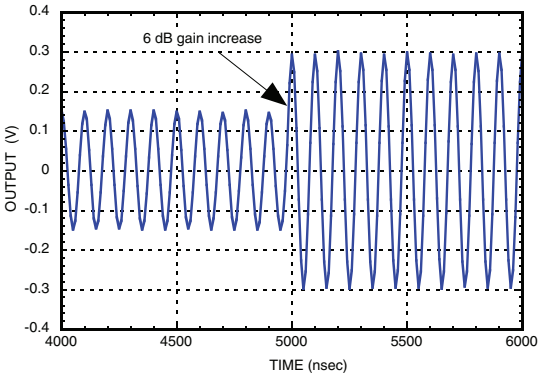


Figure 22. Transient Behavior, 10 MHz, 6 dB Gain Increase



[10] 5 dB Gain step increments

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Table 3. Absolute Maximum Ratings

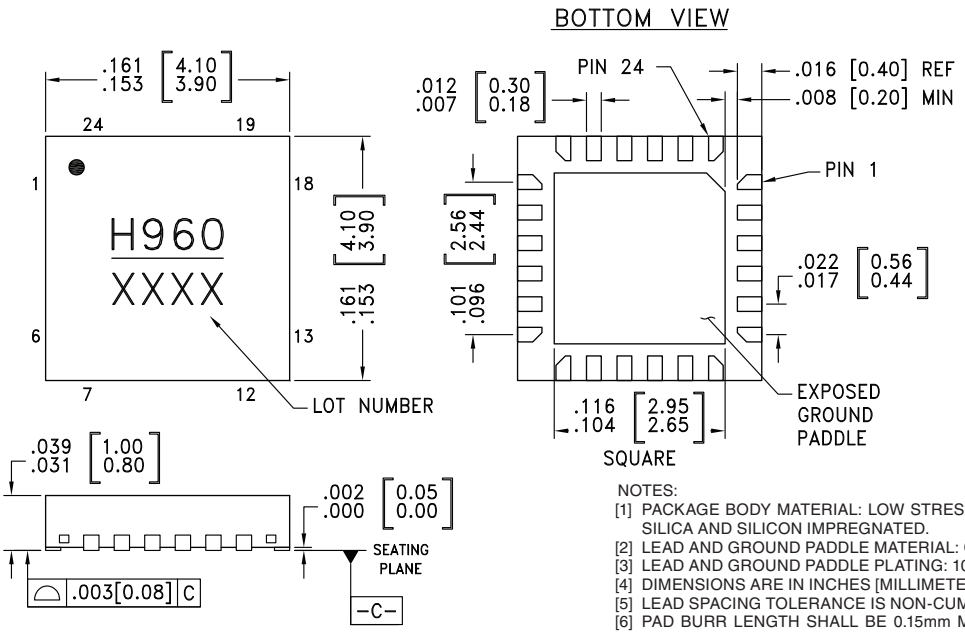
Nominal 5 V Supply to GND VDDI, VDDQ, DVDD	-0.3 to 5.5 V
Common Mode Inputs Pins (CMI, CMQ)	-0.3 to 5.5 V
Input and Output Pins IIP, IIN, IQP, IQN, OIP, OIN, OQP, OQN	-0.3 to 5.5 V
Digital Pins SEN, SDI, SCK, SDO, GC[6:0] SDO min load impedance	-0.3 to 5.5 V 1 kΩ
Operating Temperature Range	-40 to +85 °C
Storage Temperature	-65 to +125 °C
Maximum Junction Temperature	125 °C
Thermal Resistance (Rth) (junction to ground paddle)	10 °C/W

Reflow Soldering Peak Temperature Time at Peak Temperature	 260 °C 40 µs
ESD Sensitivity (HBM)	1 kV Class 1 C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
[1] PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
[2] LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
[3] LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
[4] DIMENSIONS ARE IN INCHES [MILLIMETERS].
[5] LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
[6] PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25m MAX.
[7] PACKAGE WARP SHALL NOT EXCEED 0.05mm
[8] ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
[9] REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating [2]	Package Marking [1]
HMC960LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H960 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

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Table 4. Pin Descriptions

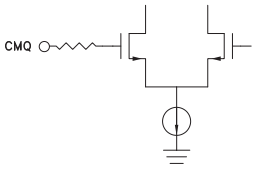
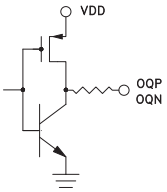
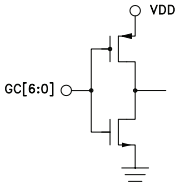
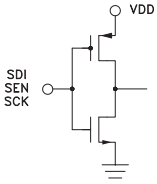
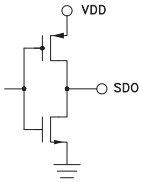
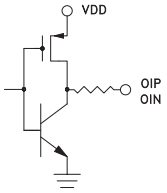
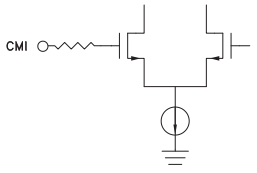
Pin Number	Function	Description	Interface Schematic
1	CMQ	Quadrature (Q) channel output common mode level	
2, 3	OQN, OQP	Quadrature (Q) channel positive and negative differential outputs	
4 - 10	GC[6:0]	Gain Control Input Pins Gain is defined as: GC[6:0] = 0d —> Gain = 0 dB GC[6:0] = 1d —> Gain = 0.5 dB GC[6:0] = 2d —> Gain = 1 dB GC[6:0] = 79d —> Gain = 39.5 dB GC[6:0] = 80d —> Gain = 40 dB	
11	DVDD	Digital 5V Supply. Must be locally decoupled to GND.	
12, 14, 15	SCLK, SDI, SEN	SPI Data clock, data input and enable respectively.	
13	SDO	SPI Data Output	
16, 17	OIP, OIN	Inphase (I) channel negative and positive differential outputs respectively	
18	CMI	Inphase (I) channel output common mode level	

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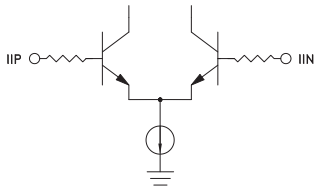
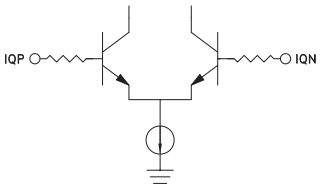
Table 4. Pin Descriptions *(Continued)*

Pin Number	Function	Description	Interface Schematic
19, 20	IIP, IIN	Inphase (I) channel positive and negative differential inputs respectively	
21	VDDI	Inphase (I) Channel 5 V Supply. Must be locally decoupled to GND	
22	VDDQ	Quadrature (Q) Channel 5 V Supply. Must be locally decoupled to GND	
23, 24	IQN, IQP	Quadrature (Q) channel negative and positive differential inputs respectively	

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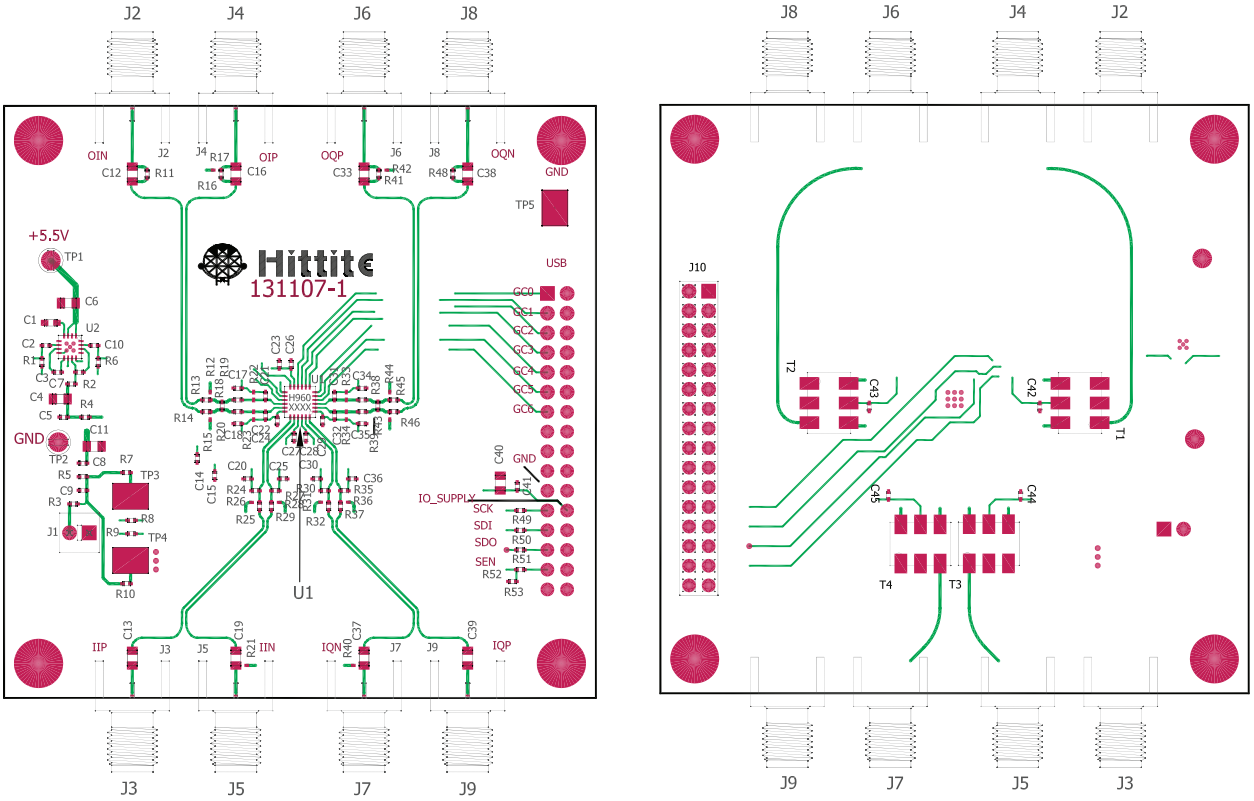
DC - 100 MHz DUAL DIGITAL VARIABLE GAIN AMPLIFIER with DRIVER

Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohms impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Table 5. Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC960LP4E Evaluation PCB	131109-HMC960LP4E
Evaluation Kit	HMC960LP4E Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software)	131191-HMC960LP4E

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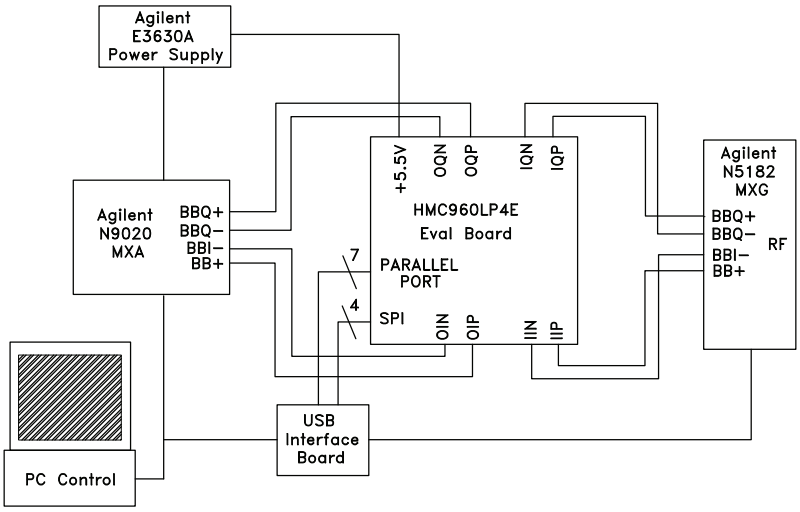
DC - 100 MHz DUAL DIGITAL VARIABLE GAIN AMPLIFIER with DRIVER

Evaluation Setup



HMC960LP4E Application Information

The wide bandwidth, large dynamic range, and excellent noise-linearity trade-off make the HMC960LP4E ideal for Automatic Gain Control applications in the baseband section of a direct down-conversion receiver. Matched dual amplifier design provides excellent gain and phase balance between the two channels. Externally controlled common mode voltage, and SPI programmable input impedance simplify the interface between the HMC960LP4E and other components in the signal path. The HMC960LP4E can be cascaded with HMC900LP5E without the need of any matching circuitry. Together, these two components provide a complete baseband line-up that can directly drive ADC's such as the 12-bit, dual channel, 320 MSPS HMCAD1520.

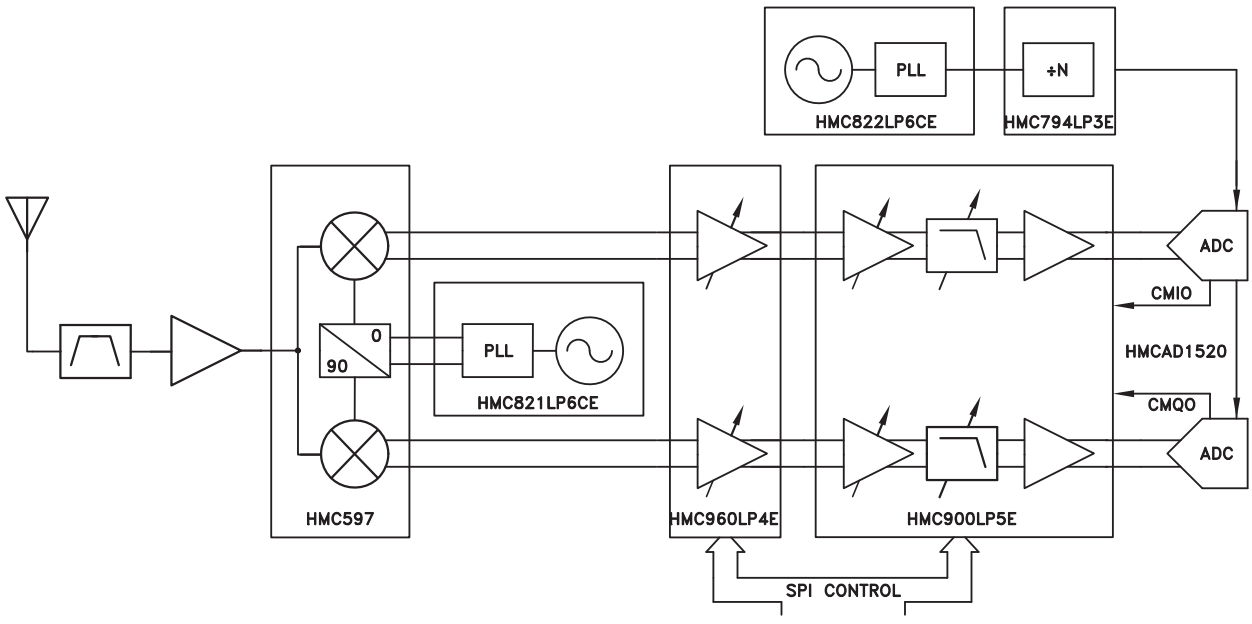


Figure 1. Typical Receive Path Block Diagram Showing HMC960LP4E

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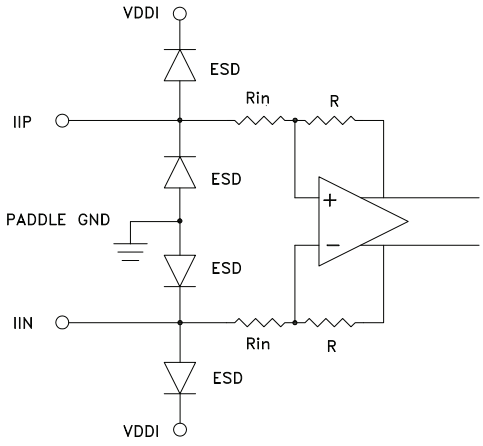
Theory of Operation

The HMC960LP4E consists of the following functional blocks

1. Input Match & Gain Stage
2. Second Gain Stage
3. Output Driver & Gain Stage
4. Bias Circuit
5. Serial Port Interface
6. Parallel Port Interface

Input Match & Gain Stage

The HMC960LP4E input stage consists of a user selectable 100 Ω or 400 Ω differential input impedance and a programmable gain of 0, 10 or 20 dB. A block diagram showing input impedance of the I channel is presented below, Q channel is similar.



NOTE:
[1] Rin is selectable VIA SPI 50 ΩOR 200Ω
[2] R = Rin or 3.162Rin or 10Rin depending on selected gain

Figure 2. Input Stage Block Diagram

Second Gain Stage

The HMC960LP4E second stage consists of a series of carefully scaled resistors to generate up to 10 dB of gain in 0.5 dB steps. The gain step is fully determined by resistor ratios and as such the gain precision is relatively independent of both temperature and process variation.

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Output Driver & Gain Stage

The HMC960LP4E output driver consists of a differential class AB driver which is designed to drive typical ADC loads directly or can drive up to 200 Ω in parallel with 50 pF to AC ground per differential output. The stage provides a programmable 0 dB or 10 dB gain via switched resistors. Note that the output common mode of the driver is controlled directly via an input pin and can be set as per "Table 1. Electrical Specifications".

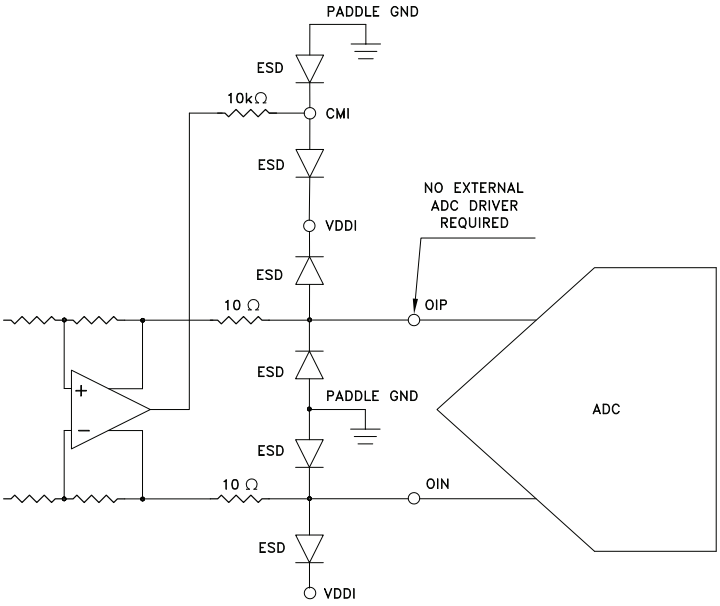

Figure 3. Output Driver Block Diagram

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Gain Decode Logic

The decode logic automatically allocates gain to the three stages so as to minimize output noise and optimize noise figure. Without using decode logic gain can be allocated arbitrarily, as shown in Table 11. Decode logic gain allocation, shown in Figure 4, can be controlled via the parallel port or the SPI, and reflects gain control shown in Table 10.

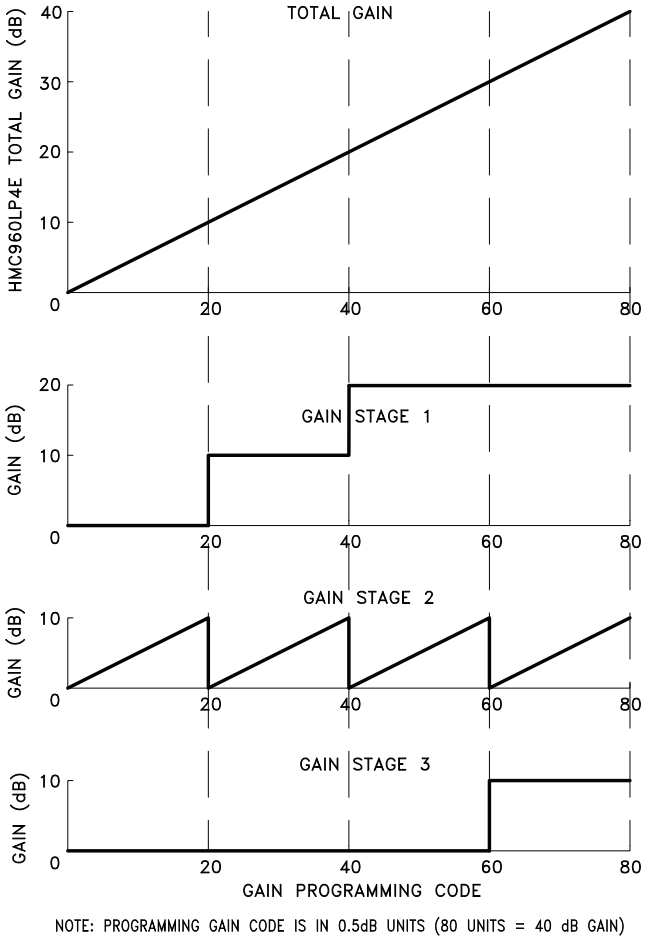

Figure 4. Decode Logic Gain Allocation

Bias Circuit

A band gap reference circuit generates the reference currents used by the different sections. The bias circuit is enabled or disabled as required with the I or Q channel as appropriate.

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Serial Port Interface

The HMC960LP4E features a four wire serial port for simple communication with the host controller. Typical serial port operation can be run with SCK at speeds up to 30 MHz.

The details of SPI access for the HMC960LP4E is provided in the following sections. Note that the READ operation below is always preceded by a WRITE operation to Register 0 to define the register to be queried. Also note that every READ cycle is also a WRITE cycle in that data sent to the SPI while reading the data will also be stored by the HMC960LP4E when SEN goes high. If this is not desired then it is suggested to write to Register 0 during the READ operation so that the status of the device will be unaffected.

Power on Reset and Soft Reset

The HMC960LP4E has a built in Power On Reset (POR) and a serial port accessible Soft Reset (SR). POR is accomplished when power is cycled for the HMC960LP4E while SR is accomplished via the SPI by writing 20h to Reg 0h followed by writing 00h to Reg 0h. All chip registers will be reset to default states approximately 250 us after power up.

Serial Port WRITE Operation

The host changes the data on the falling edge of SCK and the HMC960LP4E reads the data on the rising edge.

A typical WRITE cycle is shown in Figure 5. It is 32 clock cycles long.

1. The host both asserts SEN (active low Serial Port Enable) and places the MSB of the data on SDI followed by a rising edge on SCK.
2. HMC960LP4E reads SDI (the MSB) on the 1st rising edge of SCK after SEN.
3. HMC960LP4E registers the data bits, D23:D0, in the next 23 rising edges of SCK (total of 24 data bits).
4. Host places the 5 register address bits, A4:A0, on the next 5 falling edges of SCK (MSB to LSB) while the HMC960LP4E reads the address bits on the corresponding rising edge of SCK.
5. Host places the 3 chip address bits, CA2:CA0=[110], on the next 3 falling edges of SCK (MSB to LSB). Note the HMC960LP4E chip address is fixed as “6d” or “110b”.
6. SEN goes from low to high after the 32th rising edge of SCK. This completes the WRITE cycle.
7. HMC960LP4E also exports data back on the SDO line. For details see the section on READ operation.

Serial Port READ Operation

The SPI can read from the internal registers in the chip. The data is available on SDO pin. This pin itself is tri-stated when the device is not being addressed. However when the device is active and has been addressed by the SPI master, the HMC960LP4E controls the SDO pin and exports data on this pin during the next SPI cycle.

HMC960LP4E changes the data to the host on the rising edge of SCK and the host reads the data from HMC960LP4E on the falling edge.

A typical READ cycle is shown in Figure 5. Read cycle is 32 clock cycles long. To specifically read a register, **the address of that register must be written to dedicated Reg 0h**. This requires two full cycles, one to write the required address, and a 2nd to retrieve the data. A read cycle can then be initiated as follows;

1. The host asserts SEN (active low Serial Port Enable) followed by a rising edge SCK.
2. HMC960LP4E reads SDI (the MSB) on the 1st rising edge of SCK after SEN.
3. HMC960LP4E registers the data bits in the next 23 rising edges of SCK (total of 24 data bits). **The LSBs of the data bits represent the address of the register that is intended to be read.**
4. Host places the 5 register address bits on the next 5 falling edges of SCK (MSB to LSB) while the HMC960LP4E reads the address bits on the corresponding rising edge of SCK. **For a read operation this is “00000”.**

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5. Host places the 3 chip address bits <110> on the next 3 falling edges of SCK (MSB to LSB). Note the HMC960LP4E chip address is fixed as “6d” or “110b”.
6. SEN goes from low to high after the 32nd rising edge of SCK. This completes the first portion of the READ cycle.
7. The host asserts SEN (active low Serial Port Enable) followed by a rising edge SCK.
8. HMC960LP4E places the 24 data bits, 5 address bits, and 3 chip id bits, on the SDO, on each rising edge of the SCK, commencing with the first rising edge beginning with MSB.
9. The host de-asserts SEN (i.e. sets SEN high) after reading the 32 bits from the SDO output. The 32 bits consists of 24 data bits, 5 address bits, and the 3 chip id bits. This completes the read cycle.

   Note that the data sent to the SPI during this portion of the READ operation is stored in the SPI when SEN is de-asserted. This can potentially change the state of the HMC960LP4E. If this is undesired it is recommended that during the second phase of the READ operation that Reg 0h is addressed with either the same address or the address of another register to be read during the next cycle.

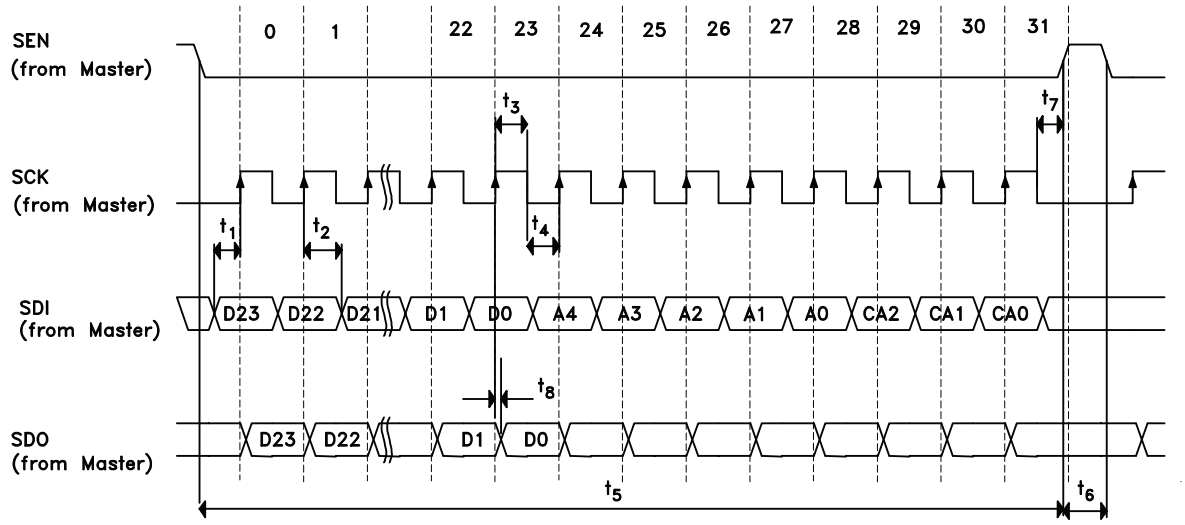

Figure 5. SPI Timing Diagram

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DVDD = 5 V ±10%, GND = 0 V

Table 6. Main SPI Timing Characteristics

Parameter	Conditions	Min	Typ	Max	Units
t_1	SDI to SCK Setup Time	8			nsec
t_2	SDI to SCK Hold Time	8			nsec
t_3	SCK High Duration [1]	10			nsec
t_4	SCK Low Duration	10			nsec
t_5	SEN Low Duration	20			nsec
t_6	SEN High Duration	20			nsec
t_7	SCK to SEN [2]	8			nsec
t_8	SCK to SDO out [3]			8	nsec

[1] The SPI is relatively insensitive to the duty cycle of SCK.

[2] SEN must rise after the 32nd falling edge of SCK but before the next rising SCK edge. If SCK is shared amongst several devices this timing must be respected.

[3] Typical load to SDO is 10 pF, maximum 20 pF

Parallel Port Interface

The HMC960LP4E features a seven bit parallel port to aid in real time gain selection. The dynamic performance of the parallel port is specified below.

Table 7. Gain Control Parallel Port Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Units
f_{SSP}	Gain control switching rate			20	MHz
t_{SSP}	Allowable skew between GC[6:0] input transitions			10	nsec

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Register Map

Three registers provide all the required functionality via the SPI port.

Table 8. Reg 01h - Enable Register

Bit	Name	Width	Default	Description
[0]	VGA_I_enable	1	1	VGA I channel enable bit
[1]	VGA_Q_enable	1	1	VGA Q channel enable bit
[2:3]	spare	2	0	
[23:4]	unused	19		

Table 9. Reg 02h - Settings Register

Bit	Name	Width	Default	Description
[1:0]	opamp_bias[1:0]	2	01	Opamp bias setting. 00 -- min bias 11 -- max bias opamp_bias[1:0]=01 recommended for low frequency operation or 10 for improved linearity for higher frequency operation.
[3:2]	drvr_bias[1:0]	2	01	Driver bias setting. 00 -- min bias 11 -- max bias drvr_bias[1:0]=10 recommended (characterized on recommended setting only)
[4]	Rin_50ohm_select	1	1	Input impedance setting: 0: Rin of 200 ohms selected 1: Rin of 50 ohms selected
[5]	Gain_Control_from_SPI	1	0	Source of Gain Control Input 0: Gain control taken from parallel port (pins) 1: Gain control taken from SPI register 3
[6]	Gain_Decode_Disable	1	0	Bypass gain decoder 0: Decoded gain taken from register 3, bits <8:0> 1: Undecoded gain taken from register 3, bits <8:0> (SPI gain control must be selected)
[7]	Gain_Deglitching_Disable	1	0	Bypass gain deglitcher 0: Gain control deglitching active 1: Gain control deglitching disabled (applies to SPI and parallel port gain control)
[23:8]	unused			

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Table 10. Reg 03h - Gain Control Register WHEN USING decode logic [1][2]

Bit	Name	Width	Default	Description
[6:0]	gain[6:0]	7	0000000	Reg 02h[5]=1 and Reg 02h[6]=0 (i.e. SPI gain control & gain decode enabled) gain[6:0] defines teh VGA channel I and Q gain of 0-40dB as follows... 0000000 - 0 dB, minimum gain setting 0000001 - 0.5 dB gain 0000010 - 1.0 dB gain ... 1001110 - 39 dB gain 1001111 - 39.5 dB gain 1010000 - 40 dB, maximum gain setting Reg 02h[5] = 1 and Reg 02h[6] = 1 (i.e. SPI gain control & gain decode bypassed)
[23:7]	unused			

Table 11. Reg 03h - Gain Control Register, WHEN NOT using decode logic [3][4]

Bit	Name	Width	Default	Description
[8:0]	gain[8:0]	9	000000000	gain[8:0] define the VGA I and Q channel gain when Reg 02h[5] = 1 and Reg 02h[6] = 1 (i.e. SPI gain control and gain decode bypassed) Generally the first 4 bits control the 1st and 3rd stage while the last 5 bits control the 2nd stage gain. x001nnnnn - 1st stage set to 0 dB x010nnnnn - 1st stage set to 10 dB x100nnnnn - 1st stage set to 20 dB 0xxxnnnnn - 3rd stage set to 0 dB 1xxxnnnnn - 3rd stage set to 10 dB xxxxnnnnn - 2nd stage set as follows: nnnnn = 00000 - set to 0 dB nnnnn = 00001 - set to 0.5 dB nnnnn = 10011 - set to 9.5 dB nnnnn = 10100 - set to 10 dB
[23:9]	unused			

[1] Reg 03h bit assignment depends on the setting of bits 5 and 6 in Reg 02h. If Reg 02h[5]=0, then all Reg 03h bits are ignored (parallel port selected)
[2] For Reg 02h[5]=1 and Reg 02h[6]=0, gain control is via an SPI register with decode, and Reg 03h[6:0] are used as follows.
[3] Note that the Parallel Port gain logic always uses the gain decode logic, and therefore the bit encoding is the same as Reg 03h - Gain Control Register WHEN USING decode logic.
[4] For Reg 02h[5]=1 and Reg 02h[6]=1, gain control is via an SPI register without decode, and Reg 03h[6:0] are used as follows.

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