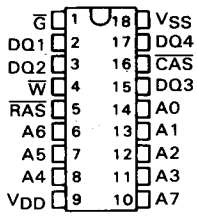
AUGUST 1980 – REVISED FEBRUARY 1988

- 16,384 × 4 Organization
- Single 5-V Supply (± 10% Tolerance)
- Performance Ranges

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ-MODIFY-WRITE CYCLE (MIN)
'4416-12	120 ns	70 ns	230 ns	320 ns
'4416-15	150 ns	80 ns	260 ns	330 ns
'4416-20	200 ns	120 ns	330 ns	440 ns

- Available Temperature Ranges with MIL-STD-883C Class B High-Reliability Processing
  – S . . . – 55°C to 100°C
  – L . . . 0°C to 70°C
- Long Refresh Period . . . 4 ms
- Low Refresh Overhead Time . . . As Low As 1.7% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs
- Early Write or $\overline{G}$ to Control Output Buffer Impedance
- Page-Mode Operation for Faster Access
- Low Power Dissipation
  – Operation . . . 200 mW (Typ)
  – Standby . . . 17.5 mW (Typ)
- SMOS (Scaled-MOS) N-Channel Technology

JD PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{DD}	5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The SMJ4416 is a Military high-speed, 65,536-bit, dynamic random-access memory organized as 16,384 words of 4 bits each. It employs state-of-the-art SMOS (scaled MOS) N-channel double-level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The SMJ4416 features $\overline{RAS}$ access times to 150 ns maximum. Power dissipation is 200 mW typical operating, 17.5 mW typical standby.

SMOS technology permits operation from a single 5-V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks have been reduced to 60 mA typical, and a – 1 V input voltage undershoot can be tolerated, minimizing system noise considerations. Input clamp diodes are used to ease system design.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with $\overline{RAS}$ in order to retain data. $\overline{CAS}$ can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 54/74 TTL. All address lines and data in are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The SMJ4416 is offered in 18-pin 300-mil ceramic side-braze dual-in-line package. It is available in −55°C to 100°C and 0°C to 70°C temperature ranges. Dual-in-line packages are designed for insertion in mounting-hole rows on 7,62 mm (300-mil) centers.

operation

address (A0 through A7)

Fourteen address bits are required to decode 1 of 16,384 storage locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the six column-address bits are set up on pins A1 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data out will remain in the high-impedance state allowing a write cycle with $\overline{G}$ grounded.

data in (DQ1 through DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latches. These latches can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In delayed write or read-modify-write, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1 through DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 54/74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(E)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high-impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying t_{GHD}.

output enable ($\overline{G}$)

The $\overline{G}$ signal controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers, putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until $\overline{G}$ or $\overline{CAS}$ is brought high.

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refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ can remain high (inactive) for this refresh sequence to conserve power.

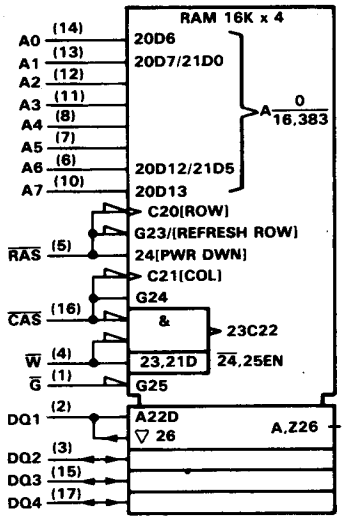
page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to set up and strobe sequential row addresses for the same page is eliminated. To extend beyond the 64 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 16K × 4 RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

power up

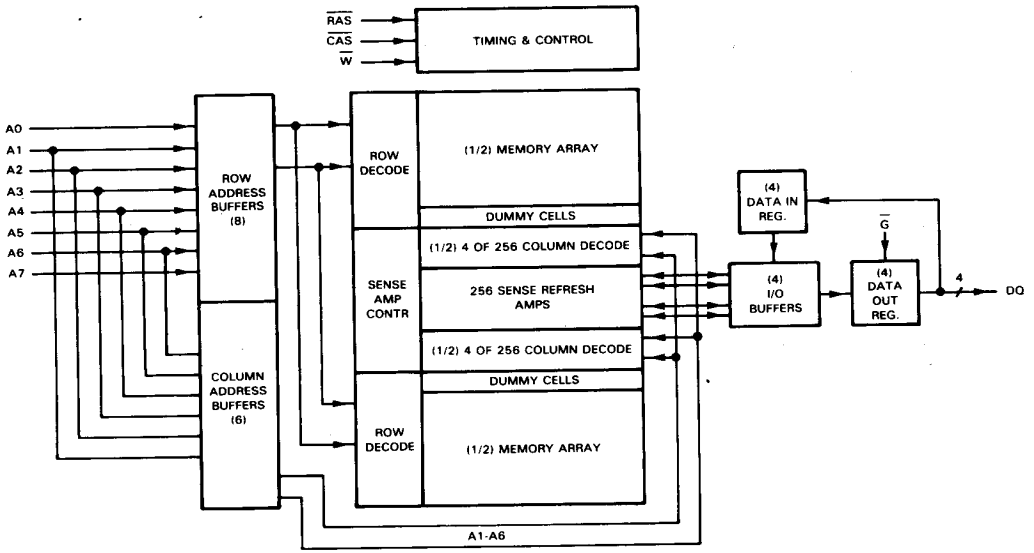
After power up, the power supply must remain at its steady-state value for 1 ms. In addition, the $\overline{RAS}$ input must remain high for 100 μs immediately prior to initialization. Initialization consists of performing eight $\overline{RAS}$ cycles before proper device operation is achieved.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the dual-in-line package.

functional block diagram



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absolute maximum ratings over operating temperature range (unless otherwise noted)†

Voltage on any pin except V_{DD} and data out (see Note 1)	−1.5 V to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS}	−1 V to 6 V
Short circuit output current	50 mA
Power dissipation	1 W
Minimum operating free-air temperature: S version	−55°C
L version	0°C
Operating case temperature: S version	100°C
L version	70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1. All voltage values in this data sheet are with respect to V_{SS}.

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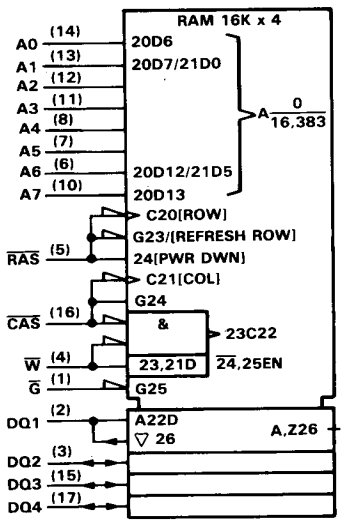

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Pin numbers shown are for the dual-in-line package.

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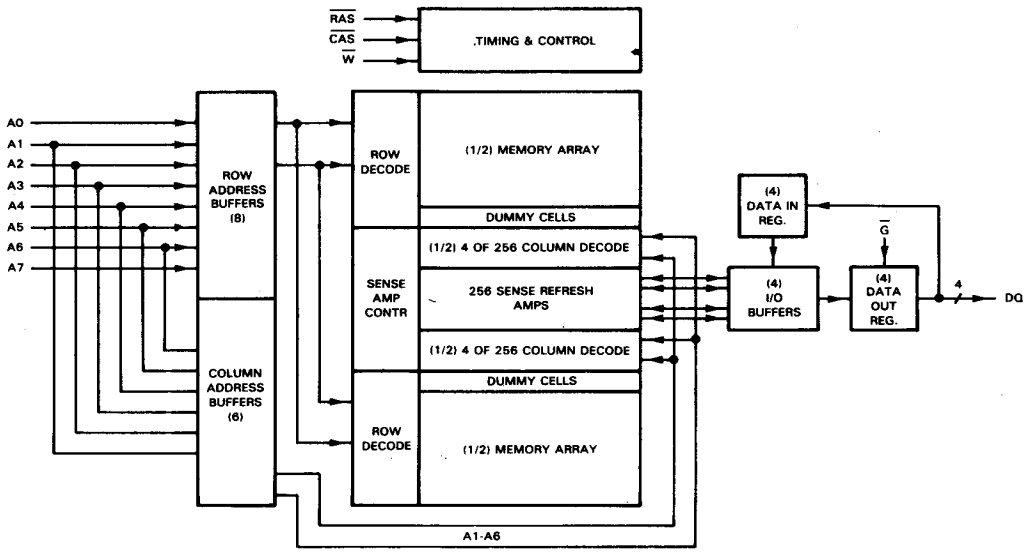

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Military Products

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Voltage on V_{DD} supply and data out with respect to V_{SS}	−1 V to 6 V
Short circuit output current	50 mA
Power dissipation	1 W
Minimum operating free-air temperature: S version	−55°C
L version	0°C
Operating case temperature: S version	100°C
L version	70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1. All voltage values in this data sheet are with respect to V_{SS}.

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recommended operating conditions

			S VERSION			L VERSION			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{DD}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{SS}	Supply voltage			0			0		V
V_{IH}	High-level input voltage	V_{DD} = 4.5 V	2.4		4.8	2.4		4.8	V
		V_{DD} = 5.5 V	2.4		5.8	2.4		5.8	
V_{IL}	Low-level input voltage		−0.6		0.8	−0.6		0.8	V
T_A	Operating free-air temperature		−55			0			°C
T_C	Operating case temperature				100			70	°C

NOTES: 2. The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.
3. Due to input protection circuitry, the applied voltage may begin to clamp at −0.6 V. Test conditions must comprehend this occurrence.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	SMJ4416-15			SMJ4416-20			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −2 mA	2.4			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{DD} = 5 V, All other pins = 0 V			±10			±10	μA
I_O	Output current (leakage)	V_O = 0.4 V to 5.5 V, V_{DD} = 5 V, $\overline{CAS}$ high			±10			±10	μA
I_{DD1}‡	Average operating current during read or write cycle	At t_c = minimum cycle		40	48		35	42	mA
I_{DD2}‡	Standby current (see Note 4)	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		3.5	5		3.5	5	mA
I_{DD3}‡	Average refresh current	t_c = minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high		25	40		21	34	mA
I_{DD4}‡	Average page-mode current	$t_{c(P)}$ = minimum cycle, $\overline{RAS}$ low, $\overline{CAS}$ cycling		25	40		21	34	mA

†All typical values are at T_C = 25°C and nominal supply voltages.
‡I_{DD1}-I_{DD4} are measured with open outputs.
NOTE 4. $V_{IL} \geq -0.6$ V on all inputs.

capacitance over recommended supply voltage range and recommended temparature range, f = 1 MHz§

PARAMETER		SMJ4416		UNIT
		TYP†	MAX	
$C_{i(A)}$	Input capacitance, address inputs	5	7	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
$C_{i/o}$	Input/output capacitance, data ports	8	10	pF

†All typical values are at T_C = 25°C and nominal supply voltages.
§These parameters are guaranteed but not tested.

switching characteristics over recommended supply voltage range and recommended operating temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	SMJ4416-15		SMJ4416-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$	C_L = 100 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{CAC}		70		120	ns
$t_{a(R)}$	Access time from $\overline{RAS}$	t_{RLCL} = MAX, C_L = 100 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA	t_{RAC}		150		200	ns
$t_{a(G)}$	Access time after $\overline{G}$ low	C_L = 100 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA			40		50	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high	C_L = 100 pF, I_{OH} = 5 mA, I_{OL} = 4.2 mA	t_{OFF}	0	30	0	40	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high	C_L = 100 pF, I_{OH} = −5 mA, I_{OL} = 4.2 mA		0	30	0	40	ns

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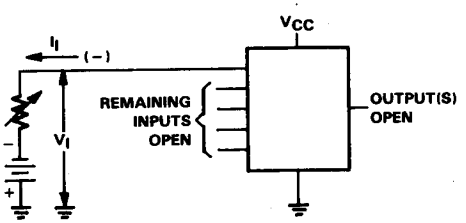
timing requirements over recommended supply voltage range and recommended operating temperature range

PARAMETER		ALT. SYMBOL	SMJ4416-15		SMJ4416-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page-mode cycle time	t_{PC}	140		210		ns
$t_{c(rd)}$	Read cycle time†	t_{RC}	260		330		ns
$t_{c(W)}$	Write cycle time	t_{WC}	260		330		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	360		440		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high (precharge time)‡	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low§	t_{CAS}	70	5000	120	5000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$ high (precharge time)	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse duration, $\overline{RAS}$ low¶	t_{RAS}	150	5000	200	5000	ns
$t_{w(W)}$	Write pulse duration	t_{WP}	40		50		ns
$t_{su(CA)}$	Column-address setup time	t_{ASC}	0		0		ns
$t_{su(RA)}$	Row-address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read-command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write-command setup time before $\overline{CAS}$ high	t_{CWL}	70		80		ns
$t_{su(WCH)R}$	Write-command setup time before $\overline{CAS}$ high for RMW cycles		60		80		ns
$t_{su(RMW)R}$	Write-command setup time before $\overline{RAS}$ high for RMW cycles		60		80		ns
$t_{su(WRH)}$	Write-command setup time before $\overline{RAS}$ high	t_{RWL}	70		80		ns
$t_{h(CLCA)}$	Column-address hold time after $\overline{CAS}$ low	t_{CAH}	40		50		ns
$t_{h(RA)}$	Row-address hold time	t_{RAH}	20		25		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low	t_{AR}	110		130		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	50		80		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	130		160		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	40		50		ns
$t_{h(RHrd)}$	Read-command hold time after $\overline{RAS}$ high‖	t_{RRH}	10		10		ns
$t_{h(CHrd)}$	Read-command hold time after $\overline{CAS}$ high‖	t_{RCH}	0		0		ns
$t_{h(CLW)}$	Write-command hold time after $\overline{CAS}$ low	t_{WCH}	50		80		ns
$t_{h(RLW)}$	Write-command hold time after $\overline{RAS}$ low	t_{WCR}	130		160		ns
t_{RLCH}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	150		200		ns
t_{CHRL}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	70		120		ns
t_{CLWL}	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{CWD}	110		170		ns
t_{RLCL}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (maximum value specified only to guarantee access time)	t_{RCD}	70	80	70	80	ns
t_{RLWL}	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (read-modify-write-cycle only)#	t_{RWD}	190		250		ns
t_{WLCL}	Delay time, $\overline{W}$ low to $\overline{CAS}$ low (early write cycle)	t_{WCS}	−5		−5		ns
t_{GHD}	Delay time, $\overline{G}$ high before data applied at DQ		30		40		ns
t_{rf}	Refresh time interval	t_{REF}		4		4	ms

†All cycle times assume t_t = 5 ns.
‡Page mode only.
§In a read-modify-write cycle, t_{CLWL} and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $t_{w(CL)}$.
¶In a read-modify-write cycle, t_{RLWL} and $t_{su(WRH)}$ must be observed. Depending on the user's transition time, this may require additional $\overline{RAS}$ low time $t_{w(RL)}$.
‖These parameters are guaranteed but not tested.
#Necessary to insure $\overline{G}$ has disabled the output buffers prior to applying data to the device.

PARAMETER MEASUREMENT INFORMATION



NOTE 5. Each input is tested separately.

FIGURE 1. INPUT CLAMP VOLTAGE TEST CIRCUIT

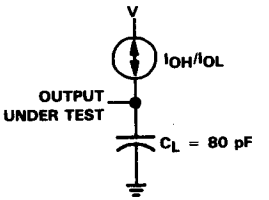
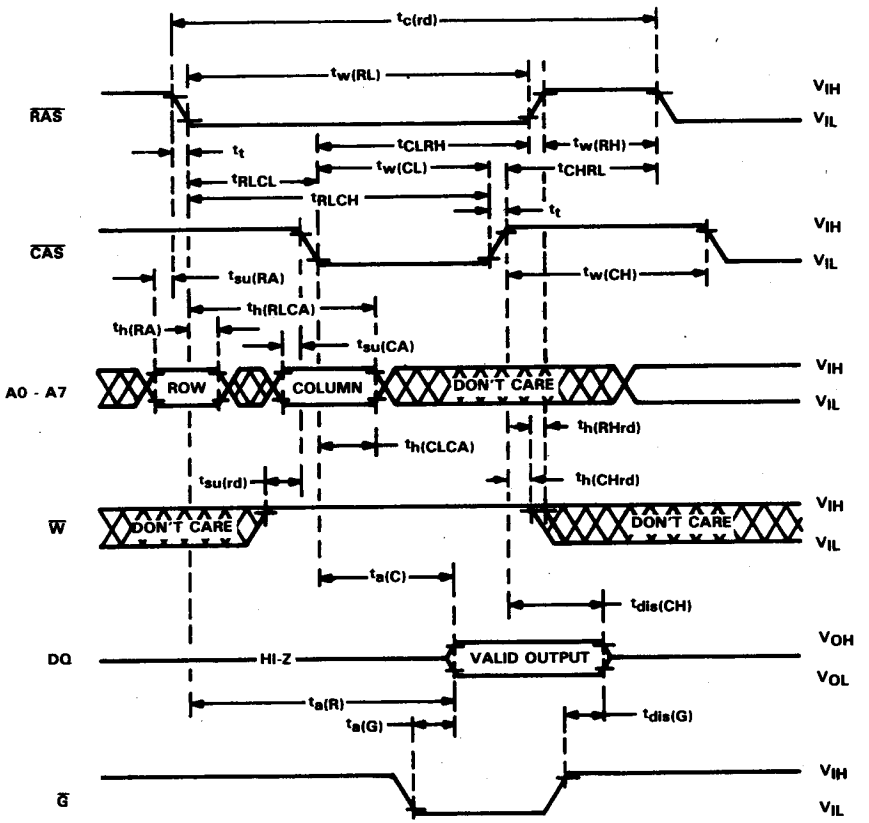


FIGURE 2. EQUIVALENT LOAD CIRCUIT

read cycle timing



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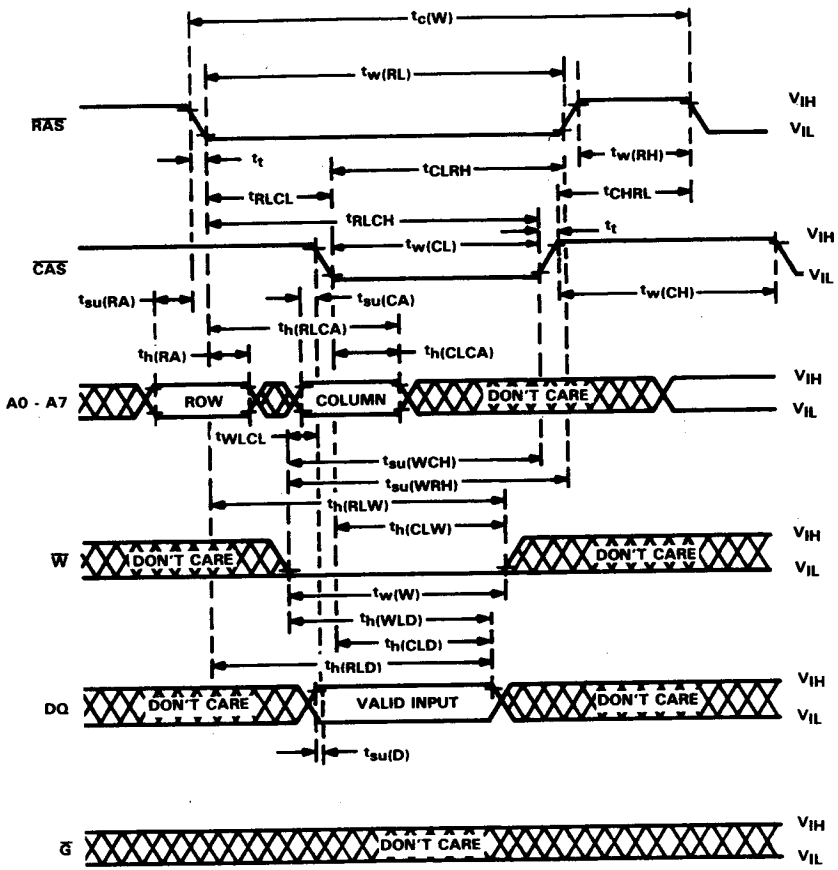
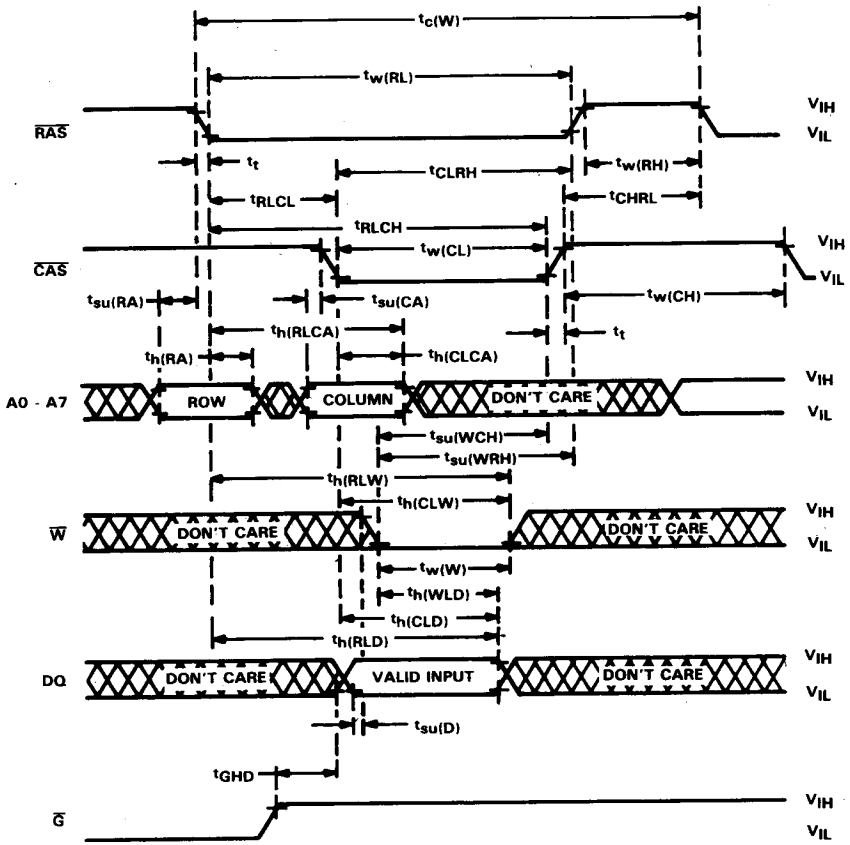
early write cycle timing



write cycle timing



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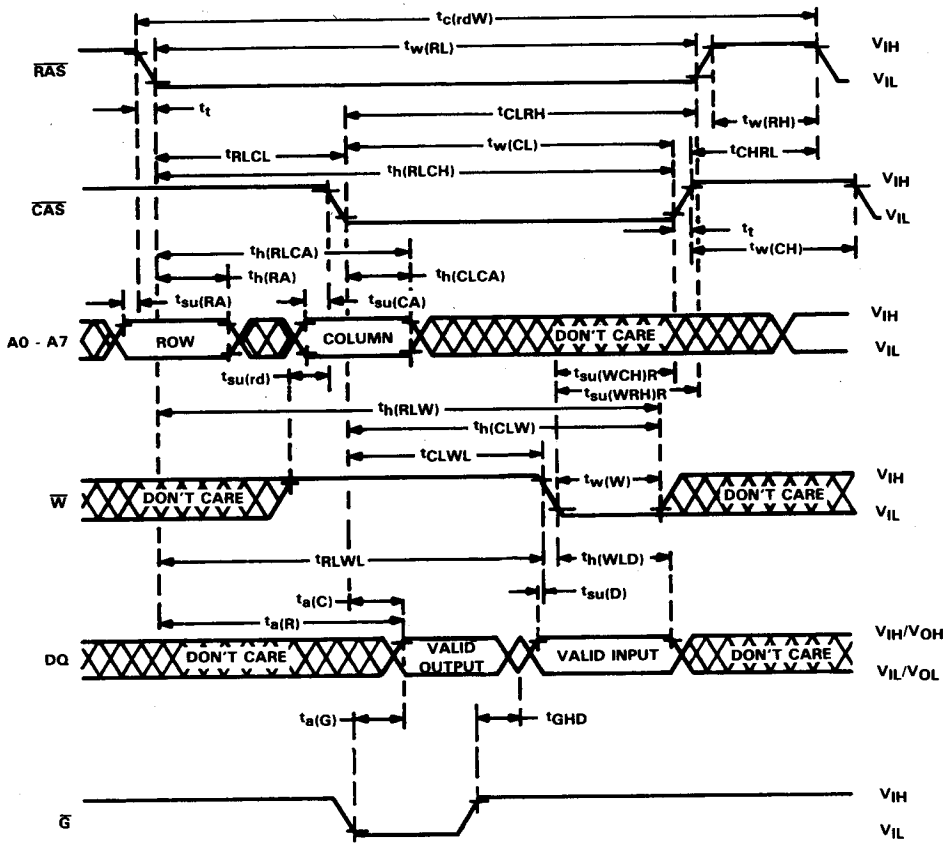
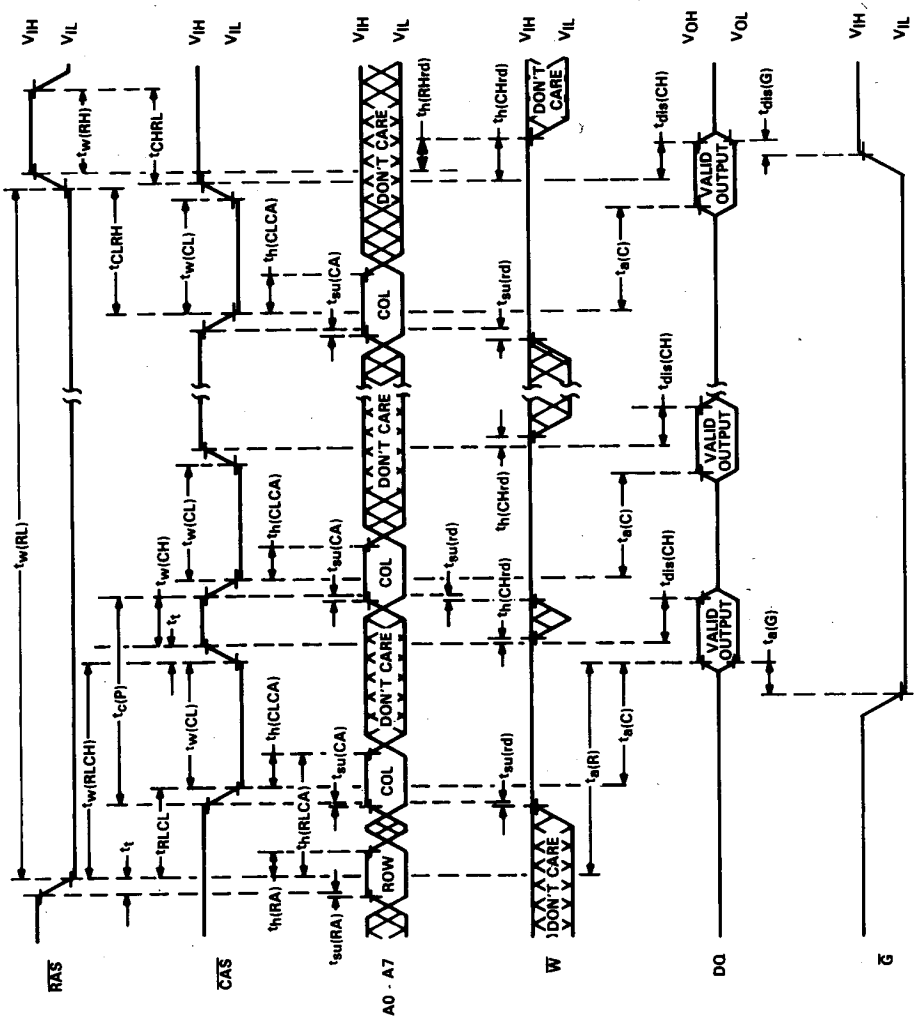
read-write/read-modify-write cycle timing



page-mode read cycle timing



NOTE 6. A write cycle or read-modify-write cycle can be intermixed with read cycles as long as the write and read-modify-write timing specifications are not violated.

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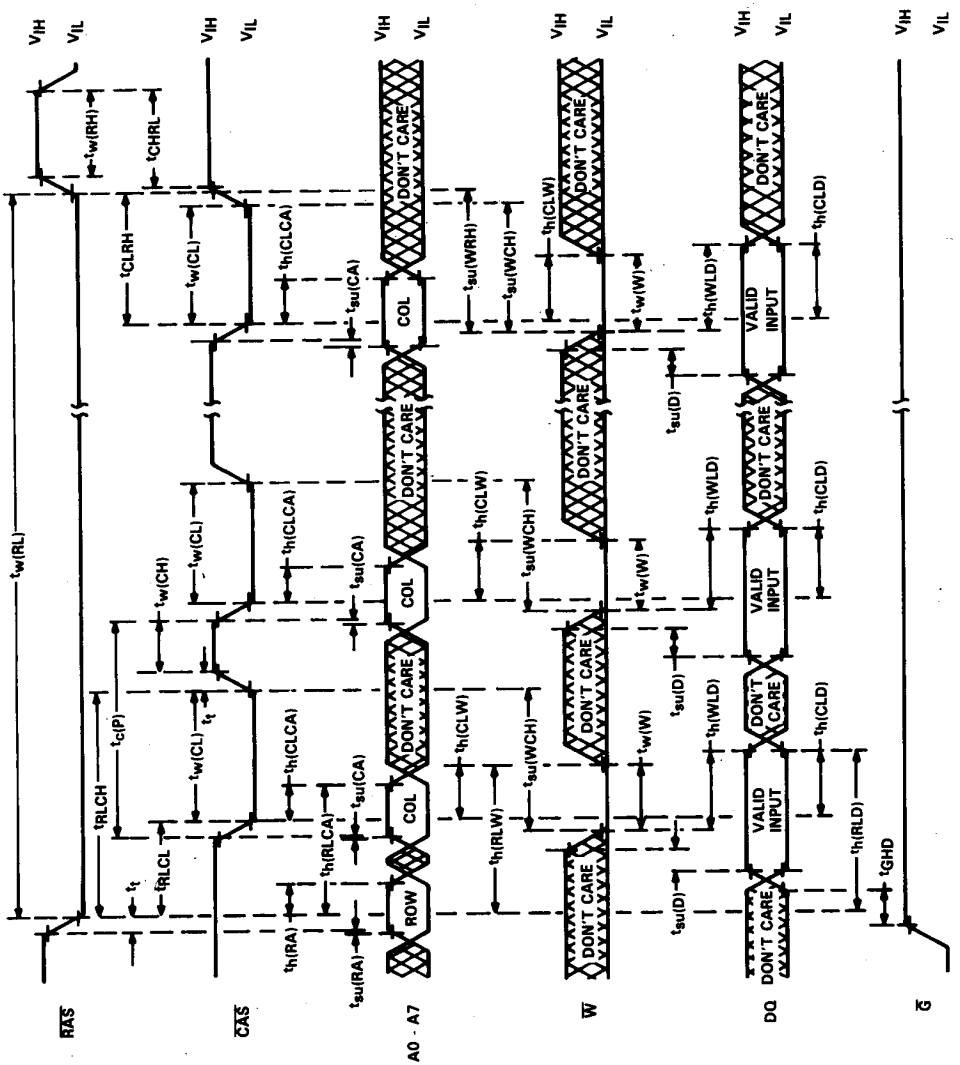
page-mode write cycle timing



NOTE 7. A read cycle or a read-modify-write cycle can be intermixed with write cycles as long as read and read-modify-write timing specifications are not violated.

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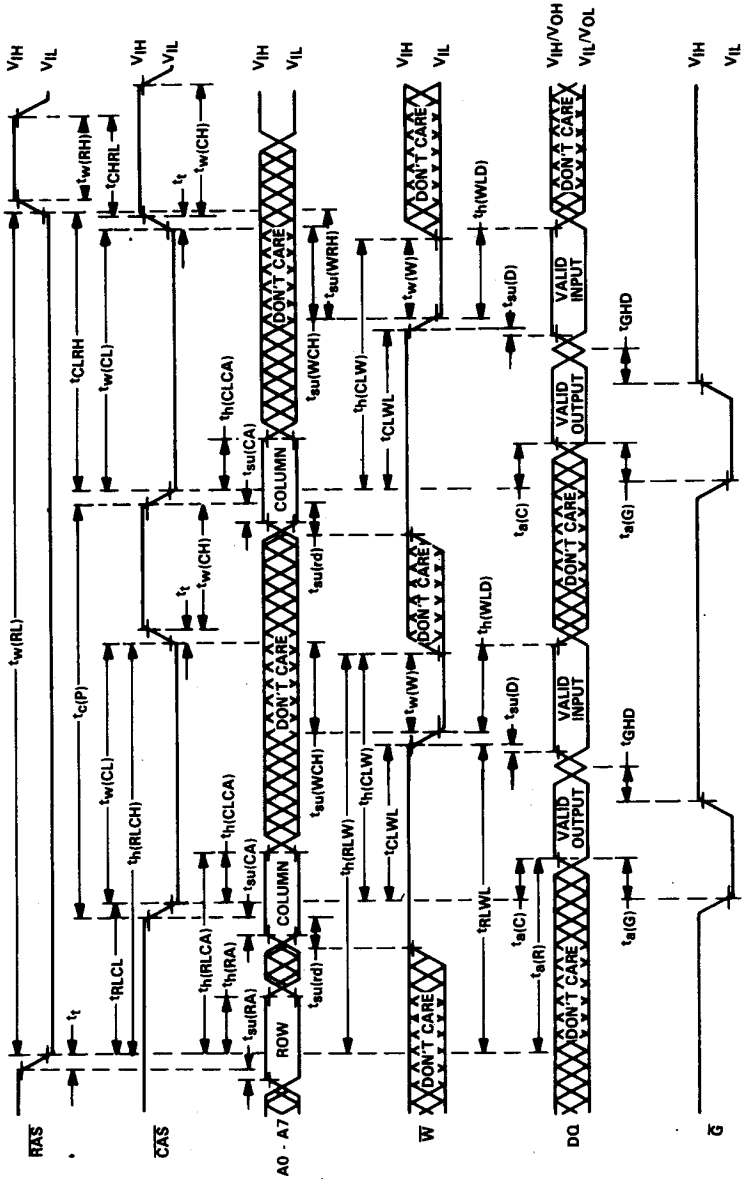
page-mode read-modify-write timing



NOTE 8. A read cycle or a write cycle can be intermixed with read-modify-write cycles as long as read and write timing specifications are not violated.

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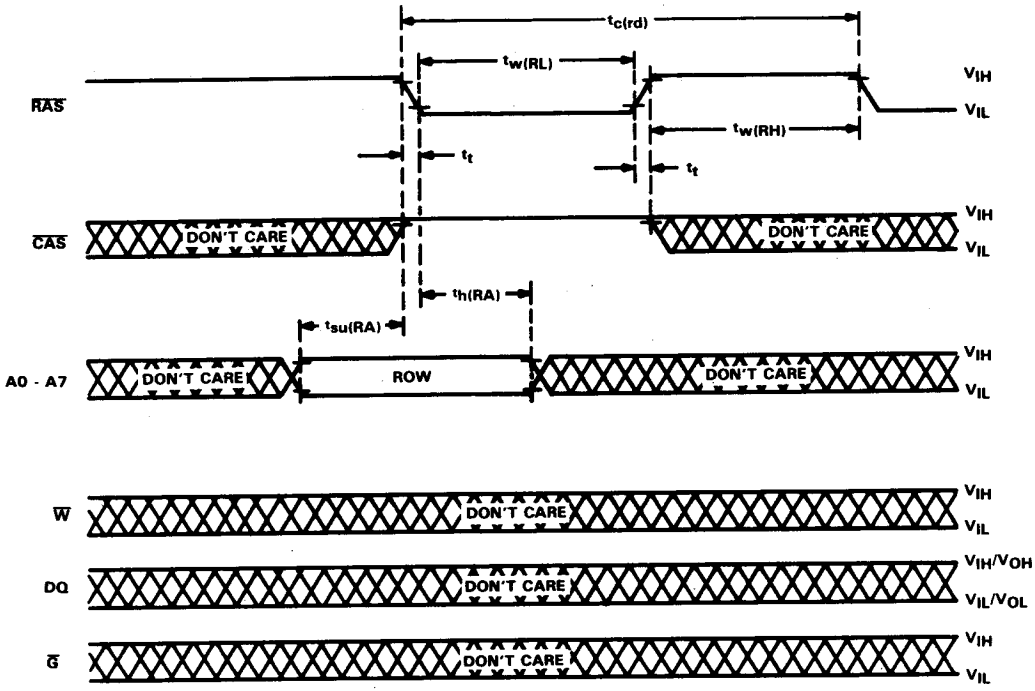
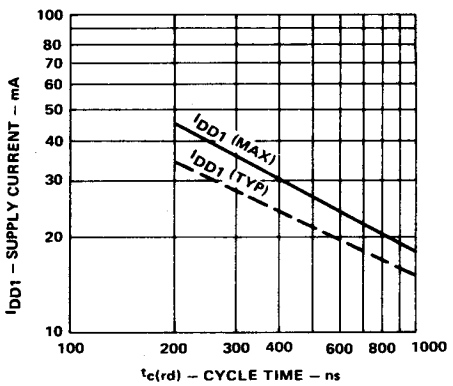
$\overline{\text{RAS}}$-only refresh timing



I_{DD1} VS CYCLE TIME



ACCESS TIME DERATING CURVE