



High-Speed CMOS Bus Interface 8-Bit Registers

QS54/74FCT374T
QS54/74FCT2374T

FEATURES/BENEFITS

- Pin and function compatible to the 74F374, 74FCT374 and 74ABT374
- Industrial temperature -40°C to 85°C
- CMOS power levels: $<7.5\text{mW}$ static
- Available in DIP, SOIC, QSOP, ZIP, HQSOP
- Undershoot clamp diodes on all inputs
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Military product compliant to MIL-STD-883, Class B

FCT-T 374T

- JEDEC-FCT spec compatible
- Std., A, C, and D speed grades with 4.5ns t_{PD} for D
- $I_{OL} = 48\text{mA}$ Ind., 32mA Mil.

FCT-T 2374T

- Built-in 25Ω series resistor outputs reduce reflection and other system noise
- Std., A and C speed grades with 5.2ns t_{PD} for C
- $I_{OL} = 12\text{mA}$ Ind.

DESCRIPTION

The QSFCT374T is a high-speed CMOS TTL-compatible 8-bit buffered registers with a buffered common clock and a buffered output enable control. The QSFCT2374T is a 25Ω resistor output version useful for driving transmission lines and reducing system noise. Data is stored in the register on the rising edge of the clock. The FCT374 is a non-inverting device. The high output current I_{OL} and I_{OH} drive high capacitance loads. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when V_{CC} is removed from the device.

Figure 1. Functional Block Diagram

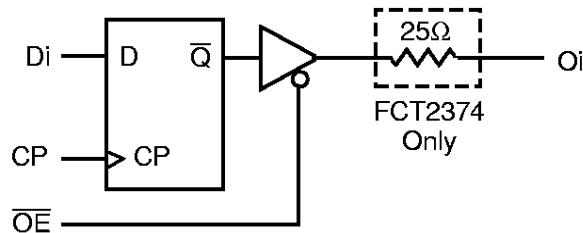


Figure 2. Pin Configurations (All Pins Top View)

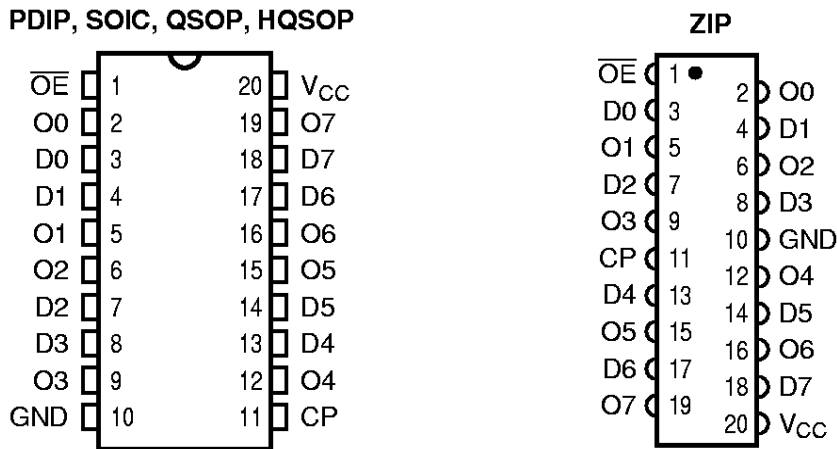


Table 1. Pin Description

Name	I/O	Description
D_i	I	Data Inputs
O_i	O	Data Outputs
CP	I	Clock Input
\overline{OE}	I	Output Enable

Table 2. Function Table

\overline{OE}	Inputs CP	D_i	Internal Q Value	Outputs O_i	Function
H	X	X	X	Hi-Z	Disable Outputs
L	\uparrow	L	L	L	Load Input Data
L	\uparrow	H	H	H	Enable Outputs
H	\uparrow	L	L	Hi-Z	Load Input Data
H	\uparrow	H	H	Hi-Z	Disable Outputs

Table 3. Absolute Maximum Ratings

Supply Voltage to Ground	-0.5V to 7.0V
DC Output Voltage V_{OUT}	-0.5V to 7.0V
DC Input Voltage V_{IN}	-0.5V to 7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	-3.0V
DC Input Diode Current with $V_{IN} < 0$	-20mA
DC Output Diode Current with $V_{OUT} < 0$	-50mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	0.5 watts
T_{STG} Storage Temperature	-65° to 150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

Table 4. Capacitance⁽¹⁾

$T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$, $V_{IN} = 0\text{V}$, $V_{OUT} = 0\text{V}$

Pins ⁽²⁾	SOIC	QSOP	PDIP	ZIP	Unit
1, 3, 4, 7, 8, 11, 13, 14, 17, 18	4	4	5	7	pF
2, 5, 6, 9, 12, 15, 16, 19	8	8	9	10	pF

Notes:

1. Capacitance is characterized but not tested.
2. Pin reference for 20-pin package.

Table 5. Power Supply Characteristics

Symbol	Parameter	Test Conditions ⁽¹⁾	Min	Max	Unit
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC}-0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	1.5	mA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}$, $V_{IN} = 3.4\text{V}$, freq = 0 ⁽²⁾	—	2.0	mA
Q_{CCD}	Supply Current per Input per MHz	$V_{CC} = \text{Max.}$, Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or V_{CC} ^(3,4)	—	0.25	mA/ MHz

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ($V_{IN} = 3.4\text{V}$).
3. For flip-flops, Q_{CCD} is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4. I_C can be computed using the above parameters as explained in the Technical Overview section.

Table 6. DC Electrical Characteristics Over Operating Range

Commercial $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 5\%$

Military $T_A = -55^{\circ}\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions	Min	Typ ⁽¹⁾	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	μA
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$	—	—	5	μA
I_{OS}	Short Circuit Current (FCT374)	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(2,3)}$	-60	—	—	mA
I_{OR}	Current Drive (FCT2374 - 25 Ω)	$V_{CC} = \text{Min.}, V_{OUT} = 2.0\text{V}^{(3)}$	50	—	—	mA
V_{IC}	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}, T_A = 25^{\circ}\text{C}^{(3)}$	—	-0.7	-1.2	V
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $I_{OH} = -12\text{mA}$ (MIL) $I_{OH} = -15\text{mA}$ (IND)	2.4 2.4	— —	— —	V
V_{OL}	Output LOW Voltage (FCT374)	$V_{CC} = \text{Min.}$ $I_{OL} = 32\text{mA}$ (MIL) $I_{OL} = 48\text{mA}$ (IND)	— —	— —	0.50 0.50	V
V_{OL}	Output LOW Voltage (FCT2374 - 25 Ω)	$V_{CC} = \text{Min.}$ $I_{OL} = 12\text{mA}$ (MIL) $I_{OL} = 12\text{mA}$ (IND)	— —	— —	0.50 0.50	V
R_{OUT}	Output Resistance (FCT2374 - 25 Ω)	$V_{CC} = \text{Min.}$ $I_{OL} = 12\text{mA}$ (MIL) $I_{OL} = 12\text{mA}$ (IND)	— 20	25 28	— 40	Ω

Notes:

1. Typical values indicate $V_{CC} = 5.0\text{V}$ and $T_A = 25^{\circ}\text{C}$.
2. Not more than one output should be shorted and the duration is ≤ 1 second.
3. These parameters are guaranteed by design but not tested.

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Table 7. Switching Characteristics Over Operating Range

Industrial $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 5.0\text{V} \pm 5\%$

Military $T_A = -55^\circ\text{C}$ to 125°C , $V_{CC} = 5.0\text{V} \pm 10\%$

$C_{LOAD} = 50\text{pF}$, $R_{LOAD} = 500\Omega$ unless otherwise noted.

Symbol	Description ⁽¹⁾		374 2374		374A 2374A		374C 2374C		374D		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay CP to Oi, 374	IND MIL	2 2	10 11	2 2	6.5 7.2	2 2	5.2 6	1.5 —	4.5 —	ns
t_{PHL} t_{PLH}	Propagation Delay CP to Oi, 2374	IND MIL	2 2	10 11	2 2	6.5 7.2	2 2	5.2 6	— —	— —	ns
t_{PZH} t_{PZL}	Output Enable Time \overline{OE} to Yi, 374	IND MIL	1.5 1.5	12.5 14	1.5 1.5	6.5 7.5	1.5 1.5	5.5 6.2	1.5 —	5.5 —	ns
t_{PZH} t_{PZL}	Output Enable Time \overline{OE} to Yi, 2374	IND MIL	1.5 1.5	12.5 14	1.5 1.5	6.5 7.5	1.5 1.5	6.2 6.9	— —	— —	ns
t_{PHZ} t_{PLZ}	Output Disable Time \overline{OE} to Yi	IND ⁽²⁾ MIL ⁽²⁾	1.5 1.5	8 8	1.5 1.5	5.5 6.5	1.5 1.5	5 6.5	1.5 —	5 —	ns
t_S	Data Setup Time Di to CP	IND MIL	2 2	— —	2 2	— —	1.5 2	— —	1.5 —	— —	ns
t_H	Data Hold Time Di to CP	IND MIL	1.5 1.5	— —	1.5 1.5	— —	1 1	— —	1 —	— —	ns
t_W	Clock Pulse Width HIGH or LOW	IND ⁽²⁾ MIL ⁽²⁾	7 7	— —	5 6	— —	4 5	— —	4 —	— —	ns

Notes:

1. Minimums guaranteed but not tested for all parameters except t_S and t_H .
2. This parameter is guaranteed by design but not tested.
3. See Test Circuit and Waveforms.