National Semiconductor

MICROCIRCUIT DATA SHEET

MJCD4013B-X REV 1A0

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BUFFERED DUAL D FLIP-FLOP

General Description

The CD4013B buffered dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

Industry Part Number

CD4013B

NS Part Numbers

JM4013BBCA
JM4013BBDA

Prime Die

CD4013B

Controlling Document

38510/05151, AMEND.3

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

(Absolute Maximum Ratings)
(Note 1, 2)

DC Supply Voltage (Vdd)	-0.5Vdc to +18Vdc
Input Voltage (Vin)	-0.5Vdc to Vdd +0.5Vdc
Storage Temperature Range (Ts)	-65 C to +150 C
Power Dissipation (Pd)	200mW
Lead Temperature (Tl) (Soldering, 10 seconds)	300C
Junction Temperature (tJ)	175C
Thermal Resistance, junction-to-case	See Mil-M-38510
Input Current (each input)	±10mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.
Note 2: Vss = 0V unless otherwise specified.

Recommended Operating Conditions
(Note 1)

DC Supply Voltage (Vdd)	+4.5Vdc to +15Vdc
Input Voltage (Vil)	
Vdd = 5V	0.0V to 1.5V
Vdd = 10V	0.0V to 2.0V
Vdd = 15V	0.0V to 4.0V
Operating Temperature Range (TA)	
CD4013BM	-55 C to +125 C
Input Voltage (Vih)	
Vdd = 5.0V	3.5V to 5.0V
Vdd = 10V	8.0 to 10.0V
Vdd = 15V	11.0 to 15.0V

Note 1: Vss = 0V unless otherwise specified.

Electrical Characteristics

DC PARAMETERS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
Vic+ (POS)	Input Clamping Voltage	VCC = Gnd, VSS= Open, Output = Open, IIN = 1mA	5, 6	INPUT		1.5	V	1
Vic- (NEG)	Input Clamping Voltage	VCC = Open, VSS = Gnd, Output = Open, IIN = -1mA	5, 6	INPUT		-6.0	V	1
Iss	Power Supply Current	VCC = 18.0V, VM=0.0V	3, 4	Vss		-0.25	uA	1
			3, 4	Vss		-2.5	uA	2
VOH	Output High Voltage	VCC = 15.0V, IOH = 0.0uA	1, 2	OUTPUT	14.95		V	1, 2, 3
VOL	Output Low Voltage	VCC = 15.0V, IOL = 0.0uA	1, 2	OUTPUT		0.05	V	1, 2, 3
IOL	Low Level Output Current	VCC = 5.0V, VOL = 0.4V	1, 2, 9	OUTPUT	0.51		mA	1
			1, 2, 9	OUTPUT	0.36		mA	2
			1, 2, 9	OUTPUT	0.64		mA	3
		VCC = 15.0V, VOL = 1.5V	1, 2, 9	OUTPUT	3.4		mA	1
			1, 2, 9	OUTPUT	2.4		mA	2
			1, 2, 9	OUTPUT	4.2		mA	3
IOH	High Level Output Current	VCC = 5.0V, VOH = 4.6V	1, 2, 9	OUTPUT	-0.51		mA	1
			1, 2, 9	OUTPUT	-0.36		mA	2
			1, 2, 9	OUTPUT	-0.64		mA	3
		VCC = 15.0V, VOH = 13.5V	1, 2, 9	OUTPUT	-3.4		mA	1
			1, 2, 9	OUTPUT	-2.4		mA	2
			1, 2, 9	OUTPUT	-4.2		mA	3
IIH	Input High Current	VCC = 18.0V	3, 4	INPUT		100	nA	1, 2
IIL	Input Low Current	VCC = 18.0V	3, 4	INPUT		-100	nA	1, 2

Electrical Characteristics

DC PARAMETERS(Continued)

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
VIH	Input Voltage High	VCC = 5.0V, VOUT = 4.5V, IOUT ≤ 1uA	1, 2, 9	INPUT	3.5		V	1, 2, 3
		VCC = 10.0V, VOUT = 9.0V, IOUT ≤ 1uA	1, 2, 9	INPUT	7.0		V	1, 2, 3
		VCC = 15.0V, VOUT = 13.5V, IOUT ≤ 1uA	1, 2, 9	INPUT	11.0		V	1, 2, 3
VIL	Input Voltage Low	VCC = 5.0V, VOUT = 0.5V, IOUT ≤ 1uA	1, 2, 9	INPUT		1.5	V	1, 2, 3
		VCC = 10.0V, VOUT = 1.0V, IOUT ≤ 1uA	1, 2, 9	INPUT		3.0	V	1, 2, 3
		VCC = 15.0V, VOUT = 1.5V, IOUT ≤ 1uA	1, 2, 9	INPUT		4.0	V	1, 2, 3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VDD = 5V, CL = 50pF, RL = 200K Ohms, tR/tF=20nS±2nS

tPHL	Propagation Delay		7, 8	CLK to Q/$\overline{Q}$	13.0	500	nS	9, 11
			7, 8	CLK to Q/$\overline{Q}$	18.0	750	nS	10
			7, 8	SET to Q/RS to $\overline{Q}$	13.0	550	nS	9, 11
			7, 8	SET to Q/RS to $\overline{Q}$	18.0	825	nS	10
tPLH	Propagation Delay		7, 8	CLK to Q/$\overline{Q}$	13.0	550	nS	9, 11
			7, 8	CLK to Q/$\overline{Q}$	18.0	825	nS	10
			7, 8	SET to Q/RS to $\overline{Q}$	13.0	420	nS	9, 11
			7, 8	SET to Q/RS to $\overline{Q}$	18.0	630	nS	10
tTHL	Transition Time		7, 8	Q/$\overline{Q}$	10.0	300	nS	9, 11
			7, 8	Q/$\overline{Q}$	14.0	450	nS	10
tTLH	Transition Time		7, 8	Q/$\overline{Q}$	10.0	350	nS	9, 11
			7, 8	Q/$\overline{Q}$	14.0	525	nS	10

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VDD = 5V, CL = 50pF, RL = 200K Ohms, tR/tF=20nS±2nS

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
fCL(MAX)	Maximum Clock frequency		7, 8	CLK		0.67	uS	9, 11
			7, 8	CLK		1.0	uS	10
tTLHCL (MAX)	Maximum Clock Transition Time		7, 8	CLK	15.0		uS	9, 10
			7, 8	CLK	10.0		uS	11
tP	Minimum Clock Pulse Width		7, 8	CLK		300	nS	9, 11
			7, 8	CLK		450	nS	10
tSHL	Setup Times		7, 8	D to CLK		165	nS	9, 11
			7, 8	D to CLK		225	nS	10
tSLH	Setup Times		7, 8	D to CLK		165	nS	9, 11
			7, 8	D to CLK		225	nS	10
tHHL	Hold Times		7, 8	D to CLK		150	nS	9, 11
			7, 8	D to CLK		225	nS	10
tHLH	Hold Times		7, 8	D to CLK		150	nS	9, 11
			7, 8	D to CLK		225	nS	10
CIN	Input Capacitance	VDD = 0.0V, f = 1MHz	10			12.0	pF	4

DC PARAMETERS: DRIFT VALUES

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Delta calculations performed at production burn-in and group C (operational life test).

ISS	Quiescent Supply Current	VCC = 18.0V, VM=0.0V	12	VSS	-0.075	0.075	uA	1
IOL	Output Current Low	VCC = 5.0V, VOL = 0.4V	12	OUTPUT	-15.0	15.0	%	1
IOH	Output Current High	VCC = 5.0V, VOH = 4.6V	12	OUTPUT	-15.0	15.0	%	1

Note 1: Screen tested 100% on each device at +25C, +125C and -55C temperature, subgroups A1, 2 & 3.
Note 2: Sample tested (Method 5005, table 1) on each MFG. lot at +25C, +125C and -55C temperature, subgroups A1, 2 & 3.
Note 3: Screen tested 100% on each device at +25C and -55C temperature only, subgroups A1 & 2.
Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C & +125C temperature only, subgroups A1 & 2.

(Continued)

Note 5: Screen tested 100% on each device at +25C temperature only, Subgroup A1.
Note 6: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C temperature only, subgroup A1.
Note 7: Screen tested 100% on each device at +25C temperature only, subgroup A9.
Note 8: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C and -55C temperature, subgroups A9, 10 & 11.
Note 9: VIL, VIH, IOL and IOH are guaranteed by applying specified conditions and testing VOL and VOH.
Note 10: Guaranteed parameter. This test is only performed during qualification.
Note 11: Guaranteed parameter, not tested.
Note 12: Drift Values need not be calculated if post burn-in electrical test is performed within 24 hours after burn-in.

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A0	M0003591	11/17/99	Linda Collins	Conversion from JRETS to MDS. Obsolete JRETS4013BX Rev. 1E. Release to MDS: MJCD4013B-X Rev. 1A0. Changed IIH max limits from 1nA and 45nA to 100nA. Changed IIL max limits from -1nA and -45nA to -100nA.